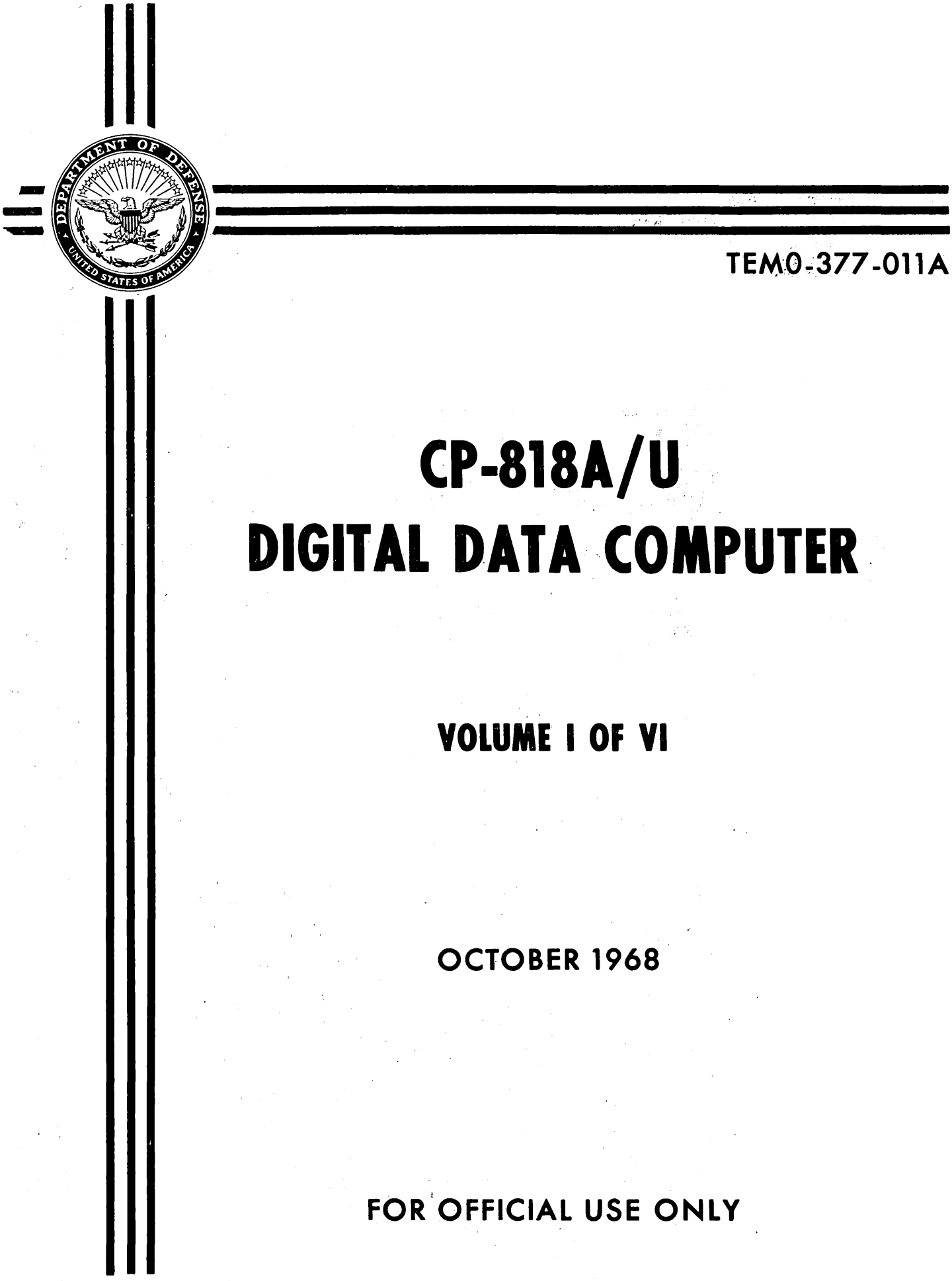


TEM0-377-011A

CP-818A/U
DIGITAL DATA COMPUTER

VOLUME I OF VI

OCTOBER 1968

FOR OFFICIAL USE ONLY

INTRODUCTION

This manual contains instructions for operation and maintenance of the CP-818A/U Digital Data Computer. It is one of a series of manuals which contain operation and maintenance instructions for the AN/GYK-9A(V) Data Processing Set.

Chapter 1 describes the equipment and its purpose; Chapter 2 contains installation instructions; Chapter 3 the operating instructions; and Chapter 4 principles of operation. Chapter 5 contains preventive maintenance procedures required to maintain the equipment in operational readiness. Chapter 6 contains corrective maintenance procedures, Chapter 7 an illustrated parts breakdown, Chapter 8 the functional schematics, and Chapter 9 wiring information. Chapter 10 contains maintenance routines, and Chapter 11 contains diagnostic tests. These chapters are contained in the following volumes.

Chapter		Volume
1	Description of Equipment	I
2	Installation	I
3	Operating Instructions	I
4	Principles of Operation	I
5	Preventive Maintenance	I
6	Corrective Maintenance	I
7	Illustrated Parts Breakdown	I
8	Functional Schematics	II
9	Wire Tabulations	III
10	Maintenance Routines	IV
11	Diagnostic Routines	V, VI

RECORD OF CHANGES

IDENTIFICATION OF CORRECTION OR CHANGE AND REG. NO. (IF ANY)	DATE ENTERED	BY WHOM ENTERED (SIGNATURE; RANK OR RATE; NAME OF COMMAND)

WARNING

HIGH VOLTAGE

IS USED IN THE OPERATION
OF THIS EQUIPMENT

DEATH ON CONTACT

MAY RESULT IF OPERATING PERSONNEL
FAIL TO OBSERVE SAFETY PRECAUTIONS

BE CAREFUL TO AVOID CONTACT WITH HIGH-VOLTAGE CIRCUITS
OR 115VAC INPUT CONNECTIONS WHILE CHECKING OR
SERVICING THIS EQUIPMENT

Mouth-to-Mouth (Mouth-to-Nose) Method of ARTIFICIAL RESPIRATION

If there is foreign matter visible in the mouth, wipe it out quickly with your fingers or a cloth wrapped around your fingers.

a. Tilt the head back so the chin is pointing upward (Fig. 1). Pull or push the jaw into a jutting-out position (Fig. 2 and 3).
These maneuvers should relive obstruction of the airway by moving the base of the tongue away from the back of the throat.


Fig. 1


Fig. 2

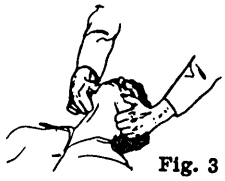


Fig. 3

b. Open your mouth wide and place it tightly over the victim's mouth. At the same time pinch the victim's nostrils shut (Fig. 4) or close the nostrils with your cheek (Fig. 5). Or close the victim's and place your mouth over the nose (Fig. 6). Blow into the victim's mouth or nose. (Air may be blown through the victim's teeth, even though they may be clenched.)
The first blowing efforts should determine whether or not obstruction exists.

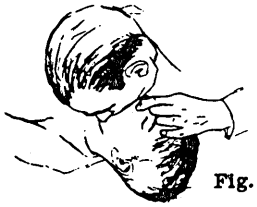


Fig. 4


Fig. 5

c. Remove your mouth, turn your head to the side, and listen for the return rush of air that indicates air exchange. Repeat the blowing effort.
For an adult, blow vigorously at the rate of about 12 breaths per minute. For a child, take relatively shallow breaths appropriate for the child's size, at the rate of about 20 per minute.

d. If you are not getting air exchange, recheck the head and jaw position (Fig. 1 or Fig. 2 and Fig. 3). If you still do not get air exchange, quickly turn the victim on his side and administer several sharp blows between the shoulder blades in the hope of dislodging foreign matter (Fig. 7).
Again sweep your fingers through the victim's mouth to remove foreign matter.


Fig. 6

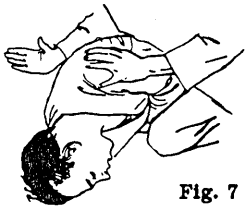


Fig. 7

Those who do not wish to come in contact with the person may hold a cloth over the victim's mouth or nose and breathe through it. The cloth does not greatly affect the exchange of air.

Holger-Nielson Method of ARTIFICIAL RESPIRATION

1 POSITION OF THE SUBJECT: Place the subject in the face down, prone position. Bend his elbows and place the hands one upon the other. Turn his face to one side, placing the cheek upon his hands.

2 POSITION OF THE OPERATOR: Kneel on either the right or left knee at the head of the subject, facing him. Place the knee at the side of the subject's head close to the forearm. Place the opposite foot near the elbow. If it is more comfortable, kneel on both knees, one on either side of the subject's head. Place your hands upon the flat of the subject's back in such a way that the palms lie just below a line running between the armpits. With the tips of the thumbs just touching, spread the fingers downward and outward.

3 COMPRESSION PHASE: Rock forward until the arms are approximately vertical and allow the weight of the upper part of your body to exert slow, steady, even pressure downward upon the hands. This forces air out of the lungs. Your elbows should be kept straight and the pressure exerted almost directly downward on the back.

4 EXPANSION PHASE: Release the pressure, avoiding a final thrust, and commence to rock slowly, backward. Place your hands upon the subject's arms just above his elbows, and draw his arms upward and toward you. Apply just enough lift to feel resistance and tension at the subject's shoulders. Do not bend your elbows, and as you rock backward the subject's arms will be drawn towards you. Then drop the arms gently to the ground. This completes the full cycle. The arm-lift expands the chest by pulling on the chest muscles, arching the back, and relieving the weight on the chest.

The cycle should be repeated 12 times per minute at a steady, uniform rate. The compression and expansion phases should occupy about equal time; the release period being of minimum duration.

5 ADDITIONAL RELATED DIRECTIONS: It is important that artificial respiration, when needed, should be started quickly. There should be a slight inclination of the body in such a way that fluid drains better from the respiratory passage. The head of the subject should be extended, not flexed forward, and the chin should not sag lest obstruction of the respiratory passages occur.

A check should be made to ascertain that the tongue or foreign objects are not obstructing the passages. These aspects can be cared for when placing the subject into position or shortly thereafter, between cycles.

A smooth rhythm in performing artificial respiration is desirable, but split-second timing is not essential. Shock should receive adequate attention, and the subject should continue to rest after resuscitation until seen by a physician or until recovery seems assured.

TABLE OF CONTENTS

CHAPTER 1

DESCRIPTION OF EQUIPMENT

CHAPTER 2

INSTALLATION

TABLE OF CONTENTS (continued)

TABLE OF CONTENTS (continued)

TABLE OF CONTENTS (continued)

TABLE OF CONTENTS (continued)

TABLE OF CONTENTS (continued)

TABLE OF CONTENTS (continued)

TABLE OF CONTENTS (continued)

CHAPTER 9 (VOLUME III)

WIRE TABULATIONS

CHAPTER 10 (VOLUME IV)

MAINTENANCE ROUTINES

TABLE OF CONTENTS (continued)

CHAPTER 11

DIAGNOSTIC ROUTINES

TABLE OF CONTENTS (continued)

CHAPTER 11

DIAGNOSTIC ROUTINES

TABLE OF CONTENTS (continued)

CHAPTER 11

DIAGNOSTIC ROUTINES

TABLE OF CONTENTS (continued)

CHAPTER 11

DIAGNOSTIC ROUTINES

TABLE OF CONTENTS (continued)

CHAPTER 11

DIAGNOSTIC ROUTINES

LIST OF ILLUSTRATIONS

VOLUME 1

LIST OF ILLUSTRATIONS (continued)

LIST OF ILLUSTRATIONS (continued)

LIST OF ILLUSTRATIONS (continued)

VOLUME II

LIST OF ILLUSTRATIONS (continued)

LIST OF ILLUSTRATIONS (continued)

LIST OF ILLUSTRATIONS (continued)

VOLUME III

LIST OF ILLUSTRATIONS (continued)

VOLUME IV

LIST OF ILLUSTRATIONS (continued)

LIST OF TABLES

VOLUME I

LIST OF TABLES (continued)

LIST OF TABLES (continued)

LIST OF TABLES (continued)

VOLUME IV

LIST OF TABLES (continued)

VOLUME IV

VOLUME V

LIST OF TABLES (continued)

LIST OF TABLES (continued)

LIST OF TABLES (continued)

LIST OF TABLES (continued)

VOLUME VI

LIST OF TABLES (continued)

LIST OF TABLES (continued)

LIST OF TABLES (continued)

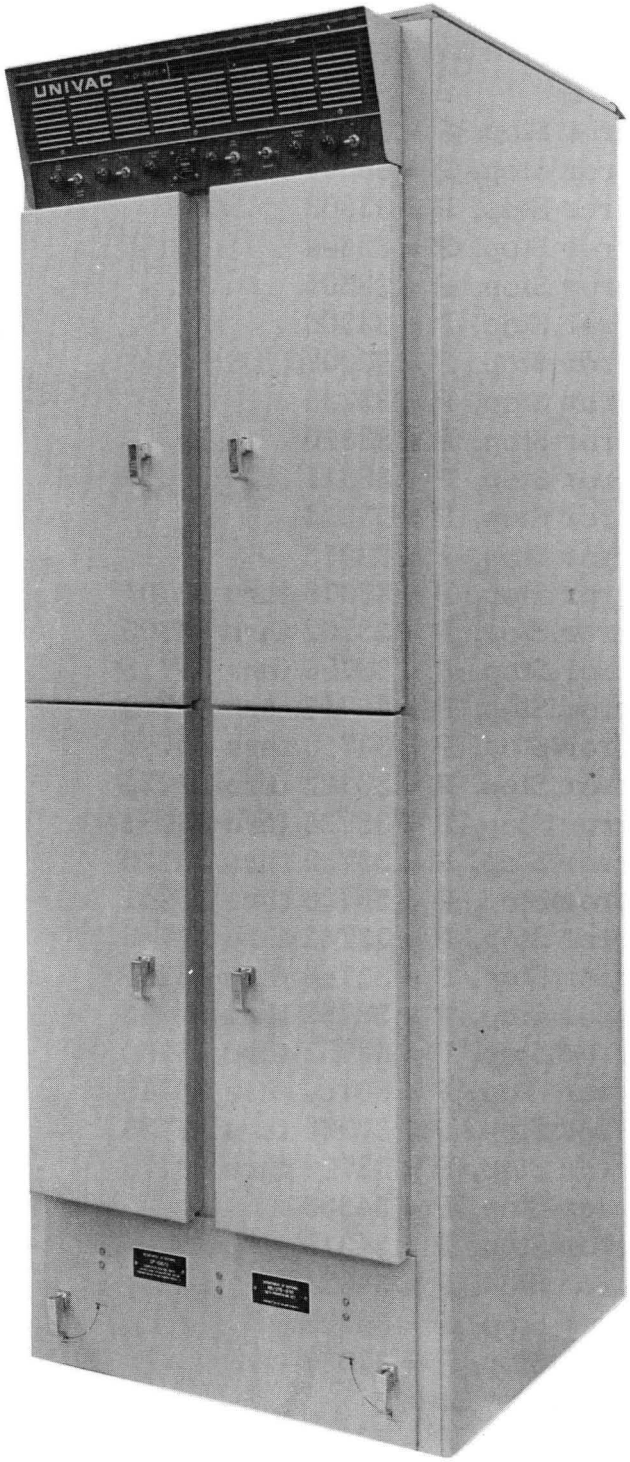


Figure 1-1. CP-818A/U Digital Data Computer (Frontispiece)

CHAPTER 1

DESCRIPTION OF EQUIPMENT

I - CLASSIFICATION

1-1. CLASSIFICATION OF EQUIPMENT. - The CP-818A/U Digital Data Computer (figure 1-1, page xlvi) and associated manuals are UNCLASSIFIED. However, the system and associated equipments may carry a higher classification.

NOTE - SECURITY REQUIREMENT

The memory core stacks may contain classified information. Clear each core stack to all ones or all zeros before removal.

II - FUNCTIONAL DESCRIPTION

1-2. SYSTEM DESCRIPTION (figure 1-2, page 1-2). - The CP-818A/U computer controls the AN/GYK-9A(V) Data Processing set. The set consists of the following equipments:

1) A magnetic tape subsystem of up to eight tape transports controlled via the C-6573A/GYK-9A(V) Magnetic Tape Control Unit (TCU).

2) Up to four OA-7385A/GYK-9A(V) Control-Indicator Group Consoles.

3) A printer/punch system of up to 40 printers or punches. The C-6572A/GYK-9A(V) Printer-Punch Control Unit (PCU) provides buffering for 40 printers or punches.

4) An auxiliary CP-818A/U Digital Data Computer (optional).

5) A paper tape unit (PTU), the RD-277A/GYK-9A(V) Perforator-Reader, with a reader and punch.

1-3. CP-818A/U COMPUTER. - The CP-818A/U computer is a special-purpose, flexible-format, digital computer. It operates as a flexible format

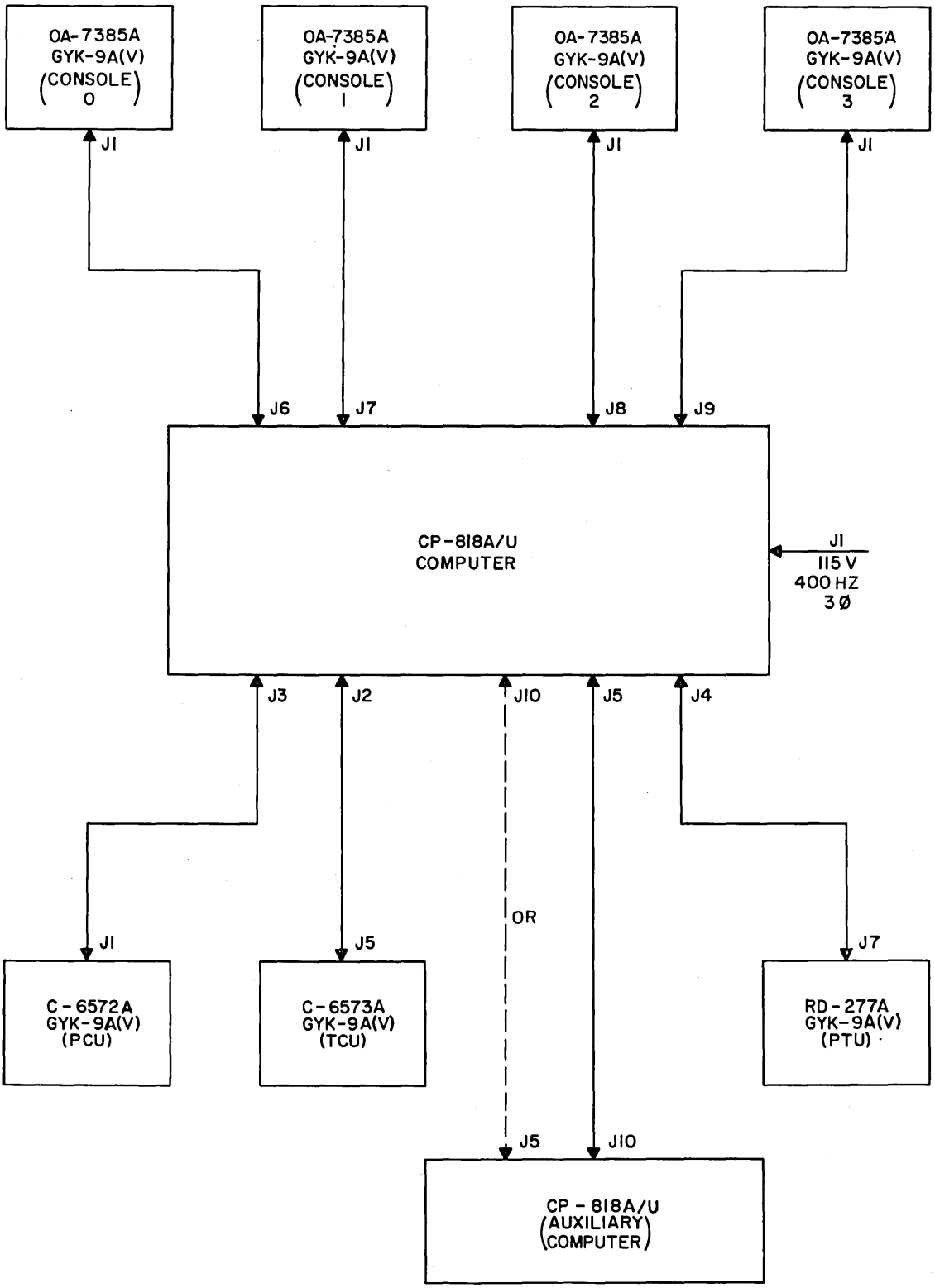


Figure 1-2. Simplified System Block Diagram

control unit between various types of digital peripheral units and processes data characters of varying lengths and formats. An internally-stored program controls buffered input/output operations and real-time, on-line operations. Functionally the computer contains five sections: control, arithmetic, input/output, memory and power. Except for memory and power the sections do not reflect any division of hardware.

a. Control Section. - The control section consists of a series of registers and command circuits that time and control the internal operations as each instruction is performed. The control section causes an instruction to be read from the memory section and translates this instruction to generate the commands required to perform the instruction.

A master clock generates the timing pulses that control the sequence of events during the execution of each instruction. The master clock cycle is 0.67 microseconds. Six cycles make up one 4-microsecond sequence. A complete instruction may require one or more sequences.

b. Arithmetic Section. - The arithmetic section contains a subtractive type adder and a series of registers. The registers and adder perform the arithmetic and logical operations required during execution of an instruction. All arithmetic operations are performed in a parallel mode with one's-complement binary arithmetic (except for multiply and divide which are limited to positive numbers). Operations performed by the arithmetic section involve addition, subtraction, multiplying, dividing, complementing, shifting, updating the program address, and modifying operand addresses.

c. Input/Output Section. - The input/output section contains the data paths and control circuits for the eight input/output (I/O) channels. Each I/O channel provides a data communication path to and/or from a peripheral device. The I/O section uses assigned memory addresses to store control words for each channel. The control words in turn specify the memory area affected by the I/O operation and dictate placement of I/O data characters. A data character can consist of 1, 2, 3, 6, or 8 bits. The control words are loaded as part of the program and can be examined or altered by program steps; however, they are referenced automatically during I/O operations. The I/O section uses a request-acknowledge or interrupt operation to establish real-time communication with each device. A priority network determines precedence in cases of simultaneous I/O requests from two or more peripheral units.

d. Memory Section. - The memory section consists of a main core memory and a bootstrap memory. The main core memory contains 16,368 core storage locations. Each location stores a 26-bit word that consists of 24 data bits and two parity bits. The main memory stores the program instructions, program operands, and data. The main memory cycle time is four microseconds. The bootstrap memory consists of 16 nondestructive-readout storage locations and contains two 8-word program loading routines. The routines are used exclusively for loading utility programs that load the operational programs.

The control section initiates the memory, accepts the memory output, or supplies the words written into memory.

e. Power Section. - The power section contains the voltage control, supply, and distribution circuits. It receives the 115 vac input, converts it to the various dc voltages, and provides voltage distribution to the logic and memory circuits.

III - PHYSICAL DESCRIPTION

1-4. PHYSICAL CHARACTERISTICS. - The computer cabinet is 71.72 inches high, 25.88 inches wide, 29.30 inches deep, and weighs approximately 850 pounds. It contains two pullout logic drawers (A1 and A2), two pullout memory drawers (A3 and A4), a pullout power supply drawer (PS1), a power control panel (A5), and two blower assemblies (A6 and A7) (figures 1-3, page 1-5, and 1-4, page 1-6). Each logic drawer contains two logic chassis and a front door panel (figure 1-5, page 1-7). Each chassis can hold 245 printed circuit cards and has two test point blocks. The logic door panels contain the associated switches and indicators. Each memory drawer contains one chassis. Each chassis can hold 154 printed circuit cards, four memory stacks, a test block, and a bootstrap assembly (figure 1-6, page 1-8). Each memory stack contains 4,096 13-bit words. The bootstrap assembly consists of four printed circuit cards bolted together and contains 16 13-bit words. Each blower assembly contains two blowers to provide cabinet cooling. The power supply drawer contains the dc voltage supplies and fuses (see figure 1-7, page 1-9). All power and signal cabling connects to the computer via a connector assembly on the top rear portion of the cabinet.

1-5. TECHNICAL CHARACTERISTICS. - Table 1-1, page 1-10, lists the technical characteristics of the computer.

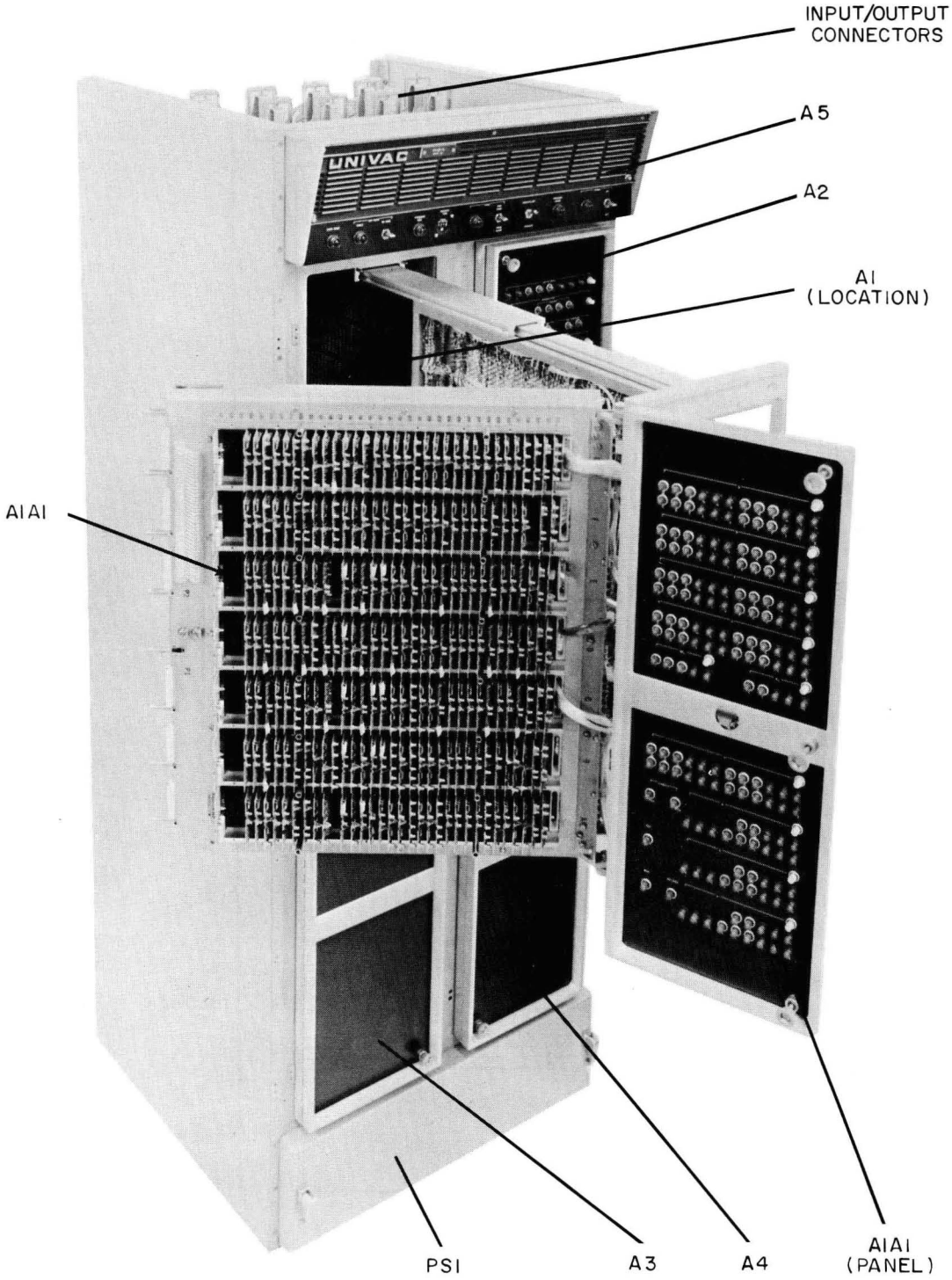


Figure 1-3. Assembly Locations

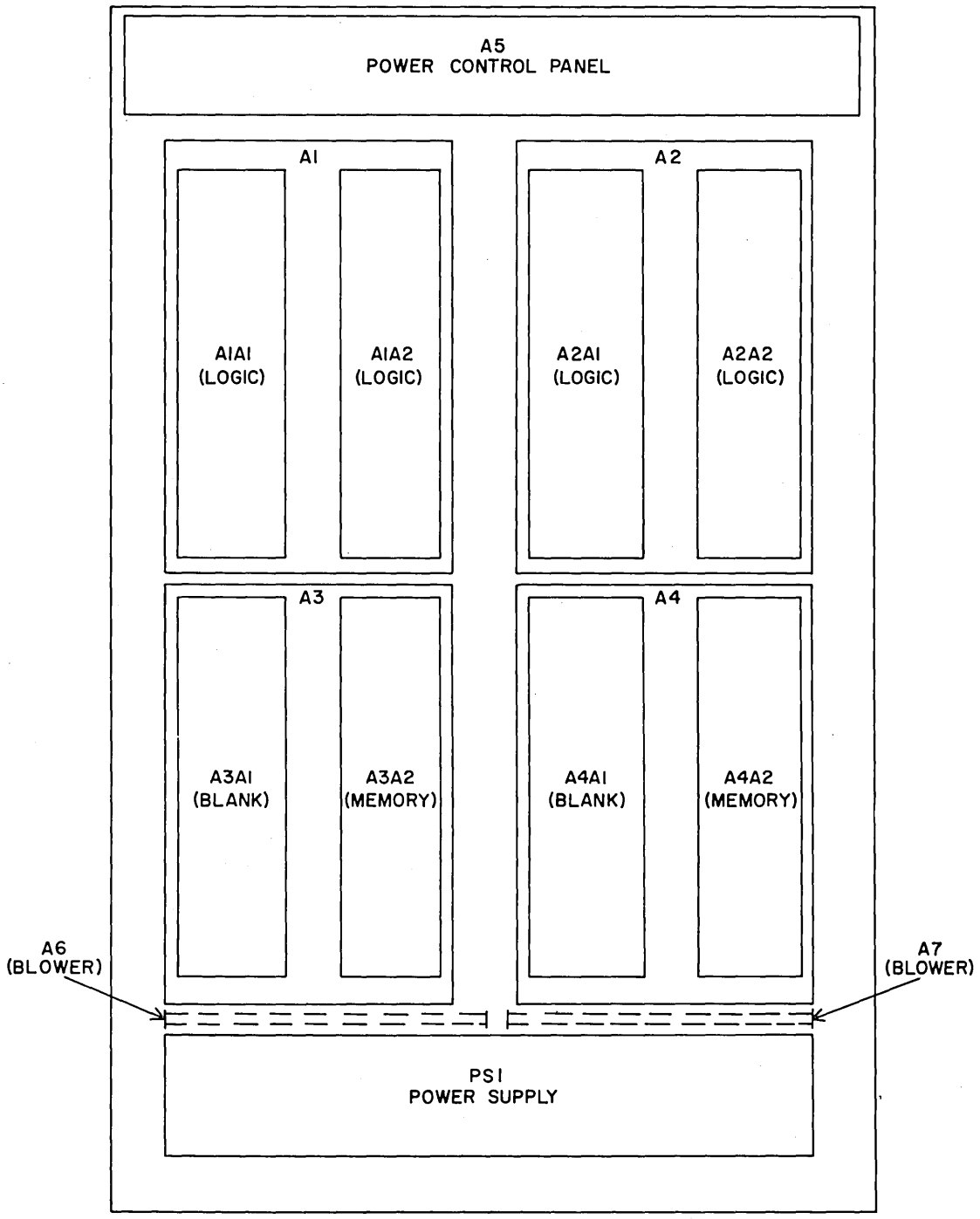


Figure 1-4. Assembly Numbering

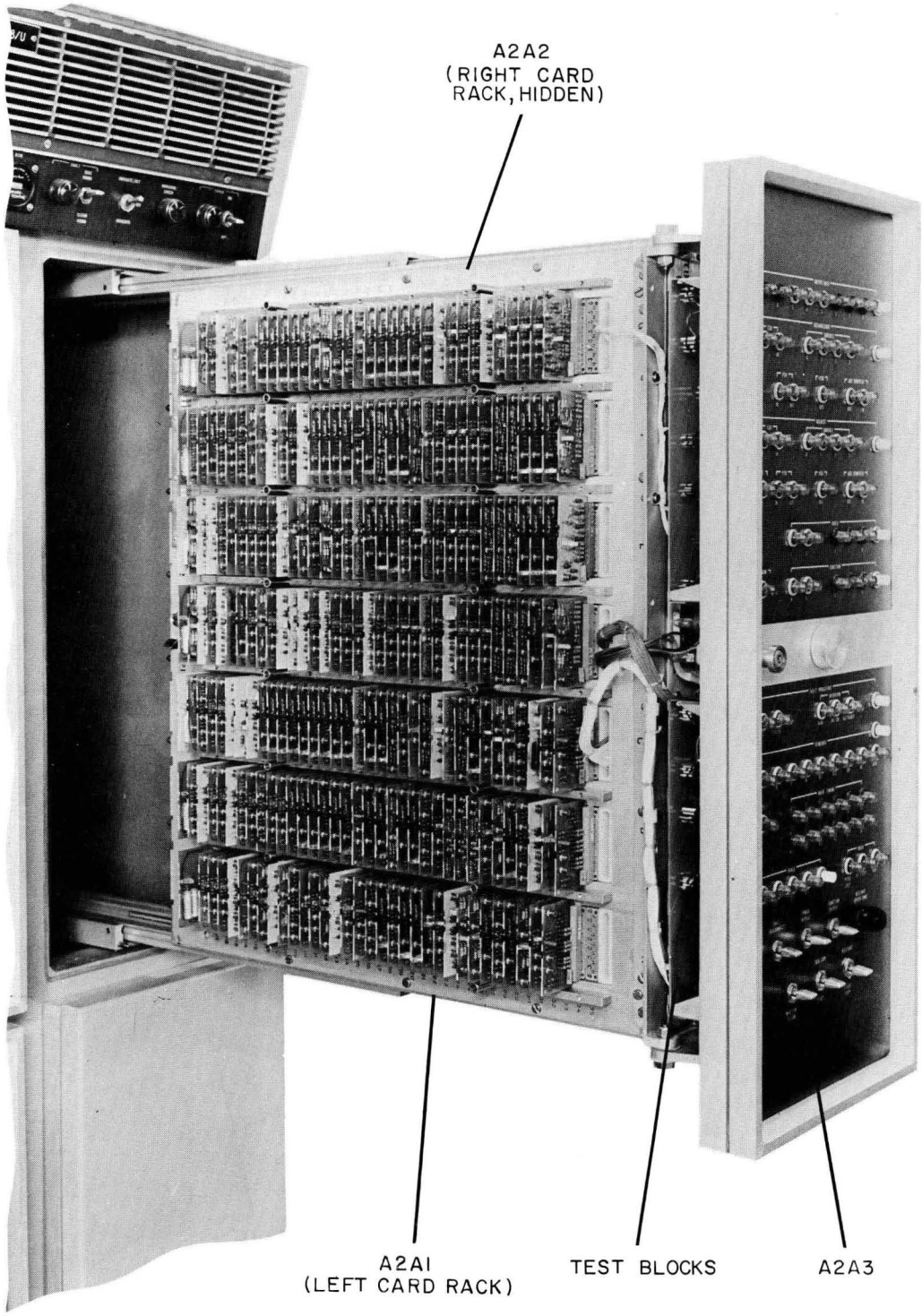


Figure 1-5. Logic Drawer A2

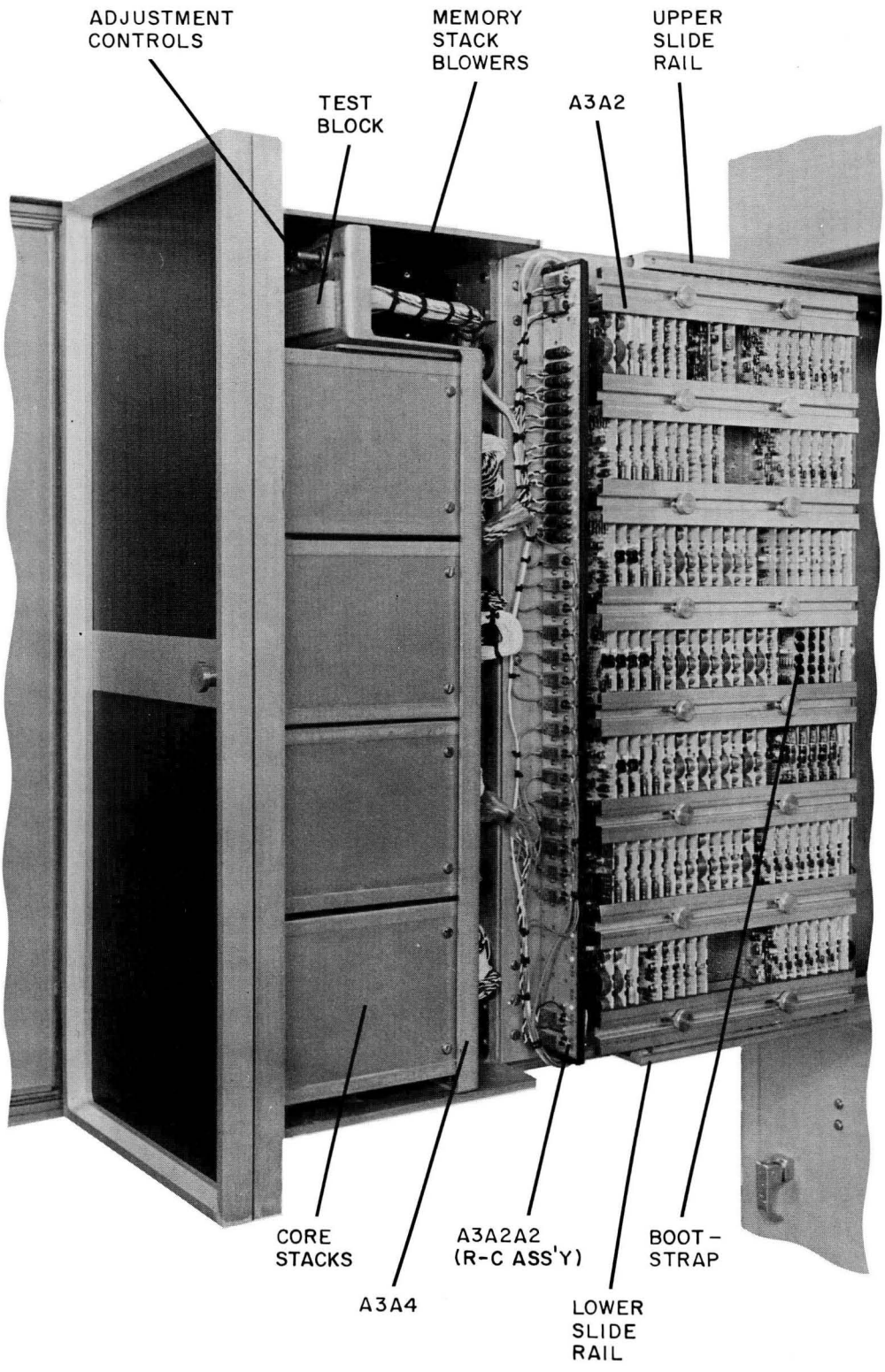


Figure 1-6. Memory Drawer A3

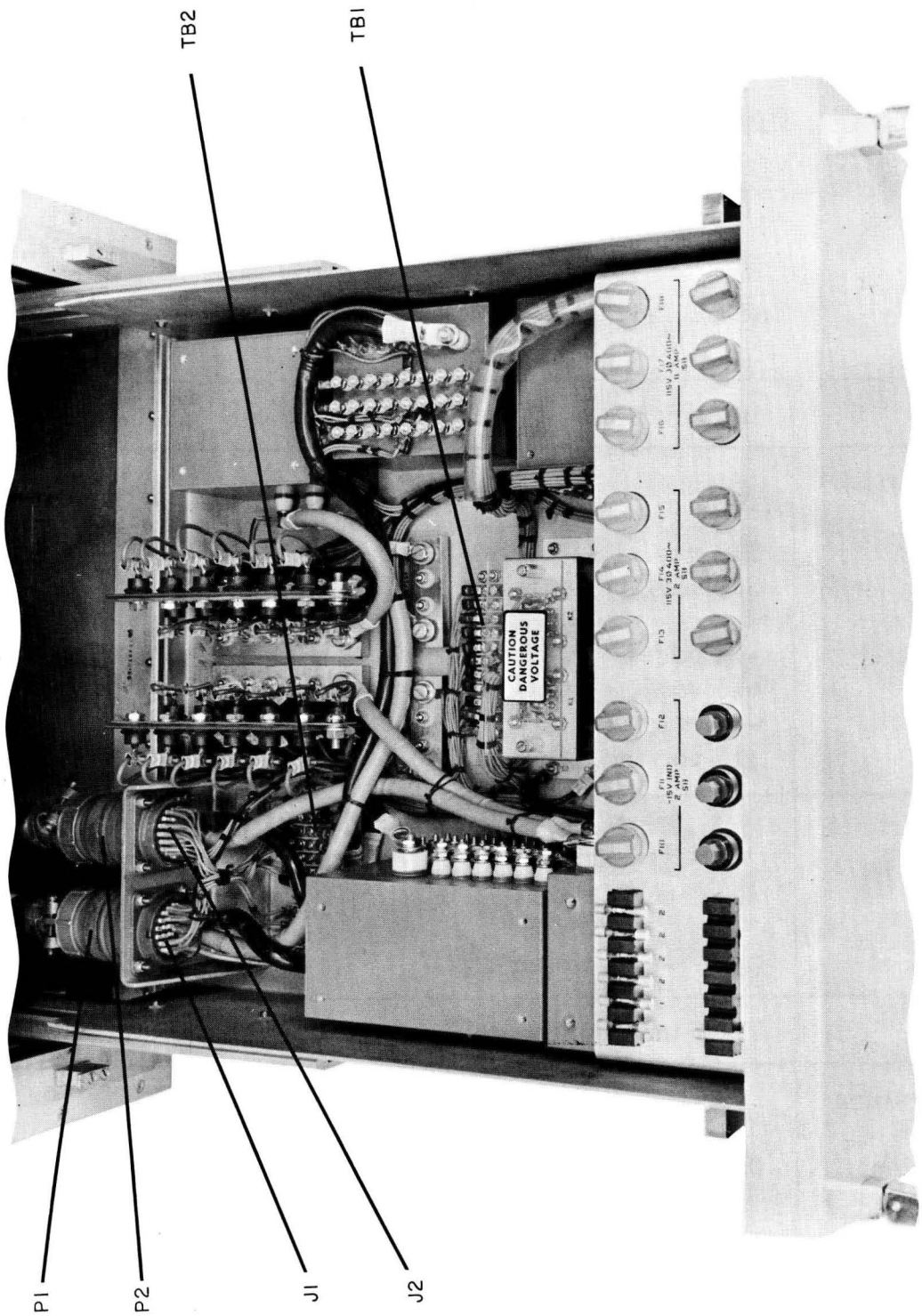


Figure 1-7. Power Supply PS1

1-6. INSTRUCTION REPERTOIRE. - Table 1-2, page 1-11, lists the computer instruction repertoire. The sequences are explained in paragraph 4-16c, page 4-44.

1-7. ASSIGNED MEMORY ADDRESSES. - Table 1-3, page 1-15, lists the reserved memory addresses. All listed addresses except bootstrap (00060 to 00077) are in core memory.

TABLE 1-1. Technical Characteristics

Item	Information	
Power		
AC Input	115 vac ±1% (line-to-line), 400 (-30, +21) Hz, 3-phase, 8 amperes per phase, 1500 watts	
Logic	-15 vdc +15 vdc -4.5 vdc +15 vdc indicator supply	
Signal Levels	Internal	I/O Lines
High	Grd (logic 0)	Grd (logic 1)
Low	-4.5v (logic 1)	-6v (logic 0)
Cooling	Four intake blowers, filtered input at 300 cfm	
Temperature		
Ambient	0°C (32°F) to 50°C (122°F)	
Alarm	46°C (115°F)	
Cutoff	60°C (140°F)	

TABLE 1-1. Technical Characteristics (continued)

Item	Information
Timing	
Cycle time	670 ±34 nanoseconds
Phase pulse	
Normal	120 nanoseconds minimum at -2v amplitude point. No pulse overlap at -1v amplitude point. (Refer to figure 4-12, page 4-38).
Narrow	80 to 100 nanoseconds at -2v amplitude point. No pulse overlap at -1v amplitude point.

TABLE 1-2. Repertoire of Instructions

Func. Code	Mnem.	Operation	Sequences	Execution Time in μsec	Instr. Format
00 11	HLT	Halt	I	4	VII
37	HLD	Stop	I	4	VII
01	LGN	Logical Negation	I	4	VII
02	TRF	Transfer on Flip-Flop	I	4	IV
03	TSR	Transfer to Subroutine	I, W	8	IV
04	TRX	Transfer on Index	I, R, (W)	8**	IV

( ) - Sequence is executed only if appropriate conditions exist
** - Add 4 μsec if transfer is executed

TABLE 1-2. Repertoire of Instructions (continued)

Func. Code	Mnem.	Operation	Sequences	Execution Time in μsec	Instr. Format
05	TAX	Transfer and Augment Index	I, R, (W)	8**	IV
06	SHF	Shift			II
06-0	SHL	Shift Left (Non-RCA)	I, (R), (W)	4 per seq	
		Shift Left (RCA)	I, (R), (RC1), (RC2), (WC), (R/W), (W)	+2/3 per shift	
	SCD/N	Shift Left Type 00	D indicates decrement mode; N indicates non-decrement mode		
	SAD/N	Shift Left Type 01			
	SXD/N	Shift Left Type 10			
	SLD/N	Shift Left Type 11			
06-1	DIV	Divide	I, (M) R, W,	44*	
06-2	SCA	Scale Accumulator	I	4, +2/3 per shift	
06-3	SCL	Scale Index and Accumulator	I, R, (W)	4 per seq. +2/3 per shift	
06-4	SHR	Shift Right	I, (R), (W)		
	SCR	Shift Right Type 00			
	SAR	Shift Right Type 01			

( ) - Sequence is executed only if appropriate conditions exist
* - Add 4 μsec if indexing (Core) occurs
** - Add 4 μsec if transfer is executed

TABLE 1-2. Repertoire of Instructions (continued)

Func. Code	Mnem.	Operation	Sequences	Execution Time in μsec	Instr. Format
	SXR	Shift Right Type 10			
	SLR	Shift Right Type 11			
06-5	MUL	Multiply	I, R, W	44	
06-6	SUD	Shift Until Different	I, R, (RC1), (RC2), (WC), (R/W), (W)	4 per seq +1-1/3 per shift	
07	EXF	External Function	I, R	8	VI
10	CLR	Clear Memory Address Y	I, (M), W	8*	I
12	STR	Store A	I, (M), W	8*	I
13	RPA	Replace Address	I, (M), W	8*	I
14	TRU	Transfer Unconditional	I, (M)	4*	I
15	TRA	Transfer on Accumulator	I, (M)	4*	I
16	TRD	Transfer if Different	I, (M)	4*	I
17	SWC	Sense Word Count	I, (M), R	8*	V
20	EXC	Exchange	I, (M), R, W	12*	I
21	ADC	Add Constant to Memory	I, R, W	12	VIII

( ) - Sequence is executed only if appropriate conditions exist
* - Add 4 μsec if indexing (Core) occurs

TABLE 1-2. Repertoire of Instructions (continued)

Fun. Code	Mnem.	Operation	Sequences	Execution Time in μsec	Instr. Format
22	ADO	Add One to Memory	I, (M), R, W	12*	I
23	AID	Add One if Different	I, (M), (R, W)	4/12*	I
24	RCA	Repeat Clear Add	I, (M), R, W	12*	I
25	ERC	End Repeat Count	I, (M), R, W	12*	I
26	STX/ SCR	Store Index/Store Repeat Count	I, (M), R, W	12*/8*	III
27	LDX/ LRC	Load Index/Load Repeat Count	I, (M), R, (W)	12*/8*	III
30	CLA	Clear Add	I, (M), R	8*	I
31	ADD	Add	I, (M), R	8*	I
32	SUB	Subtract	I, (M), R	8*	I
33	COM	Compare	I, (M), R	8*	I
34	LGA	Logical Add	I, (M), R	8*	I
35	LGM	Logical Multiply	I, (M), R	8*	I
36	ADB	Add B to A	I	4	VII

( ) - Sequence is executed only if appropriate conditions exist
* - Add 4 μsec if indexing (Core) occurs

TABLE 1-3. Assigned Memory Addresses

Octal Address	Content	Function
00001 - 00036	B Index #1 - B Index #36	
00037	B Index #37 and B Box	
00040 - 00041	Control Words #1 and #2	Repeat Clear Add or shift until tally, and jump address on the return jump
00042 - 00043	Control Words #1 and #2	Time Base Interrupt
00044 - 00045	Control Words #1 and #2	Auxiliary Computer Input
00046 - 00047	Control Words #1 and #2	Auxiliary Computer Output
00050 - 00051	Control Words #1 and #2	RD-277A Input (PTU Reader)
00052 - 00053	Control Words #1 and #2	RD-277A Output (PTU Punch)
00054 - 00055	Control Words #1 and #2	TCU Input
00056 - 00057	Control Words #1 and #2	TCU Output
00060 - 00067	Paper Tape Bootstrap	
00070 - 00077	Magnetic Tape Bootstrap	
001XX	OA-7385A/GYK-9A(V) Control Word Addresses (Console 0)	
002XX	OA-7385A/GYK-9A(V) Control Word Addresses (Console 1)	
003XX	OA-7385A/GYK-9A(V) Control Word Addresses (Console 2)	

TABLE 1-3. Assigned Memory Addresses (continued)

Octal Address	Content	Function
004XX	OA-7385A/GYK-9A(V) Control Word Addresses (Console 3)	
NOTE: XX =	00 to 37 Data Inputs 40 & 41 Special Input 42 & 43 Switch Input 44 & 45 Keyboard Input 46 & 47 Time Statement Input	50 & 51 Printer Control 52 to 73 Monitor Printer 74 & 75 Indicator Output 76 & 77 Special Output
00500 - 00501	Control Words #1 and #2	PCU (Printer #0)
00502 - 00503	Control Words #1 and #2	PCU (Printer #1)
00504 - 00505	Control Words #1 and #2	PCU (Printer #2)
00506 - 00507	Control Words #1 and #2	PCU (Printer #3)
00510 - 00511	Control Words #1 and #2	PCU (Printer #4)
00512 - 00513	Control Words #1 and #2	PCU (Printer #5)
00514 - 00515	Control Words #1 and #2	PCU (Printer #6)
00516 - 00517	Control Words #1 and #2	PCU (Printer #7)
00520 - 00521	Control Words #1 and #2	PCU (Printer #10)
00522 - 00523	Control Words #1 and #2	PCU (Printer #11)
00524 - 00525	Control Words #1 and #2	PCU (Printer #12)
00526 - 00527	Control Words #1 and #2	PCU (Printer #13)
00530 - 00531	Control Words #1 and #2	PCU (Printer #14)
00532 - 00533	Control Words #1 and #2	PCU (Printer #15)

TABLE 1-3. Assigned Memory Addresses (continued)

Octal Address	Content	Function
00534 - 00535	Control Words #1 and #2	PCU (Printer #16)
00536 - 00537	Control Words #1 and #2	PCU (Printer #17)
00540 - 00541	Control Words #1 and #2	PCU (Printer #20)
00542 - 00543	Control Words #1 and #2	PCU (Printer #21)
00544 - 00545	Control Words #1 and #2	PCU (Printer #22)
00546 - 00547	Control Words #1 and #2	PCU (Printer #23)
00550 - 00551	Control Words #1 and #2	PCU (Printer #24)
00552 - 00553	Control Words #1 and #2	PCU (Printer #25)
00554 - 00555	Control Words #1 and #2	PCU (Printer #26)
00556 - 00557	Control Words #1 and #2	PCU (Printer #27)
00560 - 00561	Control Words #1 and #2	PCU (Printer #30)
00562 - 00563	Control Words #1 and #2	PCU (Printer #31)
00564 - 00565	Control Words #1 and #2	PCU (Printer #32)
00566 - 00567	Control Words #1 and #2	PCU (Printer #33)
00570 - 00571	Control Words #1 and #2	PCU (Printer #34)
00572 - 00573	Control Words #1 and #2	PCU (Printer #35)
00574 - 00575	Control Words #1 and #2	PCU (Printer #36)
00576 - 00577	Control Words #1 and #2	PCU (Printer #37)
00600 - 00601	Control Words #1 and #2	PCU (Printer #40)

TABLE 1-3. Assigned Memory Addresses (continued)

Octal Address	Content	Function
00602 - 00603	Control Words #1 and #2	PCU (Printer #41)
00604 - 00605	Control Words #1 and #2	PCU (Printer #42)
00606 - 00607	Control Words #1 and #2	PCU (Printer #43)
00610 - 00611	Control Words #1 and #2	PCU (Printer #44)
00612 - 00613	Control Words #1 and #2	PCU (Printer #45)
00614 - 00615	Control Words #1 and #2	PCU (Printer #46)
00616 - 00617	Control Words #1 and #2	PCU (Printer #47)
00620 - 00621	Control Words #1 and #2	(Printer #50)
00622 - 00623	Control Words #1 and #2	(Printer #51)
00624 - 00625	Control Words #1 and #2	(Printer #52)
00626 - 00627	Control Words #1 and #2	(Printer #53)
00630 - 00631	Control Words #1 and #2	(Printer #54)
00632 - 00633	Control Words #1 and #2	(Printer #55)
00634 - 00635	Control Words #1 and #2	(Printer #56)
00636 - 00637	Control Words #1 and #2	(Printer #57)
00640 - 00641	Control Words #1 and #2	(Printer #60)
00642 - 00643	Control Words #1 and #2	(Printer #61)
00644 - 00645	Control Words #1 and #2	(Printer #62)
00646 - 00647	Control Words #1 and #2	(Printer #63)

TABLE 1-3. Assigned Memory Addresses (continued)

Octal Address	Content	Function
00650 - 00651	Control Words #1 and #2	(Printer #64)
00652 - 00653	Control Words #1 and #2	(Printer #65)
00654 - 00655	Control Words #1 and #2	(Printer #66)
00656 - 00657	Control Words #1 and #2	(Printer #67)
00660 - 00661	Control Words #1 and #2	(Printer #70)
00662 - 00663	Control Words #1 and #2	(Printer #71)
00664 - 00665	Control Words #1 and #2	(Printer #72)
00666 - 00667	Control Words #1 and #2	(Printer #73)
00670 - 00671	Control Words #1 and #2	(Printer #74)
00672 - 00673	Control Words #1 and #2	(Printer #75)
00674 - 00675	Control Words #1 and #2	(Printer #76)
00676 - 00677	Control Words #1 and #2	(Printer #77)
37600 - 37776		Bootstrap Load

CHAPTER 2

INSTALLATION

I - INSTALLATION PROCEDURES

2-1. SITE SELECTION. - Available site facilities govern placement of the equipment. Select a site which protects the equipment, is free of excessive dust, provides proper heat dissipation, and allows adequate space for maintenance and airflow. Figure 2-1, page 2-2, shows minimum clearances required.

2-2. INSPECTION. - No elaborate unpacking procedure is necessary as the computer arrives completely assembled. After unpacking the computer, complete the following inspection procedure.

1. Check cabinet for dents, scratches, and bent or broken parts.

2. Extend each drawer and note any binding.

3. Check each drawer for damaged parts.

4. As each drawer is extended check cabinet interior for damaged parts.

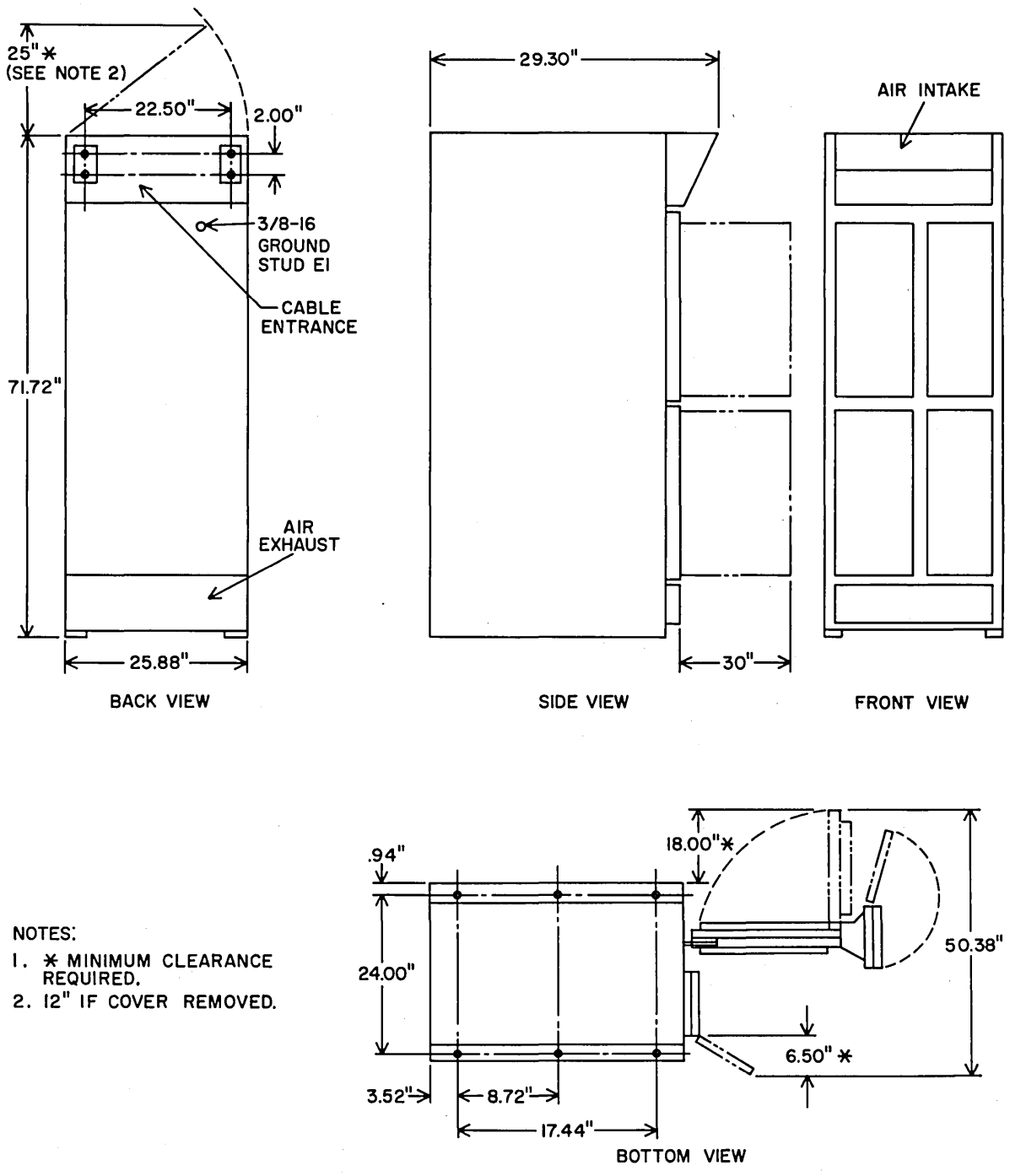
5. Rotate all fan blades and note any binding.

6. Close each drawer and note any binding.

7. Notify supervisory personnel immediately of any damage noted in steps 1 through 6.

Note: - Damage shall be reported according to the regulations of the service having jurisdiction over the damaged equipment.

2-3. MOUNTING. - Bolt the computer to the floor or to a base plate welded to the floor and bolt the stabilizers to the wall. This is necessary to prevent forward overbalance when several logic drawers are opened. Figure 2-1, page 2-2, shows the required mounting dimensions. To bolt equipment to floor or base plate and stabilizers, complete the following steps.



NOTES:

1. * MINIMUM CLEARANCE REQUIRED.
2. 12" IF COVER REMOVED.

Figure 2-1. CP-818A/U Dimensional Data

1. Remove power supply drawer PS1.

2. Position equipment.

3. Align all bolt holes (base and stabilizers).

4. Insert and tighten all bolts.

5. Replace power supply drawer PS1.

The computer is shipped with the top cover removed. Prior to operation install the cover to insure RFI integrity and drip proofing. To install the cover complete the following procedure.

1. Remove six cover-hinge mounting screws and two folding-stay mounting screws from the computer.

2. Attach cover with six mounting screws.

3. Attach folding stay.

4. Ensure that lifting eyes or plugs are installed for RFI integrity.

Note: - If top cover is not installed, all mounting screws must be in place to insure RFI integrity.

2-4. CABLING CONNECTIONS. - All cable connectors are at the top rear of the computer (see figure 2-1, page 2-2). Table 2-1, page 2-4, lists all required cables and connectors.

a. Power. - The four-conductor power cable connects to a set of high frequency line filters, FL1, FL2, and FL3, and a common ground. To connect the power cable complete the following procedure.

WARNING

BEFORE ATTEMPTING TO CONNECT POWER CABLE TO COMPUTER, ENSURE OTHER END OF CABLE IS DISCONNECTED OR EXTERNAL POWER SOURCE IS DE-ENERGIZED AND TAGGED.

TABLE 2-1. Cables and Connectors

Jack No.	External Device	Connector Type	Connectors
J1	Power	MS3106A20-15S	4
J2	TCU	Cannon DPD 4500-5207	50
J3	PCU	Cannon DPD 4500-5207	50
J4	RD-277A (PTU)	Cannon DPD 4500-5207	50
J5(J10)	AUX CMPTR	Cannon DPD 4500-5207	50
J6	CSL 0	Cannon DPD 4500-5207	50
J7	CSL 1	Cannon DPD 4500-5207	50
J8	CSL 2	Cannon DPD 4500-5207	50
J9	CSL 3	Cannon DPD 4500-5207	50

1. Remove J1 cover.

2. Seat plug P1.

3. Tighten retainer ring.

b. Ground. - The dc level input/output communication used in the system makes the cabinet grounding system extremely important. All internal grounds and cable returns connect to a common ground bus. To connect the computer to the system ground, complete the following procedure.

1. Remove nut from E1 ground stud on the back of computer (figure 2-1, page 2-2).

2. Connect system ground lead to stud.

3. Replace and tighten nut.

c. Signal. - All input/output signal connectors are 50-pin connectors mounted on the top of the cabinet (figure 2-2). Table 2-2, page 2-6, lists the peripheral equipment that connects to each jack and the signal assigned to each pin. Because of the cable drivers in the computer, cable length must not exceed 150 feet.

CAUTION. - Connect only one auxiliary computer cable. An auxiliary-computer cable connected to J5 of the CP-818A/U must connect to J10 of the auxiliary computer or a cable connected to J10 of the CP-818A/U must connect to J5 of the auxiliary computer.

To connect a signal cable, complete the following procedure.

1. Locate proper jack number.
2. Swing retainer strap forward.
3. Insert plug.
4. Push down to seat properly.

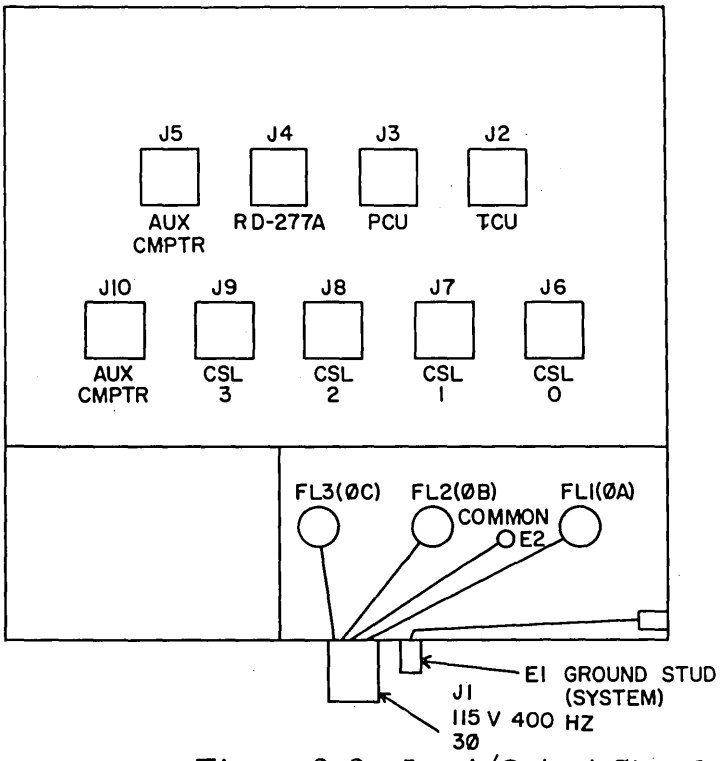


Figure 2-2. Input/Output Signal Connectors

TABLE 2-2. CP-818A/U Connector Pin Number Assignments

Connector Pin No.	J2 (TCU)	J3 (PCU)	J4 (RD-277A)	Console 0-J6 Console 1-J7 Console 2-J8 Console 3-J9	Auxiliary Computer	
					J5	J10 Pin No.
1	Out Data 2^0 r	Out Data 2^0 r	Out Data 2^0 r	Out Data 2^0 r	Out Data 2^0 r	25
2	Out Data 2^1 r	Out Data 2^1 r	Out Data 2^1 r	Out Data 2^1 r	Out Data 2^1 r	44
3	Out Data 2^2 r	Out Data 2^2 r	Out Data 2^2 r	Out Data 2^2 r	Out Data 2^2 r	45
4	Out Data 2^3 r	Out Data 2^3 r	Out Data 2^3 r	Out Data 2^3 r	Out Data 2^3 r	46
5	Out Data 2^4 r	Out Data 2^4 r	Out Data 2^4 r	Out Data 2^4 r	Out Data 2^4 r	47
6	Out Data 2^5 r	Out Data 2^5 r	Out Data 2^5 r	Out Data 2^5 r	Out Data 2^5 r	48
7	Out Data 2^6 r	Out Data 2^6 r	Out Data 2^6 r	Out Data 2^6 r	Out Data 2^6 r	49
8	Out Data 2^7 r	Out Data 2^7 r	Out Data 2^7 r	Out Data 2^7 r	Out Data 2^7 r	31
9	Out Data 2^0	Out Data 2^0	Out Data 2^0	Out Data 2^0	Out Data 2^0	34
10	Out Data 2^1	Out Data 2^1	Out Data 2^1	Out Data 2^1	Out Data 2^1	35
11	Out Data 2^2	Out Data 2^2	Out Data 2^2	Out Data 2^2	Out Data 2^2	36

*r = return line

TABLE 2-2. CP-818A/U Connector Pin Number Assignments (continued)

Connector Pin No.	J2 (TCU)	J3 (PCU)	J4 (RD-277A)	Console 0-J6 Console 1-J7 Console 2-J8 Console 3-J9	Auxiliary Computer	
					J5	J10 Pin No.
12	Out Data 2^3	Out Data 2^3	Out Data 2^3	Out Data 2^3	Out Data 2^3	37
13	Out Data 2^4	Out Data 2^4	Out Data 2^4	Out Data 2^4	Out Data 2^4	38
14	Out Data 2^5	Out Data 2^5	Out Data 2^5	Out Data 2^5	Out Data 2^5	39
15	Out Data 2^6	Out Data 2^6	Out Data 2^6	Out Data 2^6	Out Data 2^6	40
16	Out Data 2^7	Out Data 2^7	Out Data 2^7	Out Data 2^7	Out Data 2^7	22
17	Tape Mark	In Address 2^1	Lockout FF	In Address 2^1	A.C. In Busy	18
18	Tape Busy	In Address 2^2	Ext. Function	In Address 2^2	Out Busy	17
19	Data Transfer Error	In Address 2^3	Input Active	In Address 2^3	Spare	20
20	Transport Ready	In Address 2^4	Spare	In Address 2^4	Spare	19
21	Out Request	In Address 2^5	Out Request	In Address 2^5	Out Request	43

*r = return line

TABLE 2-2. CP-818A/U Connector Pin Number Assignments (continued)

Connector Pin No.	J2 (TCU)	J3 (PCU)	J4 (RD-277A)	Console 0-J6 Console 1-J7 Console 2-J8 Console 3-J9	Auxiliary Computer	
					J5	J10 Pin No.
22	Select Error	In Address 2^6	In Data 2^7	In Data 2^7	In Data 2^7	16
23	Out Ack	Spare	Out Ack	Computer Run	Out Ack	24
24	In Request	Request	In Request	Request	In Request	23
25	In Data 2^0 r	Spare r (34)	In Data 2^0 r	In Data 2^0 r	In Data 2^0 r	1
26	Tape Mark r	In Address 2^1 r	Lockout FF r	In Address 2^1 r	A.C. In Busy	27
27	Tape Busy r	In Address 2^2 r	Ext. Funct. r	In Address 2^2 r	Out Busy r	26
28	Data Transfer Error r	In Address 2^3 r	In. Active r	In Address 2^3 r	Spare r (19)	29
29	Transport Ready r	In Address 2^4 r	Spare r (20)	In Address 2^4 r	Spare r (20)	28
30	Out Request r	In Address 2^5 r	Out Request	In Address 2^5 r	Out Request r	42
31	Select Error r	In Address 2^6 r	In Data 2^7 r	In Data 2^7 r	In Data 2^7 r	8
32	Out Ack r	Spare r (23)	Out Ack r	Computer Fault	Out Ack r	33

*r = return line

TABLE 2-2. CP-818A/U Connector Pin Number Assignments (continued)

Connector Pin No.	J2 (TCU)	J3 (PCU)	J4 (RD-277A)	Console 0-J6 Console 1-J7 Console 2-J8 Console 3-J9	Auxiliary Computer	
					J5	J10 Pin No.
33	In Request r	Request r	In Request r	Request r	In Request r	32
34	In Data 2^0	Spare	In Data 2^0	In Data 2^0	In Data 2^0	9
35	In Data 2^1	Spare	In Data 2^1	In Data 2^1	In Data 2^1	10
36	In Data 2^2	Spare	In Data 2^2	In Data 2^2	In Data 2^2	11
37	In Data 2^3	Spare	In Data 2^3	In Data 2^3	In Data 2^3	12
38	In Data 2^4	Spare	In Data 2^4	In Data 2^4	In Data 2^4	13
39	In Data 2^5	Spare	In Data 2^5	In Data 2^5	In Data 2^5	14
40	Spare	Spare	In Data 2^6	In Data 2^6	In Data 2^6	15
41	Spare	Spare	Spare	Parallel Data	Spare	41
42	In Ack r	Ack r	In Ack r	Ack r	In Ack r	30
43	In Ack	Ack	In Ack	Ack	In Ack	21
44	In Data 2^1 r	Spare r (35)	In Data 2^1 r	In Data 2^1 r	In Data 2^1 r	2

*r = return line

TABLE 2-2. CP-818A/U Connector Pin Number Assignments (continued)

Connector Pin No.	J2 (TCU)	J3 (PCU)	J4 (RD-277A)	Console 0-J6 Console 1-J7 Console 2-J8 Console 3-J9	Auxiliary Computer	
					J5	J10 Pin No.
45	In Data 2^2 r	Spare r (36)	In Data 2^2 r	In Data 2^2 r	In Data 2^2 r	3
46	In Data 2^3 r	Spare r (37)	In Data 2^3 r	In Data 2^3 r	In Data 2^3 r	4
47	In Data 2^4 r	Spare r (38)	In Data 2^4 r	In Data 2^4 r	In Data 2^4 r	5
48	In Data 2^5 r	Spare r (39)	In Data 2^5 r	In Data 2^5 r	In Data 2^5 r	6
49	Spare r (40)	Spare r (41)	In Data 2^6 r	In Data 2^6 r	In Data 2^6 r	7
50	Shield & Spare r (41)	Shield & Spare r (41)	Shield & Spare r (41)	Shield & Parallel Data r	Shield & Spare r (41)	50

*r = return line

5. Raise retainer strap over top of plug.

6. Tighten screw in retainer strap.

II - ADJUSTMENTS

2-5. POWER. - The dc voltage supplies are factory adjusted for the correct output with a 115 vac input. Check the output voltages and fuses of each supply as shown in table 2-3.

TABLE 2-3. DC Voltage Check Points

Voltage (±5%)	Test Point*		Fuses	
	Number	Color	Number	Rating
+15v	TB1-A4	Red	F7, 8, 9	2ASB
-4.5v	TB1-A3	Yellow	F1, 2, 3	1ASB
-15v	TB1-A2	Violet	F4, 5, 6	3ASB
Ground	TB1-A1	Black	Black	
+15v indicator	TB2-G23		F10, 11, 12	2ASB
+15v indicator grd	TB2-G01			

* Chassis A1A1

If the output of a dc supply (+15v, -15v, or -4.5v) is not within the specified tolerance, adjust the taps on the primary side of the supply transformer.

III - REPACKING AND STORAGE

2-6. REPACKING. - To prepare the CP-818A/U for shipment or storage, complete the following procedure.

1. Clear core memory to all zeros or all ones.

2. De-energize and tag main power switch.

3. Disconnect main power cable at J1.

4. Disconnect system ground cable at stud E1.

5. Disconnect all input/output signal cables.

6. Open all chassis.

7. Tighten card hold-down straps.

8. Close all chassis.

9. Ensure all chassis locking screws are tight.

10. Remove mounting bolts.

The CP-818A/U is now ready for repacking. The type of crate and amount of repacking depend on the materials available and the equipment destination. However, the packaging used must protect the computer from dust, moisture, and vibration.

2-7. STORAGE. - To prepare the CP-818A/U for storage complete the procedure in paragraph 2-6, page 2-11. The crate or covering used must protect the computer from dust, moisture, and damage. The storage site temperature must be maintained between -40°C (-40°F) and 60°C (140°F). The relative humidity must not exceed 95%.

CHAPTER 3

OPERATING INSTRUCTIONS

I - CONTROLS AND INDICATORS

3-1. OPERATOR CONTROLS AND INDICATORS. - Operator controls and indicators and all maintenance controls and indicators (except master clock margin and memory adjustment controls) are on the power control panel, logic panel A1A3, and logic panel A2A3. Many of these controls are indicator-switches which connect to control flip-flops and register flip-flops. The indicator portion of the indicator-switch is lighted when the associated flip-flop sets. Pressing an indicator-switch sets the associated flip-flop and lights the indicator. Some groups of indicator-switches have an associated clear push-switch. Pressing this switch clears all flip-flops in the group.

a. Power Control Panel (figure 3-1, page 3-2). - Table 3-1 lists the switches and indicators on this panel and describes their function.

b. Logic Panel A1A3 (figure 3-2, page 3-6). - Table 3-2, page 3-5, lists the indicator-switches on this panel and describes their function.

c. Logic Panel A2A3 (figure 3-3, page 3-9). - Table 3-3, page 3-9, lists the indicator-switches and controls on this panel and describe their function.

d. Console Input Bit Switch (figure 3-4, page 3-17). - The console bit selection switch, located behind logic panel A2, selects either 6-bit mode or 8-bit mode when the console specifies parallel inputs.

TABLE 3-1. Power Control Panel Controls and Indicators

Control or Indicator	Type	Function
OVER TEMP	Indicator (red)	Lights when cabinet interior temperature exceeds 46°C (115°F).

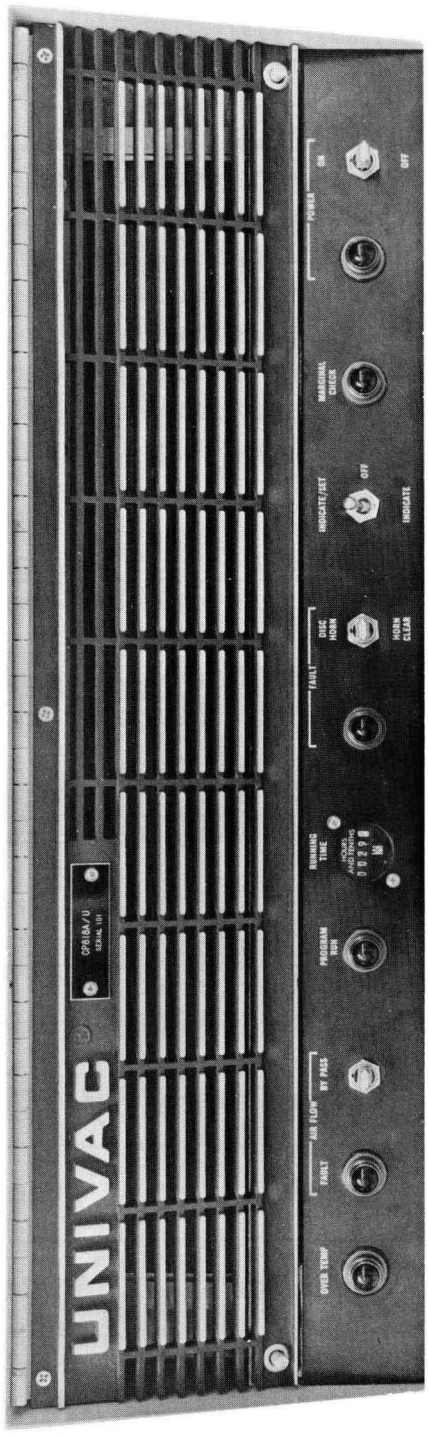


Figure 3-1. Power Control Panel

TABLE 3-1. Power Control Panel Controls and Indicators (continued)

Control or Indicator	Type	Function
AIR FLOW FAULT	Indicator (red)	Lights if cabinet airflow stops with power on (air leak, extended chassis, or a blower not operating).
BYPASS	Toggle switch	Enables dc power to be applied to the computer immediately; bypassing 30-second initial delay. Also, enables dc power to be applied to computer even though there is not sufficient airflow within cabinet to close internal airflow switch.
PROGRAM RUN	Indicator (green)	Lights when computer is operating in high-speed run mode.
RTM	Real time meter	Records time that computer dc power is on. The meter cycles from 0 through 9999.9 hours. It cannot be reset.
FAULT	Indicator (red)	Lights when one of the following logic fault conditions occurs: 1) Parity error 2) Halt (function code error) 3) Console data input overflow 4) Console switch input overflow 5) Console keyboard input overflow

TABLE 3-1. Power Control Panel Controls and Indicators (continued)

Control or Indicator	Type	Function
FAULT DISC HORN/HORN CLEAR	Toggle switch (three-position)	Center position: Horn sounds when fault occurs. HORN CLEAR: Silences horn if sounding. Horn will sound again for a different fault or when present fault is removed and occurs again. DISC HORN: Prevents horn from sounding when a fault occurs.
INDICATE/SET-OFF-INDICATE	Toggle switch (three-position)	OFF: Disables all indicator-switches on both logic panels. INDICATE: Indicator-switches indicate flip-flop states but cannot set flip-flops. INDICATE/SET: Indicator-switches indicate flip-flop states and can set flip-flops.
MARGINAL CHECK	Indicator (red)	Lights when marginal check switch on either memory chassis is in HIGH or LOW position, or when either CLOCK NARROW/NORMAL switch behind logic panel A1 is in NARROW position.
POWER	Indicator (green)	Lights when ac power is applied to the computer (POWER ON/OFF switch placed to ON position).

TABLE 3-1. Power Control Panel Controls and Indicators (continued)

Control or Indicator	Type	Function
POWER ON/OFF	Toggle switch (two-position)	ON: Applies ac power to the blowers. Thirty seconds later (when rated air flow is reached) dc power is applied to the computer logic. OFF: Removes ac and dc power from the computer logic.

TABLE 3-2. Logic Panel A1A3, Control and Indicators

Indicator-Switch	Function
A-register 00-23	Indicate the state of each bit in the A-register and enable the operator to alter the register contents. The A-register is the arithmetic section accumulator. It holds the result of an add or subtract operation; the multiplier and the least significant product bits of a multiply operation, the least significant dividend bits and the quotient of a divide operation, and the mask for a logical operation and is used in shifting and complementing operations.
D-register 00-23	Indicate the state of each bit in the D-register and enable the operator to alter the register contents. The D-register is an arithmetic section operand register. It holds one operand during arithmetic and logical operations.
X-register 00-23	Indicate the state of each bit in the X-register and enable the operator to alter the register contents. The X-register is the arithmetic section exchange register. It holds one of the operands during an arithmetic or logic operation and has a direct data path to the Z and D registers and the adder.

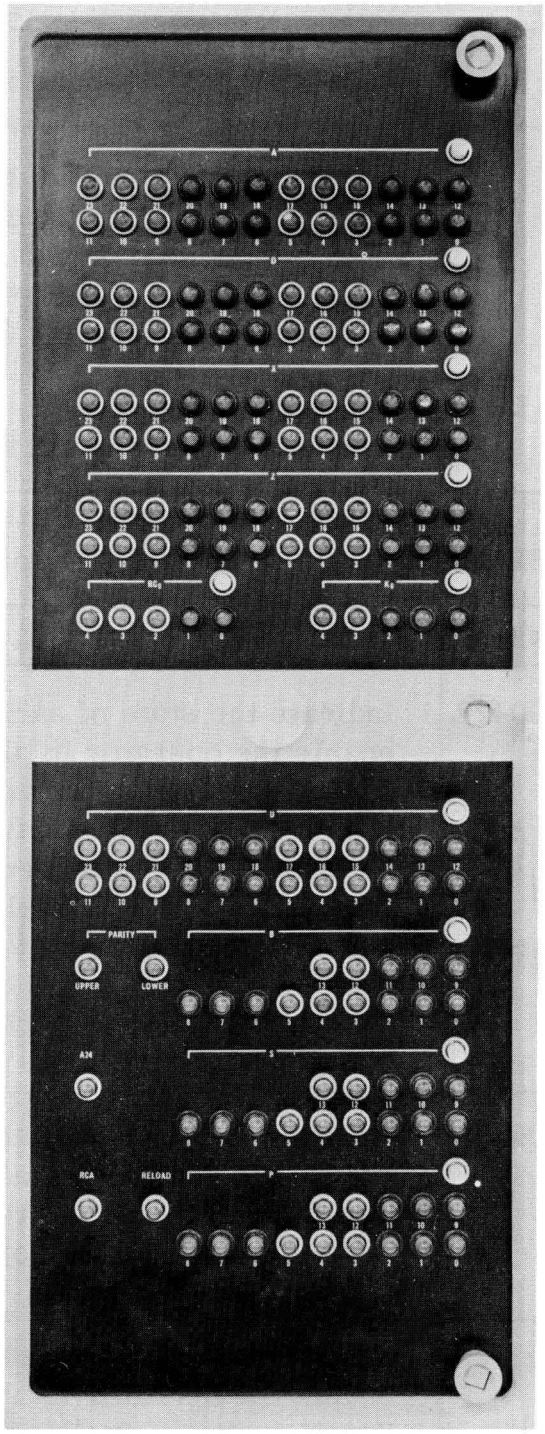


Figure 3-2. Logic Panel A1A3

TABLE 3-2. Logic Panel A1A3, Control and Indicators (continued)

Indicator-Switch	Function
Z-register 00-23	Indicate the state of each bit in the Z-register and enable the operator to alter the register contents. The Z-register is the memory input/output buffer register. It routes memory data to the F, M, K, C, X, and RC-registers and serves as the selector input register for writing data into memory.
U-register 00-23	Indicate the state of each bit in the U-register and enable the operator to alter the register contents. The U-register serves as the lower rank for the A-register during shifting operations.
B-register 00-13	Indicate the state of each bit in the B-register and enable the operator to alter the register contents. The B-register is associated with index 37 in memory and normally contains the 14-bit address field of index 37. However, it can be used to modify an instruction without using the memory.
S-register 00-13	Indicate the state of each bit in the S-register and enable the operator to alter the register contents. The S-register is the memory address register and holds the addresses to control the memory address translator during the memory cycle.
P-register 00-13	Indicate the state of each bit in the P-register and enable the operator to alter the register contents. The P-register is the program address register. It holds the address of the next instruction while the current instruction is being performed. It is incremented by the arithmetic section or reloaded with a new address (skip condition).
RC_0 0 - 4	Display count in double-rank repeat counter. Load index instruction (27) loads this register. Repeat counter is active during a shift instruction when instruction specifies RCA mode of shifting. Repeat counter decrements by one for each shift when proper mode is selected.

TABLE 3-2. Logic Pannel A1A3, Control and Indicators (continued)

Indicator-Switch	Function
K_0 0 - 4	Indicate number of shifts specified by shift (06) instruction. Register decrements by one as each shift is executed.
RCA	Lights when repeat-clear-add instruction (24) is executed and remains lighted until end-repeat-count instruction (25) is executed or until a buffer terminate or RC = 0 occurs.
RELOAD	Operates during RC1-sequence of the shift (06) instruction. Indicator is lighted after repeat counter reaches zero.
A24	Operates during a shift (06) instruction. Indicator is lighted during left shift operation when upper bit of A-register (A23) is a one and is extinguished when A23 is a zero. During right shift type 00, indicator is lighted when A00 is a one and is extinguished when A00 is a zero. During right shift type 10 or 11 operations, indicator is lighted when Z00 is a one and is extinguished when Z00 is a zero.
PARITY	
UPPER	Lights when upper half of a word read from memory (bits 12 through 23) contains an even number of one bits.
LOWER	Lights when lower half of a word read from memory (bits 1 through 11) contains an even number of one bits.

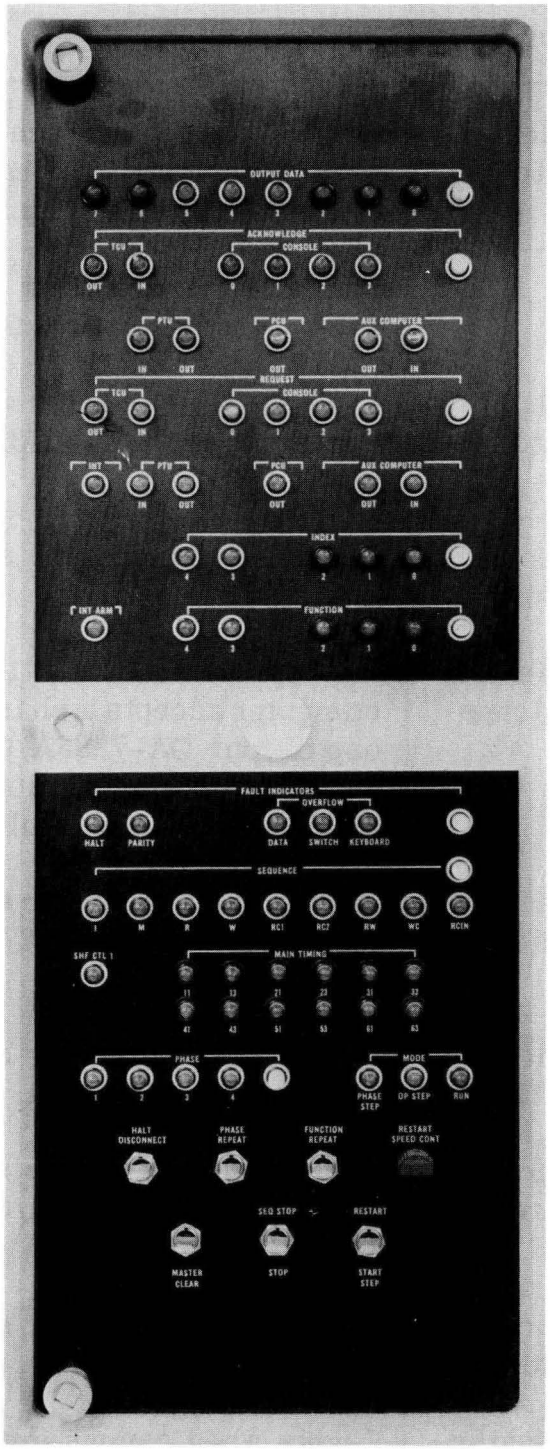


Figure 3-3. Logic Panel A2A3

TABLE 3-3. Logic Panel A2A3 Controls and Indicators

Control or Indicator	Type	Function
OUTPUT DATA 0 - 7 (C-register)	Indicator-switches	Display characters sent to peripheral equipments. Indicators clear just prior to reload.
ACKNOWLEDGE		Indicators do not clear until computer sends another acknowledge.
TCU IN	Indicator-switch	Lights when computer accepts a character from C-6573A/GYK-9A(V) (TCU).
TCU OUT	Indicator-switch	Lights when computer sends a character to TCU.
CONSOLE 0 - 3	Indicator-switches	Appropriate indicator lights when computer accepts a character from one of four OA-7385A/GYK-9A(V) consoles or when computer sends a character to a console.
PTU IN	Indicator-switch	Lights when computer accepts a character from RD-277A/GYK-9A(V) (PTU).
PTU OUT	Indicator-switch	Lights when computer sends a character to RD-277A.
PCU OUT	Indicator-switch	Lights when computer sends a character to C-6572A/GYK-9A(V) (PCU).
AUX COMPUTER OUT	Indicator-switch	Lights when computer sends a character to auxiliary computer.
AUX COMPUTER IN	Indicator-switch	Lights when computer accepts a character from auxiliary computer.

TABLE 3-3. Logic Panel A2A3 Controls and Indicators (continued)

Control or Indicator	Type	Function
REQUEST		
INT	Indicator-switch	Lights when an interrupt request is made by computer. Occurs once every millisecond while interrupt is armed.
TCU OUT	Indicator-switch	Lights when TCU requests a character from computer.
TCU IN	Indicator-switch	Lights when TCU has a character ready for computer.
CONSOLE 0 - 3	Indicator-switches	Lights when a console has a character ready for computer or when a console requests a character from computer.
PTU IN	Indicator-switch	Lights when RD-277A has a character ready for computer.
PTU OUT	Indicator-switch	Lights when RD-277A requests a character from computer.
PCU OUT	Indicator-switch	Lights when PCU requests a character from computer.
AUX COMPUTER OUT	Indicator-switch	Lights when auxiliary computer requests a character from computer.
AUX COMPUTER IN	Indicator-switch	Lights when auxiliary computer has a character ready for computer.

TABLE 3-3. Logic Panel A2A3 Controls and Indicators (continued)

Control or Indicator	Type	Function
INDEX 0 - 4 (M-register)	Indicator-switches	Display contents of M-register. M-register contains address of index register used for instruction address modification and also holds status check code during execution of 02 (TRF) instruction and the constant to be added during a 21 (ADC) instruction.
INT ARM	Indicator-switch	Lighted by an EXF (07) instruction with arm interrupt code. Extinguished by RCIN sequence of EXF instruction with disarm code.
FUNCTION 0 - 4 (F-register)	Indicator-switches	Display function code (octal) of instruction being executed.
FAULT INDICATORS		
HALT	Indicator-switch	Lights whenever a halt instruction (00, 11, 37) is executed if the HALT DISCONNECT switch is in the normal position. Computer operation stops.
PARITY	Indicator-switch	Lights whenever upper half or lower half of word read from memory contains an even number of one bits (including the parity bit). Computer operation stops.
OVERFLOW		
DATA	Indicator-switch	Lights when a console sends computer a data character and computer cannot accept character because of zero word count in assigned control words.

TABLE 3-3. Logic Panel A2A3 Controls and Indicators (continued)

Control or Indicator	Type	Function
SWITCH	Indicator-switch	Lights when a console sends computer a switch character and computer cannot accept character because of zero word count in assigned control word.
KEYBOARD	Indicator-switch	Lights when a console sends computer a keyboard character and computer cannot accept character because of zero word count in assigned control word.
SEQUENCE		
I	Indicator-switch	Lights during an I sequence (instruction is read from memory) and when computer is in master clear state.
M	Indicator-switch	Lights during an M sequence (instruction address is modified with contents of an index register or divisor read from memory during divide operation).
R	Indicator-switch	Lights during a read sequence (data read from memory).
W	Indicator-switch	Lights during a write sequence (data written into memory).
RC1	Indicator-switch	Lights during a read control word 1 sequence (first RCA, SUD shift, or I/O operation.

TABLE 3-3. Logic Panel A2A3 Controls and Indicators (continued)

Control or Indicator	Type	Function
RC2	Indicator-switch	Lights during a read control word 2 sequence (second RCA, SUD shift, or I/O operation).
R/W	Indicator-switch	Lights during a read/write sequence (data from a peripheral equipment written into memory or data for a peripheral equipment read from memory).
WC	Indicator-switch	Lights during a write control word sequence (RCA, SUD shift, or I/O operation).
RCIN	Indicator-switch	Lights during the RCIN-sequence of an interrupt instruction (TRU function code read from memory and jump address placed in P-register).
SHF CTL 1	Indicator-switch	Indicates status of shift control FF 1. This flip-flop is set during I, R, or R/W-sequence of any 06 instruction when conditions are satisfied to enable shift sequence to be performed.
MAIN TIMING 11, 13, 21, 23, 31, 33, 41, 43, 51, 53, 61, 63	Indicator-switches	Indicate status of 12 flip-flops which provide timing signals for computer operation.
PHASE 1 - 4	Indicator-switches	The PHASE 1 indicator-switch lights when the master clock generates the phase 1 clock pulse. The PHASE 4 indicator-switch lights when the master clock generates the phase 4 clock pulse.

TABLE 3-3. Logic Panel A2A3 Controls and Indicators (continued)

Control or Indicator	Type	Function
MODE		
PHASE STEP	Indicator-switch	Enables computer to operate in PHASE STEP mode.
OP STEP	Indicator-switch	Enables computer to operate in OP STEP mode.
RUN	Indicator-switch	Enables computer to operate in RUN mode.
HALT DISCONNECT	Toggle switch	Prevents a halt instruction (00, 11, 37) or parity error from stopping computer operation.
PHASE REPEAT	Toggle switch	Used in conjunction with the PHASE STEP MODE switch and individual phase indicators.
FUNCTION REPEAT	Toggle switch	Allows certain instructions to be continuously executed.
MASTER CLEAR	Toggle switch	Returns all computer circuits to their initial condition. This switch does not function while computer is operating in high-speed RUN mode.
SEQ STOP/STOP	Toggle switch	SEQ STOP: Causes computer to execute one sequence of current instruction when OP STEP mode is selected. Normal: Causes computer to execute one instruction when OP STEP mode is selected. STOP: Stops computer operation.

TABLE 3-3. Logic Panel A2A3 Controls and Indicators (continued)

Control or Indicator	Type	Function
RESTART/START STEP	Toggle switch	START STEP (momentary): Starts computer operation in selected mode. RESTART: Allows the OP STEP and PHASE STEP modes to be executed at a rate determined by setting of RESTART SPEED CONTROL.
RESTART SPEED CONTROL	Potentiometer	Controls frequency of a low speed oscillator from 2 to 100 Hz.

II - OPERATING PROCEDURES

3-2. ENERGIZING. - Perform the following procedure to apply power to the computer.

1. Throw main power switch on to apply ac voltage to computer cabinet.

2. Place POWER ON/OFF switch to ON. POWER indicator is lighted and approximately 30 seconds later computer is ready for operation if sufficient airflow is attained.

3-3. MASTER CLEAR. - Computer circuits master clear automatically as dc power is initially applied to the computer. To master clear after initial power application, perform the following steps.

1. Place SEQ STOP/STOP switch to STOP.

   Note: - The computer cannot be master cleared while operating in the RUN mode.

2. Momentarily place MASTER CLEAR switch to down position.

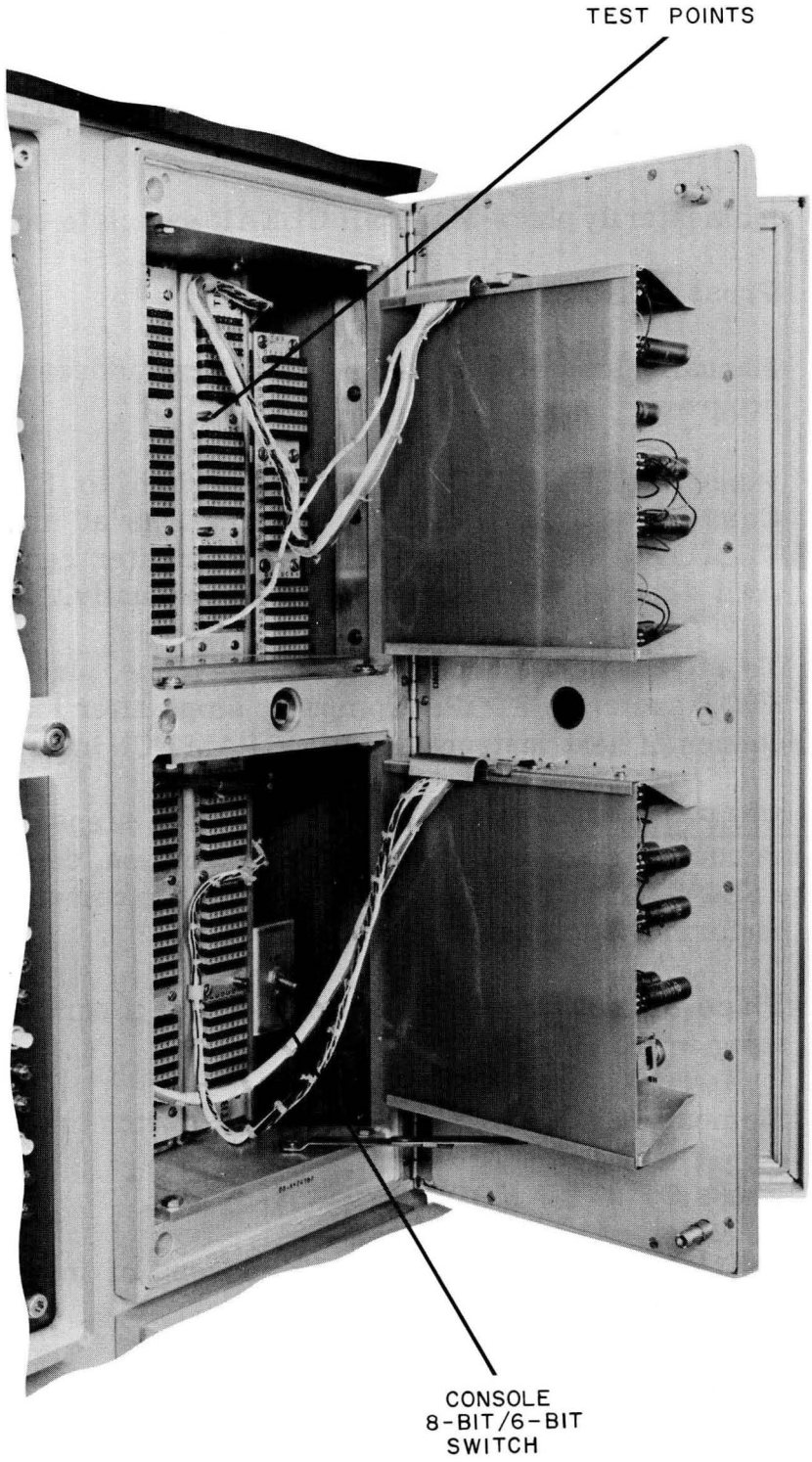


Figure 3-4. Console Input Bit Switch Location

3-4. MODES OF OPERATION. - The computer has three modes of operation: RUN, OP STEP, and PHASE STEP.

a. RUN Mode. - The RUN mode is the normal, computer mode of operation. To place the computer in the RUN mode, perform the following procedure.

1. Momentarily place MASTER CLEAR switch to down position.

2. Press RUN MODE indicator-switch.

3. Manually load P-register with starting address of computer program.

4. Place RESTART/START STEP switch to START STEP. Computer begins executing instructions at high speed and PROGRAM RUN indicator lights. Computer remains running until a fault occurs or until stopped manually.

5. To stop computer operating in RUN mode, place SEQ STOP/STOP switch to STOP. Computer stops after executing I-sequence of next instruction; PROGRAM RUN indicator goes out.

b. OP STEP Mode. - This mode of operation steps the computer through one instruction or one sequence of an instruction, depending on the position of the SEQ STOP/STOP switch. To operate the computer in the OP STEP mode, perform the following procedure.

1. Place SEQ STOP/STOP switch to STOP if computer is operating in RUN mode.

2. Momentarily place MASTER CLEAR switch to down position.

3. Press OP STEP MODE indicator-switch.

4. Manually load P-register with address of instruction to be executed.

5. Place SEQ STOP/STOP switch to SEQ STOP to enable stepping through one sequence of an instruction at a time, or leave it in normal position to enable stepping through one complete instruction at a time.

6. To enable sequential instructions or sequences to be performed, leave FUNCTION REPEAT switch in down position. To enable the same instruction or sequence to be performed repeatedly, place FUNCTION REPEAT switch in up position.

7. To perform OP STEP mode manually, place RESTART/START STEP switch to START STEP. Each time operator places switch to START STEP, computer executes one instruction or one sequence at high speed and then stops.

8. To perform OP STEP mode automatically, place RESTART/START STEP switch to RESTART. Computer executes one instruction or one sequence at variable speed and then stops. A low-speed oscillator controls rate at which OP STEP mode is performed. RESTART SPEED CONTROL controls frequency of low-speed oscillator from 2 to 100 cycles per second.

c. PHASE STEP Mode. - This mode of operation steps the computer through one clock phase at a time. This clock phase is either a different clock phase each time (PHASE REPEAT switch in normal position) or the same clock phase repeated (PHASE REPEAT switch in PHASE REPEAT position). To operate the computer in the PHASE STEP mode, perform the following procedure.

1. Place SEQ STOP/STOP switch to STOP if computer is operating in RUN mode.

2. Momentarily place MASTER CLEAR switch to down position.

3. Press PHASE STEP MODE indicator-switch.

4. Manually load P-register with desired address.

5. To perform a single clock phase repeatedly, place PHASE REPEAT switch to PHASE REPEAT (up) position and press one PHASE (1, 2, 3, or 4) indicator-switch. Computer automatically begins high-speed operation executing the selected clock phase. For non phase-repeat operation, omit this step and proceed to following steps.

6. Place PHASE REPEAT switch in normal position.

7. Press PHASE 1, 2, 3, or 4 indicator-switch to select beginning clock phase.

8. Place FUNCTION REPEAT switch in up position to continuously execute an allowable instruction.

9. To perform PHASE STEP mode manually, place RESTART/START STEP switch to START STEP. Each time operator places switch to START STEP, computer generates a single clock phase, performs those operations controlled by that clock phase, and then stops. The next sequential clock phase is performed the next time START STEP is operated.

10. To perform PHASE STEP mode automatically, place RESTART/START STEP switch to RESTART. Computer continuously generates sequential clock phases and performs those operations controlled by each clock phase. The low-speed oscillator controls rate at which clock phases are generated. RESTART SPEED CONTROL controls frequency of low-speed oscillator from 2 to 100 Hz.

3-5. PROGRAM LOADING. - Perform the following procedure to load computer programs from a paper tape unit or a magnetic tape unit.

1. Place SEQ STOP/STOP switch to STOP if computer is operating in RUN mode.

2. Momentarily place MASTER CLEAR switch to down position.

3. Press RUN MODE indicator-switch.

4. If program is on paper tape, manually load P-register with address 00060. This is address of first bootstrap instruction for loading a program from paper tape.

5. If program is on magnetic tape, manually load P-register with address 00070. This is address of first bootstrap instruction for loading a program from magnetic tape.

6. Check tape unit to ensure it is operative and program tape is loaded.

7. Place RESTART/START STEP switch to START STEP. Tape unit starts and reads program into computer.

3-6. EMERGENCY OPERATION.

a. Power Off. - If an emergency condition necessitates computer shutdown, perform the procedure in paragraph 3-7, page 3-22.

b. Computer Faults. - There are three types of computer faults: logic fault, overtemperature faults, and airflow fault.

(1) Logic faults. - There are two types of logic faults, those that can stop computer operation and those that cannot. The logic faults (errors) can be cleared either by momentarily placing the MASTER CLEAR switch to down position or by placing the RESTART/START STEP switch to START STEP.

(a) Halt and parity faults. - Halt and parity faults stop computer operation if the HALT DISCONNECT switch is in the normal position. A halt fault occurs when the computer reads an instruction with a function code of 00, 01, or 37. A parity fault occurs when the upper half or lower half of the word read from memory, including the associated parity bit, contains an even number of one bits. When either fault occurs, observe the following indications.

1) FAULT indicator lights.

2) Horn sounds (if not disconnected).

3) HALT or PARITY indicator-switch lights.

Notify maintenance personnel if a parity fault or non-programmed halt fault occurs.

(b) Overflow faults. - The overflow faults (data, switch, keyboard) do not stop computer operation. When an overflow fault occurs, observe the following indications.

1) FAULT indicator lights.

2) Horn sounds (if not disconnected).

3) One of OVERFLOW indicator-switches lights.

Overflow faults are not a hardware malfunction. Notify appropriate supervisory personnel when an overflow fault occurs.

(2) Overtemperature fault. - An overtemperature fault occurs when the cabinet internal temperature exceeds (46°C) 115°F. Computer operation does not stop unless temperature rises to (60°C) 140°F (see note). The horn sounds and the OVER TEMP indicator lights. Unless it is necessary to operate the computer with an overtemperature fault, perform the following procedure.

1. Place DISC HORN/HORN CLEAR switch to HORN CLEAR (down) position.

2. Place POWER ON/OFF switch to OFF.

3. Notify maintenance personnel.

Note: - A cabinet internal temperature (60°C) 140°F automatically removes computer dc voltages. However, the blowers continue to operate. To operate the computer with an overtemperature fault place the DISC HORN/HORN CLEAR switch to HORN CLEAR and notify maintenance personnel immediately.

(3) Airflow fault. - An airflow fault occurs when the blowers are not operating properly or when an air leak in the cabinet prevents sufficient airflow. Computer operation does not stop. The horn sounds and the AIR FLOW FAULT indicator lights. If continued computer operation is necessary, place the DISC HORN/HORN CLEAR switch to HORN CLEAR and notify maintenance personnel. However, if the computer is allowed to operate with an airflow fault, the cabinet internal temperature may rise high enough [60°C (140°F)] to automatically stop computer operation. If continued computer operation is not necessary, place POWER ON/OFF switch to OFF; then notify maintenance personnel.

3-7. DE-ENERGIZING. - Perform the following procedure to remove power from the computer.

1. Place POWER ON/OFF switch to OFF.

2. Throw main power switch off.

III - OPERATOR ADJUSTMENTS AND MAINTENANCE

3-8. ADJUSTMENTS. - The CP-818A/U requires no operator adjustments.

3-9. MAINTENANCE. - The CP-818A/U requires no operator maintenance.

CHAPTER 4

PRINCIPLES OF OPERATION

I - INSTRUCTION REPERTOIRE

4-1. GENERAL. - The CP-818A/U instruction repertoire consists of 31 instructions (see table 4-1). Since the formats of these instructions vary, the instructions are divided into eight groups. The following paragraphs supply the instruction word format (with any variables) and all associated word formats and a description of how each instruction operates.

TABLE 4-1. Instruction Repertoire

Function Code (f)	Mnemonic Notation	Instruction Name
Group I Instructions		
10	CLR	Clear Memory Address
12	STR	Store A
13	RPA	Replace Address
14	TRU	Transfer Unconditionally
15	TRA	Transfer on Accumulator
16	TRD	Transfer if Different
20	EXC	Exchange
22	ADO	Add One to Memory
23	AID	Add One if Different
24	RCA	Repeat Clear Add
25	ERC	End Repeat Count
30	CLA	Clear Add
31	ADD	Add
32	SUB	Subtract
33	COM	Compare

TABLE 4-1. Instruction Repertoire (continued)

Function Code (f)	Mnemonic Notation	Instruction Name
34	LGA	Logical Add
35	LGM	Logical Multiply
Group II Instruction (7 Sub-orders)		
06	SHF	Shift
06-0	SHL	Shift Left
	SCD or SCN (Type 00) SAD or SAN (Type 01) SXD or SXN (Type 10) SLD or SLN (Type 11)	(Suffix D, as in SXD, indicates decrement mode; suffix N, as in SXN, indicates nondecrement mode.)
06-1	DIV	Divide
06-2	SCA	Scale Accumulator
06-3	SCL	Scale Index and Accumulator
06-4	SHR SCR (Type 00) SAR (Type 01) SXR (Type 10) SLR (Type 11)	Shift Right
06-5	MUL	Multiply
06-6	SUD	Shift Until Different
Group III Instructions		
26	STX/SRC	Store Index/Store RC0
27	LDX/LRC	Load Index/Load RC0
Group IV Instructions		
02	TRF	Transfer on Flip-Flop or Status Line
03	TSR	Transfer to Subroutine
04	TRX	Transfer on Index

TABLE 4-1. Instruction Repertoire (continued)

Function Code (f)	Mnemonic Notation	Instruction Name
05	TAX	Transfer and Augment Index
Group V Instruction		
17	SWC	Sense Word Count
Group VI Instruction		
07	EXF	External Function
Group VII Instructions		
00 11	HLT	Halt
37	HLD	Stop
36	ADB	Add B
01	LGN	Logical Negation
Group VIII Instruction		
21	ADC	Add Constant to Memory

4-2. GROUP I INSTRUCTIONS.

a. Formats. - Figure 4-1, page 4-4, illustrates the instruction word formats and the index word format for the group I instructions. Figure 4-1A, page 4-4, shows the instruction word format for index register modification to the base address of the instruction. The lower 14 bits of any one of 36_8 memory locations (00001 through 00036) can be added to the base address of most group I instructions. For example, if the index register address is zero, no base address modification occurs; if the index register address equals one, the lower 14 bits of memory location 00001 are added to the base address of the instruction; if the index register address equals 36_8, the lower 14 bits of memory location 00036 are added to the base address.

Figure 4-1B, page 4-4, shows the instruction word format for most group I instructions when bits 14 through 18 equal 37_8. When bits 14 through 18 equal 37_8, the contents of the B-register are added to the base address. If

bits 9 through 13 of the instruction are not equal to zero, the contents of an index register are added to the modified address of the instruction. Figure 4-2, page 4-5, shows examples of both types of instruction address modification.

Figure 4-1C shows the format of the index words (memory locations 00001 through 00036). The tally field is a value used by the computer program to count various computer conditions or events see paragraphs 4-5b(3), page 4-17, and 4-5b(4), page 4-17. The address field is the value added to the base address of the instruction.

b. Descriptions.

(1) Clear memory address (10). - This instruction stores zeros in the memory location specified by the address portion of instruction. The base address can be modified with the contents of an index register and/or the B-register. $0 \longrightarrow Y$.

23 - 19	18 - 14	13 - 0
FUNCTION CODE (f)	INDEX REGISTER ADDRESS ($1_8 - 36_8$)	BASE ADDRESS

A. Instruction Word Format for Index Register Modification

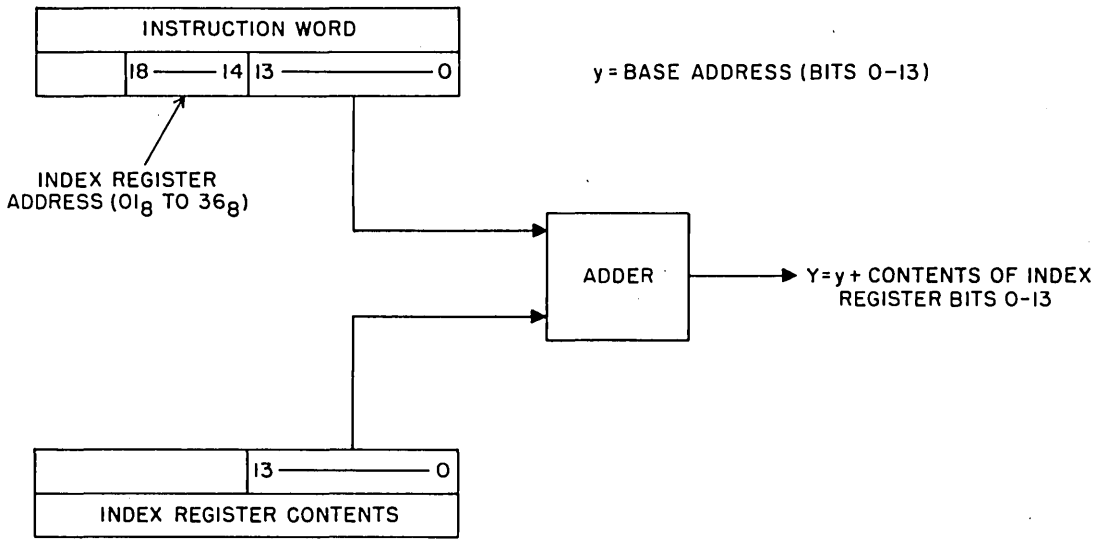
23 - 19	18 - 14	13 - 9	8 - 0
FUNCTION CODE (f)	B-REGISTER ADDRESS (37_8)	INDEX REGISTER ADDRESS ($1_8 - 36_8$)	BASE ADDRESS

B. Instruction Word Format for Index and/or B-Register Modification

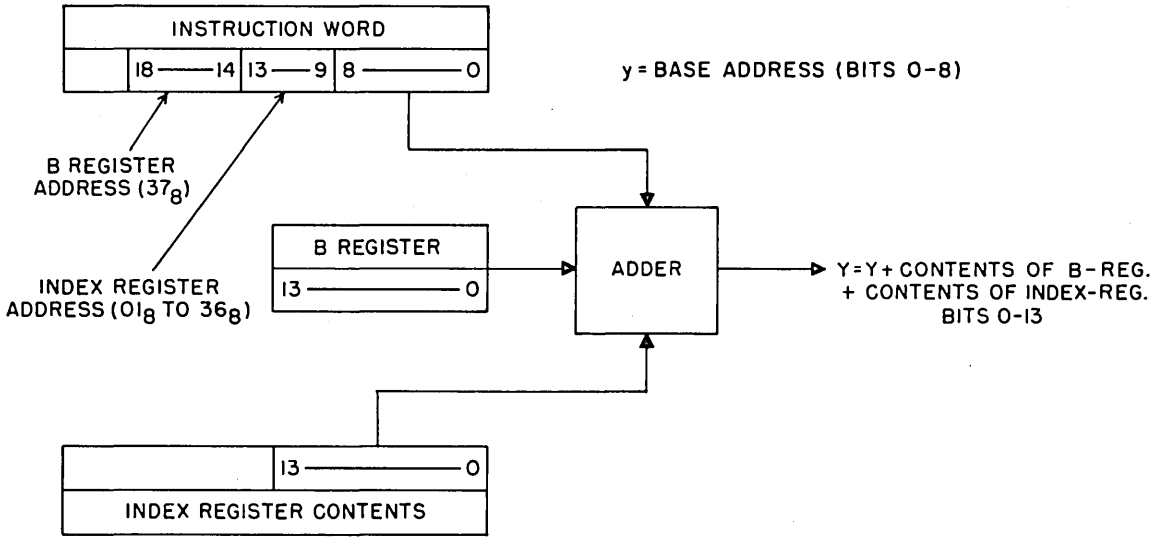
23 - 14	13 - 0
TALLY FIELD	ADDRESS FIELD

C. Index Word Format

Figure 4-1. Group I Instruction Word Formats and Index Word Format



A. BASE ADDRESS MODIFICATION WITH MEMORY INDEX REGISTER CONTENTS



B. BASE ADDRESS MODIFICATION WITH BOTH MEMORY INDEX REGISTER CONTENTS AND B REGISTER CONTENTS

Figure 4-2. Examples of Instruction Address Modification

(2) Store A (12). - This instruction stores the contents of the A-register in the memory location specified by the address portion of the instruction. The base address can be modified with the contents of an index register and/or of the B-register. (A) $\longrightarrow$ Y.

(3) Replace address (13). - This instruction replaces the low-order 14 bits of the memory location specified by the address portion of the instruction with the low-order 14 bits of the A-register. The instruction address can be modified with the contents of an index register and/or the B-register. $(A_{0-13}) \longrightarrow Y_{0-13}$ and $(Y_{14-23})i = (Y_{14-23})f$.

(4) Transfer unconditionally (14). - This instruction transfers program control from the present memory position to the memory location specified by the address portion of the instruction. The base address can be modified with the contents of an index register and/or the B-register. NI = (Y).

(5) Transfer on accumulator (15). - This is a conditional transfer (jump) instruction, and its operation depends upon the contents of the A-register.

1) If the contents of the A-register equal zero, no program transfer occurs and the next sequential instruction is executed. If A = 0: NI = (P).

2) If the contents of the A-register are positive ($A_{23} = 0$), program control transfers from its present memory position to the memory location specified by the address portion of the instruction. The base address can be modified with the contents of an index register and/or the B-register. If A > 0: NI = Y.

3) If the contents of the A-register are negative ($A_{23} = 1$), the next sequential instruction is skipped.
If A < 0: NI = (P) + 1.

(6) Transfer if different (16). - This is a conditional transfer instruction, and its operation depends upon the states of the upper bit of the A-register (A_{23}) and the A_{24} flip-flop. The A_{24} flip-flop sets when the A-register is left shifted and bit A_{23} is a one.

1) If the A_{23} and A_{24} flip-flops are both set or both clear, no program transfer occurs and the next sequential instruction is executed. If $A_{24} = A_{23}$: NI = (P).

2) If the A_{23} and A_{24} flip-flops are not in the same state (one set and the other cleared), program control transfers from its present position to the memory location specified by the address portion of the instruction. For this condition the base address can be modified with the contents of an index register and/or the B-register. If $A_{24} \neq A_{23}$: NI = Y.

(7) Exchange (20). - This instruction exchanges the contents of the A-register with the contents of the memory location specified by the address portion of the instruction. The contents of the A-register go to the memory location and the contents of the memory location go to the A-register. The instruction address can be modified with the contents of an index register and/or the B-register. (A)i $\longrightarrow$ Y and (Y)i $\longrightarrow$ Af.

(8) Add one (22). - This instruction adds one to the contents of the memory location specified by the address portion of the instruction. The base address can be modified with the contents of an index register and/or the B-register. (Y)i + 1 $\longrightarrow$ Yf.

(9) Add one if different (23). - This is a conditional, add-one instruction. Its operation depends upon the states of the upper bit of the A-register (A_{23}) and the A_{24} flip-flop. The A_{24} flip-flop sets when the A-register is shifted and the bit shifted out of A_{23} is a one.

1) If the A_{23} and A_{24} flip-flops are both set or both clear, continue with the next sequential instruction.
If $A_{23} = A_{24}$: no addition, NI = (P).

2) If the A_{23} and A_{24} flip-flops are not in the same state (one set and the other cleared), add one to the contents of the memory location specified by the address portion of the instruction. For this condition the base address can be modified with the contents of an index register and/or the B-register. If A23 $\neq$ A24: (Y)i + 1 $\longrightarrow$ Yf.

(10) Repeat clear add (24). - This instruction replaces the entire contents of the RCA control word (memory location 00040) with the contents

of the memory location specified by the address portion of the instruction and sets the RCA-flip-flop. The base address can be modified with the contents of an index register and/or the B-register. (Y) $\longrightarrow$ RCA CW1 and Set RCA FF.

The RCA instruction is used in conjunction with the SHF (06) and ERC (25) instructions to process data one bit at a time. As words being processed in the A-register are shifted, the RC-register is decremented by one for each bit shifted. When the register reaches zero, the next sequential word in memory is loaded into the A-register and the RC-register is reset with the refill count.

Figure 4-3 illustrates the RCA control-word format. The refill count specifies the number of times a word is to be shifted in multiples of four; four is the minimum and 28 the maximum number shifts. The refill count is stored in the RC-register ($Z_{21-23} \longrightarrow RC0_{2-4}$). The word count specifies the number of words to be shifted. The address specifies the beginning address of the first memory word to be shifted. Paragraph 4-16e(1)(b), page 4-52, contains a detailed operational description of the RCA shift mode. (The RCA instruction-word format is illustrated in A and B of figure 4-1, page 4-4.)

(11) End repeat count (25). - This instruction stores the contents of the RCA control word (memory location 00040) in the memory location specified by the address portion of the instruction. The address can be modified with the contents of an index register and/or the B-register. The instruction also clears the RCA control-logic flip-flop. (RCA CW1) $\longrightarrow$ Y and Clear RCA FF.

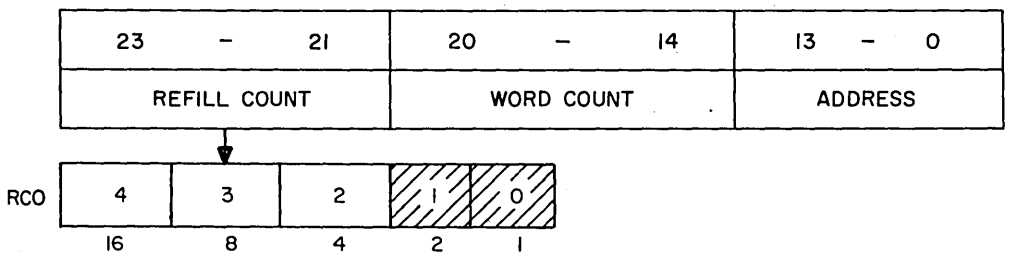


Figure 4-3. RCA Control Word Format

(12) Clear add (30). - This instruction replaces the contents of the A-register with the contents of the memory location specified by the address portion of the instruction. The base address can be modified with the contents of an index register and/or the B-register. (Y) $\longrightarrow$ A.

(13) Add (31). - This instruction adds algebraically the contents of the memory location specified by the address portion of the instruction to the contents of the A-register. The result remains in the A-register. The base address can be modified with the contents of an index register and/or the B-register. (A)i + (Y) $\longrightarrow$ Af.

(14) Subtract (32). - This instruction subtracts algebraically the contents of the memory location specified by the address portion of the instruction from the contents of the A-register. The result remains in the A-register. The base address can be modified with the contents of an index register and/or the B-register. (A)i - (Y) $\longrightarrow$ Af.

(15) Compare (33). - This instruction is a conditional skip instruction. The contents of the A-register are compared with the contents of the memory location specified by the address portion of the instruction. The base address can be modified with the contents of an index register and/or the B-register. The instruction operates as follows.

Note: For this instruction, all ones are less than all zeros.

1) If the contents of the A-register are greater (more positive) than the contents of the specified memory location, the computer program continues with the next sequential instruction. If (A) > (Y): NI = (P).

2) If the contents of the A-register are less (more negative) than the contents of the specified memory location, the next sequential instruction is skipped and the computer program continues. If (A) < (Y): NI = (P) + 1.

3) If the contents of the A-register are equal to the contents of the specified memory location, the next two sequential instructions are skipped and the computer program continues. If (A) = (Y): NI = (P) + 2.

(16) Logical add (34). - This instruction adds logically (without carries) the contents of the memory location specified by the address portion of the instruction to the contents of the A-register. The result remains in the A-register. The base address can be modified with the contents of an index register and/or the B-register. (A)i $\oplus$ (Y) $\longrightarrow$ Af.

Example: (Y) = 0011
(A)i = 0101
(A)f = 0110

(17) Logical multiply (35). - This instruction multiplies (bit by bit) the contents of the A-register with the contents of the memory location specified by the address portion of the instruction. The results remain in the A-register. The base address can be modified with the contents of an index register and/or the B-register. (A)i + (Y) $\longrightarrow$ Af.

Example: (Y) = 0011
(A)i = 0101
(A)f = 0001

4-3. GROUP II INSTRUCTION.

a. Format. - Figure 4-4, page 4-11, illustrates three different instruction-word formats for the group II (SHF, 06) instruction. The shift count (bits 0 through 4) specifies the number of shifts to be performed; the number of shifts for a divide or multiply operation is normally 24_{10}.

The sub-order (bits 5 through 7) indicates that one of the sub-orders listed in table 4-2, page 4-12, is to be executed. The mode designator is used for a shift left (06-0) instruction only and indicates the following:

Mode
1 - Do not decrement repeat counter.

0 - Decrement repeat counter if the RCA flip-flop is set.

(See instructions 24 and 25, pages 4-7 and 4-8.)

The type shift (bits 12 and 13) specifies circular or end-off shifting and designates the registers to be shifted. See table 4-3, page 4-12.

23 19	18 14	13 12	11	10 8	7 5	4 0
FUNCTION CODE	INDEX REGISTER ADDRESS	TYPE SHIFT	MODE	BLANK	SUB ORDER	SHIFT COUNT

A. FORMAT FOR SHIFT INSTRUCTIONS OTHER THAN SUB-ORDER 001_2 AND 101_2

23 19	18 14	13 12 11 10 9	8	7 5	4 0
FUNCTION CODE	INDEX REGISTER ADDRESS (DIVISOR)	INDEX REGISTER ADDRESS(DIVIDEND) (UPPER)	BLANK	SUB ORDER (001_2)	SHIFT COUNT

B. FORMAT FOR SUB-ORDER 001_2 (DIVIDE) INSTRUCTION

23 19	18 14	13 8	7 5	4 0
FUNCTION CODE	INDEX REGISTER ADDRESS (MULTIPLICAND)	BLANK	SUB ORDER (101_2)	SHIFT COUNT

C. FORMAT FOR SUB-ORDER 101_2 (MULTIPLY) INSTRUCTION

Figure 4-4. Shift Instruction Word Format

TABLE 4-2. Shift Instruction Sub-Orders

Sub-Order Bits 7 6 5	Shift Instruction	Reference
0 0 0	Shift Left (SHL)	06-0
0 0 1	Divide (DIV)	06-1
0 1 0	Scale Accumulator (SCA)	06-2
0 1 1	Scale Index and Accumulator (SCL)	06-3
1 0 0	Shift Right (SHR)	06-4
1 0 1	Multiply (MUL)	06-5
1 1 0	Shift Until Different (SUD)	06-6

TABLE 4-3. Shift Instruction Type Shift

		Sub-Order	
Type Bits 13 12		000 (SHL) Left Shifting	100 (SHR) Right Shifting
0 0	Shift A-Register Circular	SCN SCD	SCR
0 1	Shift A-Register End-Off	SAN SAD	SAR
1 0	Shift Index Register End-Off	SXN SXD	SXR
1 1	Shift Index and A-Register End-Off	SLN* SLD**	SLR*

* Mode 1 or RCA flip-flop clear
** Mode 0 and RCA flip-flop set

For sub-orders 000_2 and 100_2 (SHL and SHR), the index-register address (bits 14 through 18) designates which of the 37_8 index registers is to be shifted. These bits are only significant for type 10 and 11 instructions. For sub-order 001_2 (DIV), bits 14 through 18 designate the address of the index register containing the divisor; bits 9 through 13 designate the address of the index register containing the most significant bits of the dividend. The index-register address is not used for sub-order 010_2 (SCA). For sub-order 011_2 (SCL), the index-register address (bits 14 through 18) designates which index register is to be scaled at the time the A-register is scaled. For sub-order 101_2 (MUL), the index-register address designates the location of the multiplicand. For sub-order 110_2 (SUD), the index register specified by bits 14 through 18 counts the number of times the A-register is shifted.

b. Description. - The shift instruction is divided into six types. The type of shift instruction to be performed is selected by the sub-order code of the shift instruction format. A detailed description of the seven shift functions is provided in paragraph 4-16e, page 4-50.

(1) Shift left (SHL, 06-0). - This instruction sub-order shifts the contents of the A-register (previously loaded) and/or the contents of an index register to the left. The instruction specifies the number of shifts.

(2) Shift right (SHR, 06-4). - This instruction sub-order shifts the contents of the A-register (previously loaded) and/or the contents of an index register to the right. The instruction specifies the number of shifts.

(3) Multiply (MUL, 06-5). - This instruction sub-order multiplies the contents of the specified index register (multiplicand) with the contents of the previously-loaded A-register (multiplier). A 46-bit product of the two operands is obtained by this operation. The low order bits of the product are in the A-register and the high order bits are loaded into the index register that supplied the multiplicand.

(4) Divide (DIV, 06-1). - This instruction sub-order divides a 46-bit dividend by a 23-bit divisor. The result is a 23-bit quotient plus a 23-bit remainder. The low-order bits of the dividend are (previously loaded) in the A-register. The high-order bits of the dividend are in the index register specified by bits 9 through 13 of the instructions. The divisor is in the index register specified by bits 14 through 18 of the instruction.

At the completion of the dividing operation, the quotient is stored in the A-register and the remainder is loaded into the index register that provided the high-order bits of the dividend.

(5) Scale accumulator (SCA, 06-2). - This instruction sub-order scales the contents of the A-register left (cyclic) until the two high-order bits are different ($A_{23} \neq A_{22}$) or shift counter equals zero. Either positive or negative numbers can be scaled. The index field (bits 14 through 18) of the instruction word is not used. The shift counter is loaded with the contents of the shift count in the instruction word. Shifting terminates when A_{22} and A_{23} are different (scaled accumulator), or when the shift counter decrements to zero (may or may not be scaled). When shifting terminates because the shift counter decrements to zero, the accumulator is scaled only if A_{22} and A_{23} are different (not zeros or ones at the same time).

(6) Scale index and accumulator (SCL, 06-3). - This instruction sub-order scales a 48-bit operand contained in the specified index-register (high-order 24 bits) and the A-register (low-order 24 bits). The index field of the instruction word specifies the index register to be shifted. In this sub-order, the A-register (loaded by the previous instruction) and the L-register are left shifted together one place at a time, end-around. Shifting continues until the two high-order bits of the Z-register (Z_{20} and Z_{21}) are different, or the shift count register decrements to zero.

(7) Shift until different (SUD, 06-6). - This instruction sub-order shifts the contents of a buffer left (end-off through the A-register) until bits 23 and 24 are different or buffer terminates. The index register specified in this instruction is used to tally the number of shifts. The RCA FF, the mode bit, and the shift field of the instruction word have no significance.

4-4. GROUP III INSTRUCTIONS.

a. Format. - Figure 4-5, page 4-15, illustrates the instruction word format for the group III instructions. The two group III instructions load index registers or store the contents of index registers elsewhere in memory. These instructions both operate on an index register and can be modified by an index register.

Bits 14 through 18 specify which register contents are added to the base address of the instruction. If bits 14 through 18 equal 0, the base address is not modified. If bits 14 through 18 equal 1_8 through 36_8, the contents of

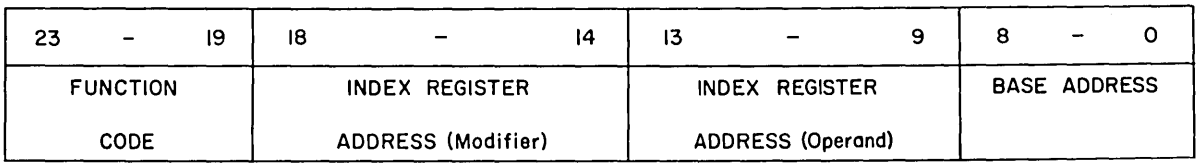


Figure 4-5. Group III Instruction Word Format

an index register are added to the base address. If bits 14 through 18 equal 37_8, the contents of the B-register are added to the base address.

Bits 9 through 13 specify which register is operated on. Table 4-4 lists the interpretations of these bits for the two group III instructions.

b. Descriptions.

(1) Store index (26). - This instruction replaces the contents of the memory location specified by the address portion of the instruction with the contents of the index register specified by the instruction index field

TABLE 4-4. Group III Instructions, Bits 9 through 13, Interpretation

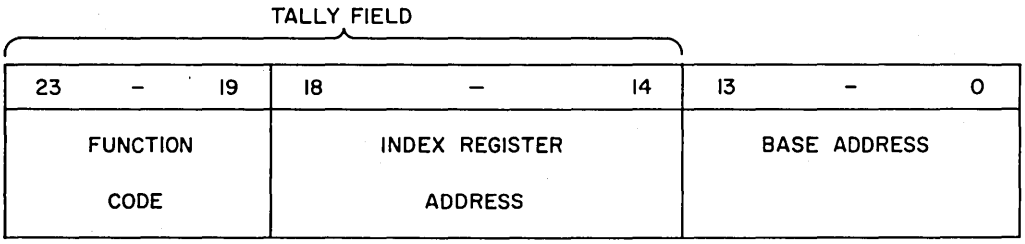
Instruction	Interpretation
26	
All zeros	Repeat counter is operated on.
1_8 through 37_8	An index register is operated on.
27	
All zeros	Repeat counter is operated on.
1_8 through 36_8	An index register is operated on.
37_8 (instruction 26)	Index register 37_8 is operated on.
37_8 (instruction 27)	Index register 37_8 and the B-register are operated on.

(bits 9 through 13). If no index register is specified, the instruction stores the contents of the repeat counter (RC) in the five low order positions of the memory location specified by the address portion of the instruction. The base address may be modified with the contents of either an index register or the B-register. (I) $\longrightarrow$ Y or $\left[(RC) \longrightarrow Y_{0-4} \text{ and } 0 \longrightarrow Y_{5-23}\right]$.

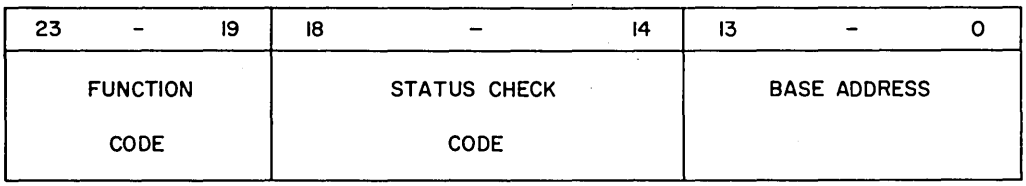
(2) Load index (27). - This instruction replaces the contents of the specified index register or index register and B-register with the contents of the memory location specified by the instruction address. If no index or B-register is specified, the five low order bits of the specified memory location are loaded into the repeat counter. The base address can be modified with the contents of either an index register or the B-register. (Y) $\longrightarrow$ I or $(Y_{0-4}) \longrightarrow$ RC.

4-5. GROUP IV INSTRUCTIONS.

a. Formats. - Figure 4-6 illustrates two different instruction-word formats for the group IV instructions. The base address of the group IV instructions cannot be modified. The index register address (bits 14 through 18) specifies the index register to be operated on. The status-check code (bits 14 through 18) specifies which status condition is to be checked.



A. Format for 03 (TSR), 04 (TRX), 05 (TAX) Instructions



B. Format for 02 (TRF) Instruction

Figure 4-6. Group IV Instruction Word Formats

b. Descriptions.

(1) Transfer on flip-flop or status line (02). - This instruction is a conditional transfer instruction. The instruction checks the control-logic jump flip-flop or status line specified by the status-check code portion of the instruction. If the specified flip-flop or status line is set, the program continues in normal sequence. If the specified flip-flop or status line is not set, program control transfers from its present position to the memory location specified by the address portion of the instruction. Table 4-5, page 4-18, lists the status-check codes and the conditions they check. FF CLR: NI = Y; FF Set: NI = (P)

(2) Transfer to subroutine (03). - This is an unconditional transfer instruction. This instruction stores the contents of the P-register (next instruction address) into bits 0 through 13 of the index register specified by the instruction. The lower 14 bits of the instruction (next instruction address) are then transferred to the P-register.
$(P) \longrightarrow I_{0-13}$, NI = Y.

(3) Transfer on index (04). - This is a conditional transfer instruction. If the tally-field portion (I_t) of the index register specified by the instruction equals zero, no program transfer occurs and the next sequential instruction is executed. If the tally field does not equal zero, it is decremented by one, and program control transfers from its present position to the memory location specified by the instruction address.

If the index-register-address portion of the instruction equals 37_8, only the index register 37_8 is referenced and not the B-register.
If $I_t = 0$: NI = (P). If $I_t \neq 0$: $(I_t)i - 1 \longrightarrow I_t$ and NI = Y.

(4) Transfer and augment index (05). - This is a conditional transfer instruction. If the tally-field portion of index register specified by the instruction equals zero, no program transfer occurs and the next sequential instruction is executed. If the tally field does not equal zero the following occurs.

1) The tally field (I_t) of the specified index register is decremented by one

2) The address-field (I_a) of the specified index register is incremented by one

TABLE 4-5. Transfer Conditions

Status Check Codes	Status Condition	Equipment
0 0 0 0 0	Tape Mark	TCU
0 0 0 0 1	Tape Busy	TCU
0 0 0 1 0	Data Transfer Error	TCU
0 0 0 1 1	Transport Ready	TCU
0 0 1 0 0	Input Overflow	TCU
0 0 1 0 1	Control Error	TCU
0 0 1 1 0	RCA (Set)	Computer Control Section
0 0 1 1 1	$A_{23} = A_{24}$	Computer Control Section
0 1 0 0 0	Initiate	Auxiliary Computer
0 1 0 0 1	Output Busy	Auxiliary Computer
0 1 0 1 0	Input Busy	Auxiliary Computer
0 1 0 1 1	Console Switch Input Word Complete	Consoles 0, 1, 2, or 3
0 1 1 0 0	Console Data Control Word 1 Complete	Console 0
0 1 1 0 1	Console Data Control Word 1 Complete	Console 1
0 1 1 1 0	Console Data Control Word 1 Complete	Console 2
0 1 1 1 1	Console Data Control Word 1 Complete	Console 3

3) Program control transfers from its present position to the memory location specified by the instruction address.

Note: - If the index-register-address portion of the instruction equals 37_8 and the tally-field portion of index register 37_8 does not equal zero, both index register 37_8 and the B-register are operated on. The tally-field portion of the index register is incremented by one, and the incremented address field is transferred to the B-register. If $(I_t) = 0$: NI = (P). If $(I_t) \neq 0$: $(I_t)i - 1 \longrightarrow (I_t)f$, $(I_a)i + 1 \longrightarrow (I_a)f$, and NI = Y.

4-6. GROUP V INSTRUCTION.

a. Format. - Figure 4-7 illustrates the variable instruction-word format for sense word count instruction (17).

b. Description. - The sense word count (SWC) instruction is a conditional skip instruction. It checks the word-count portion of a memory word specified by the address portion of the instruction. This memory is normally an I/O or RCA control word. If the word count equals zero, the next instruction of the program is skipped. If the word count is not equal to zero, no instruction is skipped and the program continues. The 17 instruction has two modes of operation. If bit 9 of the instruction is zero, a 7-bit word count (bits 14 through 20) is checked. If bit 9 of the instruction is one, an 8-bit word count (bits 14 through 21) is checked. The base address may be modified with the contents of an index register (01_8 through 36_8) or the contents of the B-register (37_8). If $I_{14 - 20 \text{ or } 21} \neq 0$: NI = (P); If $I_{14 - 20 \text{ or } 21} = 0$: NI = (P) + 1; or Ywc $\neq 0$: NI = (P); Ywc = 0: NI = (P) + 1.

23 - 19	18 - 14	13 - 10	9	8 - 0
FUNCTION CODE	INDEX REGISTER ADDRESS	BLANK	MODE	BASE ADDRESS

Figure 4-7. Group V Instruction Word Format

4-7. GROUP VI INSTRUCTION.

a. Format. - Figure 4-8 illustrates the instruction-word format for the external function instruction (07). The peripheral-unit code specifies which peripheral equipment receives the external function code or specifies time base interrupt. (See table 4-6). When this codes specifies the auxiliary computer, it also specifies the function that the auxiliary computer is to perform.

Note: - The consoles initiate their own input and output operations and thus no external function for the consoles is required.

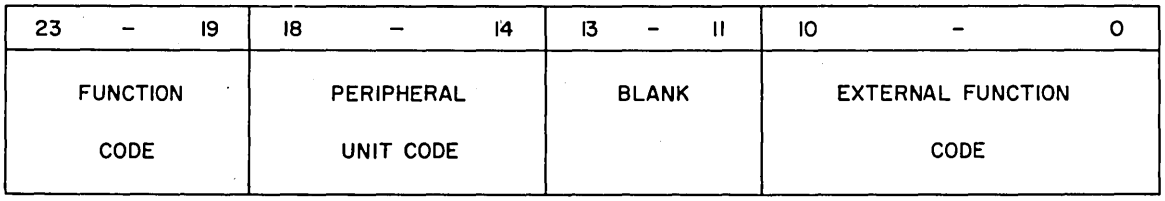


Figure 4-8. Group VI Instruction Word Format

TABLE 4-6. Peripheral Unit Codes

Peripheral Unit Code	Peripheral Unit
0 0 0 0 1	TCU
0 0 0 1 0	RD-277A
0 0 0 1 1	PCU
0 0 1 0 0	Auxiliary Computer Output
0 0 1 1 0	Auxiliary Computer Input
0 0 1 1 1	Time Base Interrupt

The external function code specifies the type of operation the computer wants the peripheral unit to perform or the type of interrupt instruction to be performed (arm or disarm). Tables 4-7 through 4-10, pages 4-21 through 4-24, list the function codes for the TCU, RD-277A, PCU and time base interrupt.

b. Description. - This instruction sends an external function code which either instructs a peripheral unit to perform an input or output operation, or controls a time base interrupt operation. The time base interrupt provides a variable count interrupt under program control. The range of variability is from one millisecond to one second in one-millisecond steps. The interrupt is initiated (armed) by an EXF instruction with a 300_8 code. (A 240_8 code will disarm the interrupt.) A control word in memory location 42 must be previously loaded with a count (tally) and a jump address (address of subroutine). A control word in memory location 43 must be previously loaded with a TRU function code in order to return to the main routine at the point of exit. The time base interrupt has the highest priority in the I/O system.

TABLE 4-7. TCU Function Codes

External Function Code	Function
Bits 2^2 - 2^0	
0 0 0	Tape Transport 0 Address
0 0 1	Tape Transport 1 Address
0 1 0	Tape Transport 2 Address
0 1 1	Tape Transport 3 Address
1 0 0	Tape Transport 4 Address
1 0 1	Tape Transport 5 Address
1 1 0	Tape Transport 6 Address
1 1 1	Tape Transport 7 Address

TABLE 4-7. TCU Function Codes (continued)

External Function Code	Function
Bits 2^7 - 2^3	
1 0 0 0 0	Halt
1 0 0 0 1	Status
1 0 0 1 0	Read Odd Parity
1 0 0 1 1	Read Even Parity
1 0 1 0 0	Backspace Odd Parity
1 0 1 0 1	Backspace Even Parity
1 0 1 1 0	Rewind
1 0 1 1 1	Unload
1 1 0 0 0	Write Odd Parity
1 1 0 0 1	Write Even Parity
1 1 0 1 0	Write End of File
1 1 0 1 1	Write End of File
1 1 1 0 0	Write Extended Inter-Record Gap, Odd Parity
1 1 1 0 1	Write Extended Inter-Record Gap, Even Parity
1 1 1 1 0	Write Extended Inter-Record Gap, End of File
1 1 1 1 1	Write Extended Inter-Record Gap, End of File

TABLE 4-8. RD-277A Function Codes

Function Codes		
For Computer $2^{10} - 2^{7}$	For RD-277A $2^{6} - 2^{0}$	Function
0 0 0 1	0 0 0 0 0 0 1	Turn Punch Off
0 0 0 1	0 0 0 1 0 0 0	Turn Reader Off
0 0 0 1	0 0 0 1 0 0 1	Turn Reader and Punch Off
1 0 0 1	0 1 0 1 0 0 0	Turn Reader On
1 0 1 1	0 1 0 1 0 0 0	Turn Reader On with Lockout
0 1 0 1	0 0 0 0 1 0 1	Turn Punch On
1 1 0 1	0 1 0 1 1 0 1	Turn Reader and Punch On
1 0 0 1	0 1 0 1 0 0 1	Turn Reader and Punch Off
0 1 0 1	0 0 0 1 1 0 1	Turn Punch On and Reader Off
0 1 1 1	0 0 0 0 1 0 1	Turn Punch On with Lockout
1 1 1 1	0 1 0 1 1 0 1	Turn Reader and Punch On with Lockout
1 0 0 1	1 0 0 0 0 0 0	Zero Suppression

TABLE 4-9. PCU Function Codes

External Function Code Bits 2^7 - 2^0	Function
1 1 x x x x x x	Select Printer *
1 0 1 0 0 0 0 0	Deselect Printer **
1 0 0 0 0 0 0 0	No Print

* Selects one of a possible 40_{10} printers/ punches

** The deselect printer function code is in response to a data request from the PCU. The printer/punch deselected is the one that the PCU requested data for.

TABLE 4-10. Time Base Interrupt Function Codes

External Function Code Bits 2^7 - 2^0	Function
1 1 x x x x x x	Arm Interrupt
1 0 1 x x x x x	Disarm Interrupt

When armed, the computer makes requests at a one KHz rate. As each request is honored, the control word in address 42 is read and a tally check is made:

If the tally does not equal zero, it is decremented by 1 and restored to address 42 with no change in the jump address. The program then proceeds to the next instruction.

If the tally equals zero, the contents of the P-register are written into address 43. The jump address from location 42 is then loaded into the P-register. The program proceeds to the jump address (address of the subroutine), and the time base interrupt is automatically disarmed. A jump instruction to address 43 is required to return to the interrupted routine (main routine).

4-8. GROUP VII INSTRUCTIONS.

a. Format. - Figure 4-9 shows the instruction word format for the group VII instructions. The group VII instructions do not use address modification and are completed within four microseconds.

b. Description.

(1) Halt (00, 11). - The halt instruction conditionally stops computer operation. With the HALT DISCONNECT switch in the center position, the computer stops when a halt instruction is executed. The FAULT indicator lights and the horn, if not disabled, sounds. With the HALT DISCONNECT switch in the up position, the computer does not stop when a halt instruction is executed. However, the FAULT indicator lights and the horn, if not disabled, sounds. There is no address modification.

(2) Stop (37). - The stop instruction may be eliminated from a program by operator request during an assembly run. In all other respects, the stop instruction is the same as the halt (00, 11) instruction.

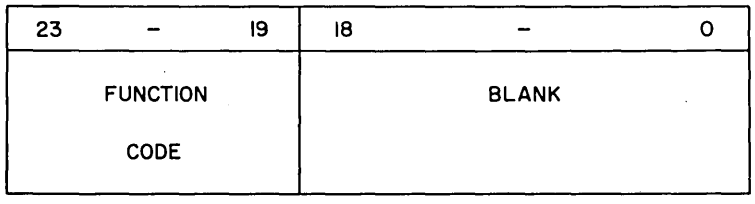


Figure 4-9. Group VII Instruction Word Format

(3) Logical negation (01). - This instruction complements the contents of the A-register. It changes ones to zeros, and zeros to ones. Ai $\longrightarrow$ A.

(4) Add B (36). - This instruction algebraically adds the contents of the B-register to the contents of the A-register. The 24-bit result is stored in the A-register and the 14 low order bits are stored in the B-register. (B)i + (A)i $\longrightarrow$ A and $(A_{0-13}) \longrightarrow$ B.

4-9. GROUP VIII INSTRUCTION.

a. Format. - Figure 4-10 shows the instruction word format for the add constant to memory (21) instruction. This instruction does not use index modification. C + (Y) $\longrightarrow$ Y.

b. Description. - This instruction adds the five bit constant specified in bits 14 through 18 to the contents of the memory location specified by the address portion of the instruction word.

23 – 19	18 – 14	13 – 0
FUNCTION CODE	CONSTANT	ADDRESS

Figure 4-10. Group VIII Instruction Word Format

II - BLOCK DIAGRAM DESCRIPTION

4-10. GENERAL. - The computer consists of five functional sections: control, arithmetic, input/output, memory, and power. Figure A-1, page A-3, is a block diagram of the computer, showing all computer sections except power.

4-11. CONTROL SECTION. - The control section generates timing signals, and memory addresses, and routes data between the memory and all computer sections. The timing and control signals read instructions, interpret them, and execute them. The memory addresses specify the memory locations for reading instructions, instruction operands, and peripheral unit data from memory and for writing instruction operands

and peripheral unit data into memory. All data transfers to and from memory are via the control section.

a. Computer Control. - Computer control master clears, starts, and stops the computer and initiates the mode of operation from panel controls. The computer has three modes of operation: RUN, OP STEP, and PHASE STEP (refer to paragraph 3-4, page 3-18).

b. Timing Circuits. - The timing circuits consist of a master clock, main timing chain, arithmetic timing chain, shift timing chain, and advance-P timing logic.

(1) Master clock. - The master clock generates four pulses every 667 nanoseconds. Each pulse is approximately 167 nanoseconds long. The four pulses (Ø1, Ø2, Ø3, and Ø4) comprise one clock cycle; six clock cycles (four microseconds) comprise one computer (memory) cycle.

(2) Main timing chain. - The main timing chain, along with outputs from the master clock and other control section circuits, generates the timing signals required to perform the instructions. The main timing chain cycles continuously when the computer is in the RUN mode, stopping momentarily during arithmetic and shift instructions, and during instructions where skip conditions exist.

(3) Arithmetic timing chain. - The arithmetic timing chain generates the signals necessary to perform arithmetic operations. Arithmetic operations consist of incrementing and decrementing index words and control words and of performing logical negation, addition, subtraction, division and logical multiplication.

(4) Shift timing chain. - The shift timing chain generates the signals required to perform the shifting portion of the shift instruction.

(5) Advance-P timing logic. - The advance-P timing logic generates the signals required to increment the P-register. The P-register contains the memory address of the next instruction to be performed.

c. Sequence Circuits. - The sequence circuits, along with the timing chains and master clock, generate the signals required to perform the instructions. Each instruction requires that certain sequences be performed in a specific order. The sequence circuits consist of a sequencer and sequence enable circuits. The sequencer indicates the sequence in process

and provides multiple outputs throughout the computer logic. These outputs, combined with timing chain outputs, master clock outputs, and other control signals, initiate the functions that must be performed during the sequence. The sequence enable circuits monitor the current sequence, the current instruction, and other control signals to enable the next sequence. At completion of the current sequence, the output of the sequence enable circuits is gated to the sequencer and the next sequence starts.

d. Function Circuits. - The function circuits consist of an F-register and a function code translator. The F-register is loaded from the Z-register when an instruction is read from memory. It stores the 5-bit function code (bits 19 through 23) portion of the instruction while the instruction is executed.

The function code translator decodes the F-register contents into enable signals. These enable signals represent the different instructions; they go to the sequence circuits and other circuits to control execution of the instruction.

e. Shift Circuits. - The shift circuits control computer operation during a shift instruction. The shift circuits consist of a shift counter (K-register), and shift control. The shift counter is loaded from the Z-register when a shift instruction is read from memory. It counts the number of shifts specified by the instruction and indicates to shift control when the specified number of shifts has been performed. The repeat counter is loaded from the Z-register when a shift instruction specifying an RCA mode shift is read from memory. The RCA mode allows the computer to process sequential words in memory as a continuous stream of data. As the word being processed in the accumulator is shifted, the repeat counter is decremented by one for each bit shifted. When the counter reaches zero, the next sequential memory word is read into the accumulator, and the counter is reset to continue the processing. Shift control initiates the type of shift operation specified by the contents of the K and RC-registers and generates the control enables for the appropriate circuits.

f. Address Circuits. - The address circuits consist of the P, S, and B-registers. The P-register holds the memory address of the next instruction to be performed. While an instruction is operating, the contents of P are transferred to S (memory address register) which holds the instruction address while the instruction is being performed. When S is loaded, the address is sent to the memory circuits and the instruction is read into the Z-register. Immediately after the P register contents are

transferred to S, they are also sent to the arithmetic section. The arithmetic section adds one to the current address and returns the incremented address to P. If the current instruction specifies a jump or skip, the P-register is cleared and reloaded with the new value later in the instruction.

The B-register functions as an index register or as an operand register. It stores a quantity which can be referenced by instructions to modify the instruction address. Normally it holds the 14-bit address of index 37 (see figure 4-2, page 4-5). However, a 36 (ADB) instruction loads an operand into the register and it is added to the value in the A-register with the lower order 14 bits returned to B.

g. Data Transfer Circuits. - The data transfer circuits transfer data between the memory section to all other computer sections. The data transfer circuits consist of a Z-register, selector, and parity circuits.

(1) Z-register. - The Z-register is a 24-bit, data-routing register. It is the output register for main memory and bootstrap memory. It is also an output register for the arithmetic section. Portions of the memory data loaded into the Z-register go to the K and RC-registers, F-register, M-register, and C-register. The data which the Z-register receives from the arithmetic section generally goes to the selector for storage in memory.

(2) Selector. - The selector functions as a word assembler and a data transfer path. It assembles characters from input peripheral equipment into words that are stored in main memory. The selector also routes data from the Z-register to main memory and the X-register. Data from the Z-register to the selector transfers directly or shifts one place to the left or right.

(3) Parity circuits. - The parity circuits generate parity bits for data written into memory and for some output operations and check the parity of each word read from memory. When a parity error (the 26-bit word read from memory contains an even number of ones) occurs, computer operation stops and the PARITY ERROR and FAULT indicators light.

h. M-Register. - The M-register is loaded from the Z-register to perform either of two functions. It holds the memory-index-register-address portion of most instructions and it holds the status check code portion of the 02 (TRF) instruction. The index register addresses go to the S-register to read up the index contents for operand address modification

(see figure 4-2, page 4-5). The status check code generates status circuits enables.

i. Status Circuits. - The status circuits monitor and control input/output conditions and compare the status-check-code portion of the 02 (TRF) instruction (contained in the M-register) with the existing status conditions (see paragraph 4-5, page 4-16). If the status condition specified by the instruction exists, the computer program continues in sequence. If the status condition specified by the instruction does not exist, the program control transfers to another memory location.

j. Fault Circuits. - The fault circuits detect computer faults and control computer operation when a fault occurs. The fault circuits detect five faults: halt, parity, console data overflow, console switch overflow, and console keyboard overflow. When the fault circuits detect a halt or parity fault, the associated indicator and FAULT indicator light, the horn sounds, and computer operation stops. When the fault circuits detect an overflow fault, the associated indicator and FAULT indicator light, the horn sounds, but computer operation does not stop. When any computer fault occurs, it is indicated at the consoles.

4-12. ARITHMETIC SECTION. - The arithmetic section performs arithmetic and logical operations. Arithmetic operations are addition, subtraction, multiplication, and division. Logical operations are complementing, shifting, comparison, addition, and logical multiplication. The control section and the input/output section time-share the arithmetic section. The control section uses the arithmetic section to modify instruction addresses (P-register) and to perform the arithmetic instructions. The input/output section uses the arithmetic section to update control words. The arithmetic section consists of an X-register, D-register, adder, A-register, and U-register.

a. X-Register. - The X-register is an exchange register between the data transfer circuits and the other arithmetic registers. Operands from memory enter the arithmetic section via the data transfer circuits and the X-register. Data from the arithmetic section that is to be stored in memory leaves the arithmetic section via the X-register (or the adder). The X-register holds one of the operands added or subtracted by the adder.

b. D-Register. - The D-register holds one operand during the multiply or divide instruction and one of the operands added or subtracted by the adder. The D-register inputs are from the X-register, M-register, A-register, or B-register.

c. Adder. - The adder is a 24-bit subtractive type. It subtracts the complement of the operand in the D-register from the operand in the X-register. The X and D-register adder inputs are not gated so the adder output is always the difference between the X-register contents and the complemented D-register contents. Addition is performed by loading X and D with the operands to be added. Subtracting the complement of D from X results in the addition of the two operands. Subtraction is performed by loading D with the complement of the operand and X with the other operand. Then during the D-to-adder transfer the contents of D are recomplemented, and the result is the difference of the two operands.

d. A-Register. - The A-register is an accumulator and a data transfer register. It receives inputs from the adder and the D and U-registers and transfers data to the X, U, and D-registers. The D-register inputs are for complementing and for exchanging the A-register contents with the contents of a memory location. The U-register inputs are for shifted data. The adder inputs are for the results of arithmetic and logical operations. The A-register outputs to the X-register are for adding the contents of B to A and storing the contents of A in memory. In some SHF operations, A_{23} is transferred to X_{00}. The A-register outputs to the U-register are for left-shifting or right-shifting the A-register contents. The A-register outputs to the D-register are for logical negation (LGN).

e. U-Register. - The U-register serves as the lower rank for the A-register shifting operations. The contents of the A-register are shifted left or right when sent to the U-register. The shifted data is sent back to the A-register.

4-13. INPUT/OUTPUT SECTION. - The computer receives data from input peripheral equipment and sends data to output peripheral equipment via the input/output section. The computer controls the transfer of data between it and all peripheral equipment. However, the peripheral consoles initiate data transfers to and from the computer when data is available or requested by the operator.

a. Input/Output Control. - Input/output control monitors the sequencer output to determine if an input/output sequence is in process. If no input or output data transfer is in process, input/output control gates input and output requests from the peripheral equipment into the input/output request logic. Input/output control performs other functions described in paragraph 4-18b(1), page 4-109.

b. Input/Output Requests. - The input/output request logic stores input and output data requests from the peripheral equipment until they have been honored by the computer. Signals from the input/output request logic go to input/output priority and acknowledge circuits.

c. Input/Output Priority. - Priority determines which input or output request is honored first if more than one are present. When an input or output data request is present, the control section delays operation of the computer program at the end of the current instruction, and the I/O data requests present are processed. After processing all I/O requests, the computer program continues until another I/O data request is received. The order of priority is listed in paragraph 4-18b(3), page 4-130.

d. Data Input Gates. - The data circuits gate data from input peripheral equipment to computer memory via the selectors. If the data is from a console or PCU, a memory address accompanies the data. Otherwise, the origin of the input data request determines where in memory the data is to be stored.

e. Address Input Gates. - The address input amplifiers receive the address that accompanies input and output requests from the consoles and the address that accompanies output requests from the PCU and send it to the S-register with preset bits. The console address accompanying console input data identifies the origin of the data within the console and specifies the address of the memory control word for that data. The memory control word specifies where the data is to be stored. The console address accompanying a request for output data identifies the console unit requesting data and specifies the address of the memory control word for the data. The memory control word specifies the memory location from where the data is to be removed. The address accompanying the PCU output request specifies which of the printers or punches is requesting data and the location of the memory control word for that printer or punch. This memory control word specifies the memory location from where the data is stored.

f. C-Register. - The 8-bit C-register temporarily stores output data until it is accepted by peripheral equipment. C-register enables determine which portion of the 24-bit memory output is transferred from the Z-register to the C-register.

g. Acknowledge Circuits. - The input/output acknowledge circuits monitor the input and output data request selected by priority. From this information, these circuits provide enable signals which gate the appropriate

input data to memory or gate output data from memory to the C-register, and which also generate input and output acknowledge signals for the peripheral equipments.

4-14. MEMORY SECTION. - The memory section consists of a main memory, a bootstrap memory, and associated control and drive circuits. Both memories are random-access, with a four-microsecond cycle time.

a. Main Memory. - The main memory consists of 16,384 (16,368 useable) core storage locations. The memory consists of two chassis. Each chassis stores 16,368 13-bit (half-words) words. One bit of each half-word is a parity bit.

b. Main Memory Control. - Main memory control controls the reading of data from memory and the writing or restoring of data in memory. It also monitors the printed-circuit-card voltages and disables the memory and stops the computer when logic voltages drop below minimums. Memory control cycles each time a sequence is executed. It does not cycle when a bootstrap memory location is referenced or when the computer is in the PHASE STEP mode.

c. Address Translator. - The address translator translates the S-register outputs to select the specified memory stack and the read, write, and inhibit current generators.

d. Read, Write, and Inhibit Current Generators. - The current generators supply read, write, and inhibit currents through the memory cores. A read generator supplies read current through the selected cores to read data from memory into the Z-register. A write current generator supplies write current through the selected cores to write data (from the Z-register via the selector) into memory or to restore data previously read out of memory. The inhibit current generator supplies inhibit current opposite in direction to the write current to prevent switching of the cores that are to remain in a zero state.

e. Bootstrap Memory. - The nondestructive-readout bootstrap memory consists of 16 permanently-wired storage locations. This memory is divided into two parts. Each part has 16 permanently wired 13-bit half-words. One bit is a parity bit. The bootstrap memory addresses are octal 00060 through 00077. Addresses 00060 through 00067 contain instructions for loading a computer utility program via an RD-277A. Addresses 00070 through 00077 contain instructions for loading a computer utility program via a TCU.

Whenever the S-register contains a bootstrap memory address, the bootstrap control disables main memory control and gates the bootstrap words into the Z-register. The bootstrap address translator automatically activates the proper drive line causing the word to be read out to the Z-register. No restore cycle is required.

4-15. POWER SECTION. - The power section consists of dc power supplies and power control circuits. The dc power supplies furnish power to the printed circuit cards and panel indicators. The power control circuits apply power to the computer, remove power from the computer, and control the lighting and extinguishing of power control indicators.

III - FUNCTIONAL DESCRIPTION

4-16. CONTROL SECTION.

a. Computer Control (figure 4-11, page 4-35).

(1) Master clear (figure 8-1a, page 8-3). - The operator cannot master clear the computer when it is operating in the RUN mode (PROGRAM RUN indicator lighted). Placing the MASTER CLEAR switch to the down (MASTER CLEAR) position returns all computer circuits to their initial operating condition. Also, if any of the printed circuit card voltages drop below the normal value, the computer circuits are master cleared.

(2) Modes of operation. - The computer has three modes of operation: RUN, OP STEP, and PHASE STEP. The RUN mode is the on-line mode of operation. The OP STEP and PHASE STEP modes are off-line modes used for program debugging and maintenance.

(a) RUN mode. - The operator selects the RUN mode (figure 8-1, page 8-1) by pressing the RUN MODE indicator-switch. This starts the master clock via circuit 04J00. The OP STEP MODE and PHASE STEP MODE indicators are extinguished. The operator starts the computer by placing the RESTART/START STEP switch to START STEP. The run flip-flop sets via circuit 02J01 with the high outputs from the RESTART/START STEP switch and the start-enable-one-shot flip-flop. Run flip-flop outputs disable the master clear circuits, light the PROGRAM RUN indicator, start the main timing chain, and light the COMPUTER RUN indicators on the four consoles (figure 8-5, page 8-11). Computer operation begins when the main timing chain starts. An output from the run flip-flop also clears the start-enable-one-shot flip-flop. The start-enable-one-shot flip-flop performs the same function for all modes. The

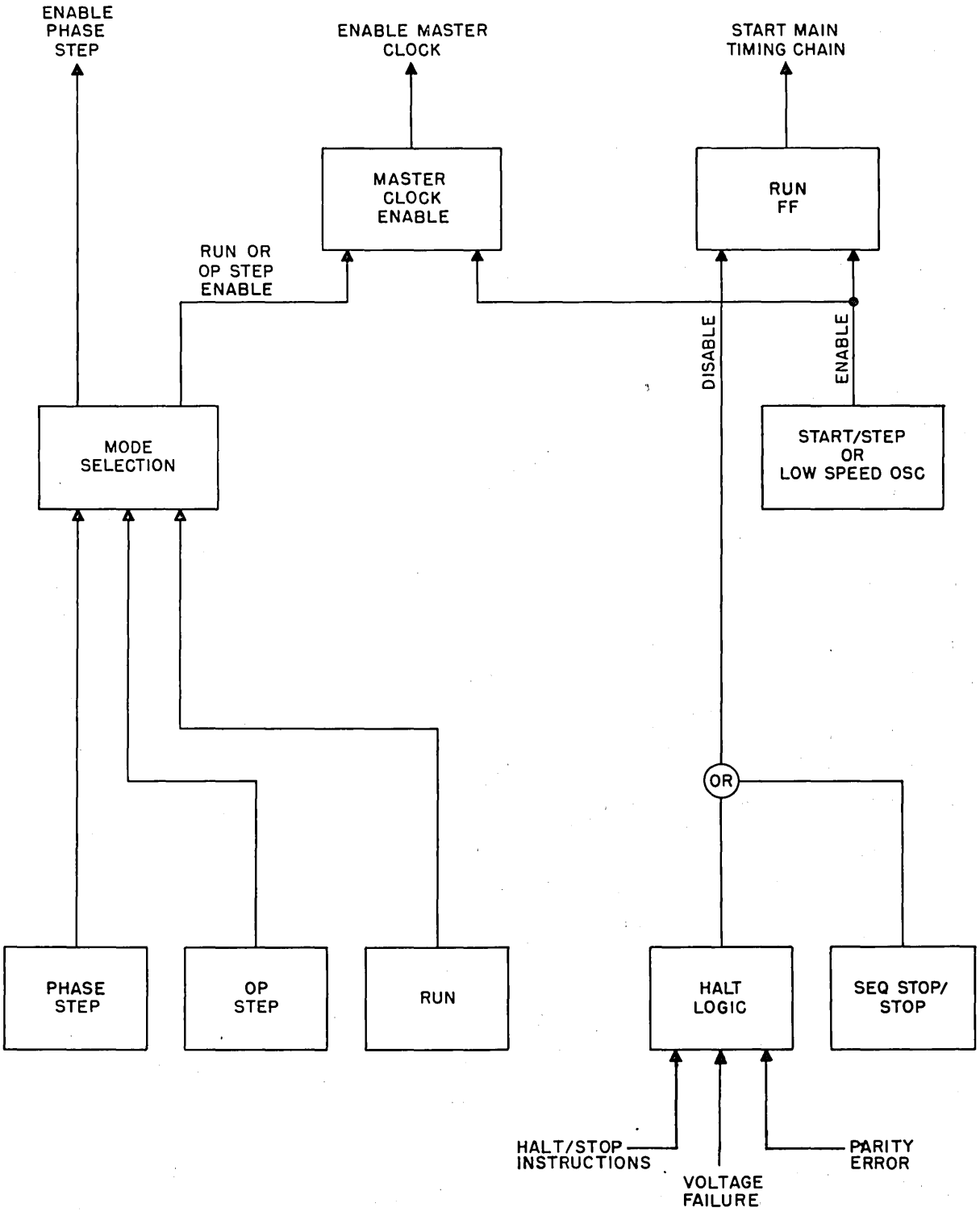


Figure 4-11. Computer Control Switches and Circuits

flip-flop sets when the RESTART/START STEP switch is in the neutral position and clears when the RESTART/START STEP switch is placed to the START STEP position. The flip-flop remains clear until the switch returns to the neutral position.

The purpose of the start-enable-one-shot flip-flop is to ensure that the computer stops when encountering errors, even though the operator may still be holding the RESTART/START STEP switch at START STEP. For example, the operator starts computer operation. A computer error that stops computer operation occurs before the operator releases the RESTART/START STEP switch to the neutral position. Without the start-enable-one-shot flip-flop, computer operation would not stop. With it, computer operation stops no matter how long the RESTART/START STEP switch is in the START STEP position. The start-enable-one-shot flip-flop that was cleared when computer operation started sets again when the RESTART/START STEP switch returns to the netural position.

Computer operation continues until a halt or parity error occurs, or until the operator places the SEQ STOP/STOP switch to STOP.

A halt occurs when the computer reads an 00, 11, or 37 (HLT) instruction to set the halt flip-flop and clear the run flip-flop at time 5.2 of the I-sequence. A parity error occurs when the 26-bit word read from memory contains an even number of ones. The parity error can occur during an I, M, or R-sequence; it clears the run flip-flop at time 5.2 of that sequence.

When the SEQ STOP/STOP switch is placed to STOP, the run flip-flop clears at time 5.2 of the next sequence. Any time the run flip-flop clears, it disables the main timing chain and stops the computer.

Note: - A halt or parity error does not stop computer operation if the HALT DISCONNECT switch is in the up (HALT DISCONNECT) position.

(b) OP STEP mode. - The operator selects the OP STEP mode (figure 8-1, page 8-1) by pressing the OP STEP MODE switch. This starts the master clock via circuit 04J00. The RUN MODE and PHASE STEP MODE indicators are extinguished.

The OP STEP mode can be started manually or automatically. To start it manually, the operator places the RESTART/START STEP to START STEP. To start it automatically, the operator places the RESTART/START STEP switch to RESTART. Then, a low-speed oscillator output performs

the same function as placing the RESTART/START STEP switch to START STEP. The low-speed oscillator is adjustable between 2 and 200 Hz. The computer control logic for starting the OP STEP mode manually or automatically operates the same as that for starting the RUN mode. The computer control logic for stopping the OP STEP mode differs from the RUN mode logic. Once the OP STEP mode starts, the computer operates to perform one instruction or one sequence of an instruction, depending upon the position of the SEQ STOP/STOP switch. If the SEQ STOP/STOP switch is in the SEQ STOP position, the run flip-flop clears at time 5.2 of every sequence. If the SEQ STOP/STOP switch is in the STOP position, the run flip-flop clears at time 1.2 of each I-sequence. Clearing the run flip-flop disables the main timing chain and stops the computer.

(c) PHASE STEP mode. - The PHASE STEP mode (figures 8-1, page 8-1, and 8-3, page 8-7) can be started manually or automatically. The PHASE STEP mode can be executed in two different ways. First, each time the mode is started, a different clock pulse is generated. Secondly, if the PHASE REPEAT switch is in the up (PHASE REPEAT) position, the selected clock pulse is generated continuously. The operator selects the PHASE STEP mode by pressing the PHASE STEP MODE indicator-switch. The RUN MODE and OP STEP MODE indicators are extinguished. Pressing the PHASE STEP MODE indicator-switch prepares the control logic for the PHASE STEP mode as follows.

1) It disables the memory. No memory reference can be made in the PHASE STEP mode.

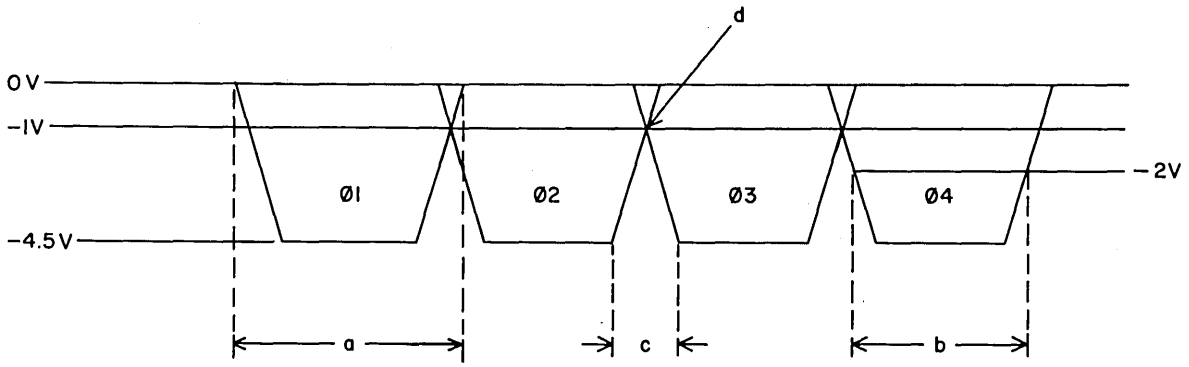
2) It disables the clock pulse amplifiers (50C01 through 50C04, figure 8-2, page 8-5) of the master clock. This enables the PHASE STEP mode logic (figure 8-3, page 8-7) to control the master clock output.

3) It enables the PHASE STEP logic (figure 8-3, page 8-7).

4) It disables the master clock via circuit 04J00 (figure 8-1, page 8-1). Now only the RESTART/START STEP switch can enable the master clock.

b. Timing Circuits.

(1) Master clock (figure 8-2, page 8-5). - Figure 4-12, page 4-38, shows the four clock pulses produced by the master clock. The



a = 167±34 nsec, Pulse Width at 0 v Amplitude

b = 120 nsec, Minimum Pulse Width at -2 v Amplitude

c = 10 nsec, Pulse Separation at 100% Amplitude

d = No Overlap at -1 v Amplitude

Figure 4-12. Master Clock Output

master clock consists of a feedback amplifier, delay network, phase generator circuits, phase flip-flops, and phase drivers.

The feedback amplifier (term 20C00), in series with the delay line network, inverts signals after they have propagated down the delay network. The delay network consists of one 100-nanosecond delay (term 20C10) and two 50-nanosecond delays (terms 20C20 and 20C30). Each delay has ten taps (taps 6 through 15). For the 100-nanosecond delay, each tap is a 10-nanosecond delay. For the 50-nanosecond delay, each tap is a 5-nanosecond delay. Two phase-generator circuits, odd and even, receive delay line outputs and, from these outputs, help generate the clock pulses and set and clear the phase flip-flops. The two phase flip-flops, and the phase generator circuits control the phase drivers to produce the four clock phases. Figure A-2, page A-5, shows the master clock timing.

The clock control logic provides enables for starting and stopping the clock. A high input to the feedback amplifier (20C00) starts the clock; a low input stops it. When the start signal appears, the clock begins cycling. The first pulse generated is an odd-numbered clock pulse. If the previous

stop signal occurred during Ø1 or Ø2 clock pulse time, the clock starts with a Ø3 clock pulse. If the previous stop signal occurred during Ø3 or Ø4 clock pulse time, the clock starts with a Ø1 clock pulse.

While the clock is stopped, all delay, phase-generator-circuit and phase-driver outputs are high. If the clock previously stopped after Ø2 clock pulse time, both odd and even phase flip-flops are set. If the clock previously stopped after Ø4 clock pulse time, both phase flip-flops are clear. Assume that the first clock pulse to be generated is Ø1.

When the clock starts, a low output from the feedback amplifier enables the odd-phase-generator circuit and starts propagating. With the odd-phase-generator output low, and the odd flip-flop clear, phase driver 50C01 is enabled, a Ø1 clock pulse is generated, and the even-phase flip-flop sets. The Ø1 output remains until the low input from the feedback amplifier propagates through the delay network to tap 9 of delay line 2. The odd-phase generator is disabled and the Ø1 clock pulse drops. After the low clock-enable signal propagates through the delay network, the feedback amplifier inverts it to a high, and a high begins propagating through the delay network. When the high signal reaches tap 7 of delay line 1, it enables the even-phase generator. With the even-phase generator output a low, and the even flip-flop set, phase amplifier 50C02 generates the Ø2 clock pulse. Also, the odd-phase flip-flop sets. The Ø2 output remains until the high signal propagates through the delay network and reaches tap 9 of delay line 2. The even-phase generator is then disabled and the Ø2 clock pulse drops. The high signal, after propagating through the delay network, is again inverted by the feedback amplifier. Clock pulses Ø3 and Ø4 are initiated and terminated the same as clock pulses Ø1 and Ø2, except that both phase flip-flops are set for Ø3 and Ø4.

The CLOCK ODD NARROW/NORMAL and EVEN NARROW/NORMAL switches are maintenance switches. When these switches are in the NORMAL position, the master clock outputs are as shown in figure 4-12, page 4-38. When the switches are in the NARROW position, the duration of each clock pulse is 80 to 110 nanoseconds.

(2) Main timing chain (figures 8-5, page 8-11, and 8-6, page 8-13). - The main timing chain times the operations that are performed during all computer sequences. The main timing chain consists of 12 series-connected flip-flops. During the run mode, these flip-flops continuously set and clear in sequence, stopping momentarily during skip instructions, when the skip condition is satisfied, and during shift instructions. One complete cycle of the main timing chain takes four microseconds.

Figure 4-13, page 4-41, is a timing diagram for the main timing chain. Each main timing chain cycle requires six master clock cycles. Six flip-flops (T11, T21, T31, T41, T51, T61) set at Ø2, remain set for one clock cycle, and clear at the following Ø2. The remaining six flip-flops (T13, T23, T33, T43, T53, T63) set at Ø4, remain set for one clock cycle, and clear at the following Ø4. Thus, two adjacent flip-flops are always set at the same time. The timing chain flip-flops have usable outputs for two of the four clock phases for which they are set. Those flip-flops set at Ø2 have outputs used during Ø4 and Ø1 time; those set at Ø4 have outputs used during Ø2 and Ø3 time. The flip-flop designators (T11, T13, T21, etc.) indicate when the flip-flop sets, clears, and has usable outputs. For example, flip-flop T21 has its usable outputs during Ø4 time of the first master clock cycle (time 1.4) and Ø1 time of the second master clock cycle (time 2.1). It sets at Ø2 time of the first master clock cycle, and clears at Ø2 time of the second master clock cycle.

Figure 4-14, page 4-42, shows two examples of how main-timing-chain outputs are used. Figure 4-14A, page 4-42, shows the main-timing-chain output from flip-flop T33. This output along with signals from the sequences and the master clock, generates signals to clear the Z-register and to gate a word from memory into the Z-register. The clear-Z signal occurs at time 3.2 of the R-sequence. Time 3.2 is the second clock phase in the third clock cycle of the R-sequence. The memory $\longrightarrow$ Z signal occurs one clock phase later. Figure 4-14B, page 4-42, shows the main-timing-chain output from flip-flop T51. The clear-X signal occurs at time 4.4 of the W-sequence. Time 4.4 is the fourth clock phase in the fourth clock cycle of the W-sequence. The X $\longrightarrow$ Z signal occurs one clock phase later at time 5.1.

Shift-control flip-flop 2 (figure 8-15, page 8-35) controls the main timing chain during shift instructions. During a shift instruction, the flip-flop sets until the shift operation is complete.

(3) Advance-P timing logic (figure 8-7, page 8-15). - The advance-P timing logic times and controls the incrementing of the P-register.

Figure 4-15, page 4-42, shows the operations controlled and timed by the advance-P timing logic and shows how the arithmetic section increments the P-register. The numbers on the lines indicate the order in which the events occur. The advance-P timing logic first clears the X and D-registers and then transfers the contents of the P-register to the X-register.

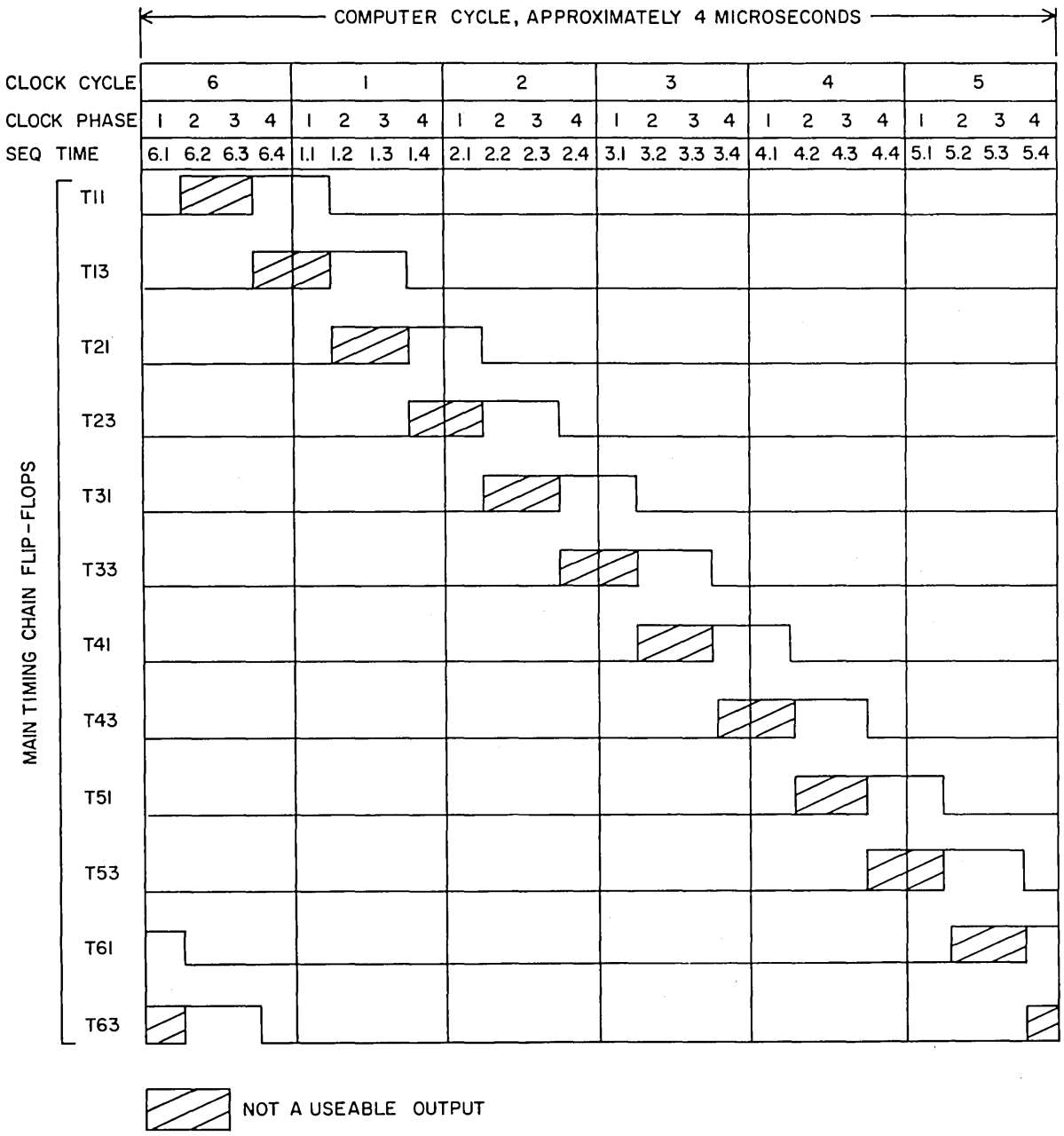


Figure 4-13. Main Timing Chain, Timing Diagram

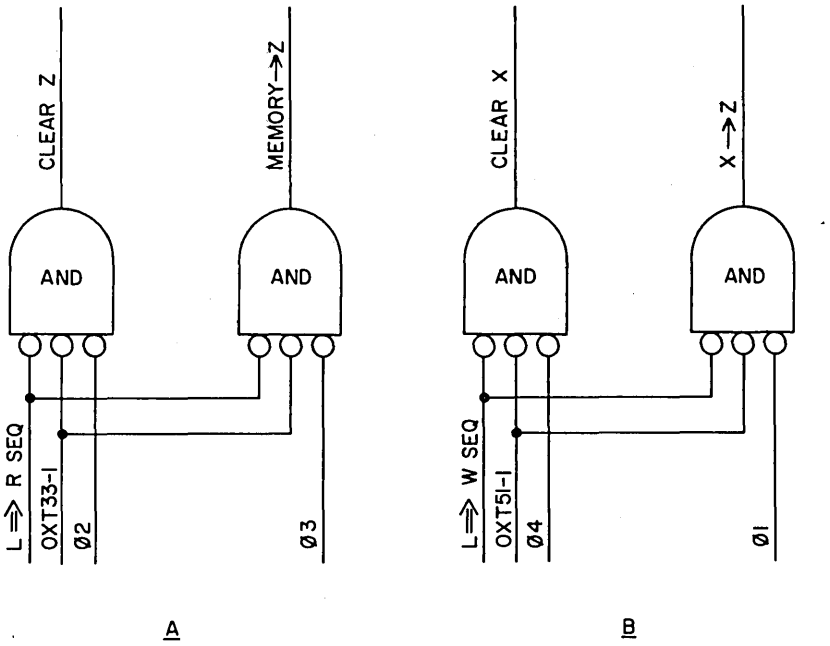


Figure 4-14. Main Timing Chain Outputs

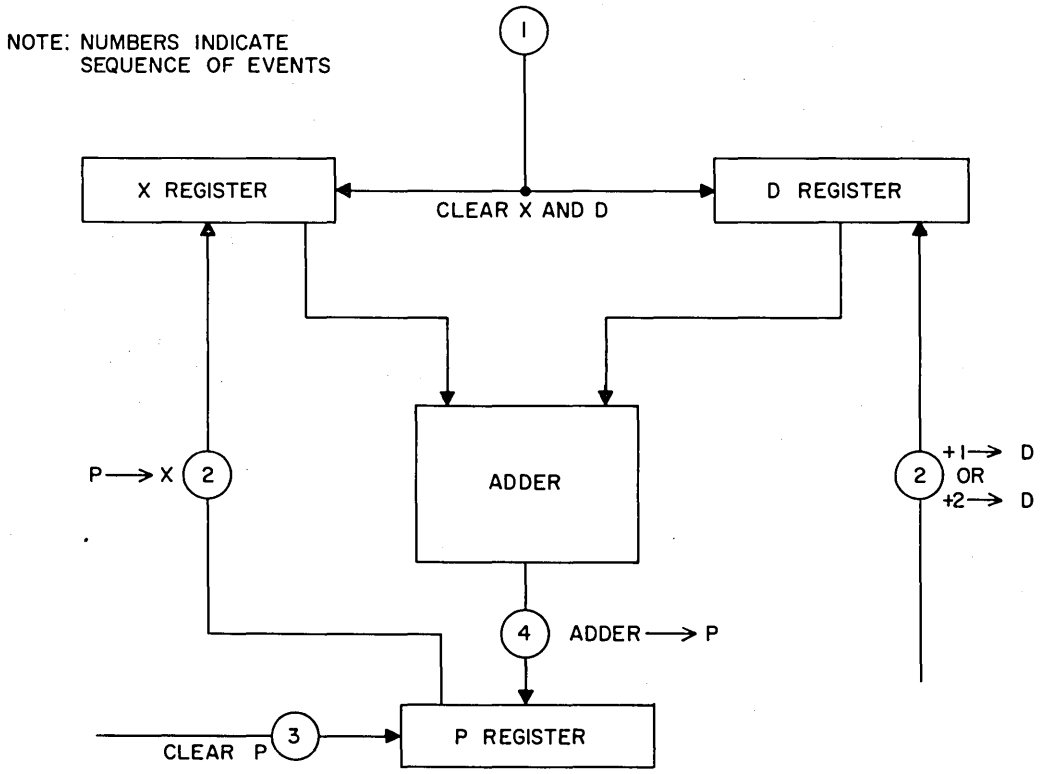


Figure 4-15. P-Register Operations

The D-register is set to plus one or plus two. The timing logic then clears the P-register and transfers the adder output to the P-register.

The P-register is incremented at different times during computer operation for different conditions.

Table 4-11 lists the conditions that increment the P-register and shows when the timing logic functions are performed.

The output of gate 08L01 (figure 8-7, page 8-15) is used to set the skip flip-flop during the R-sequence of the COM instruction. It also is used to enable the adder $\longrightarrow$ Z during the shifting sequence of the 06-1 (DIV) instruction.

(4) Arithmetic-timing (figure 8-8, page 8-17). - The arithmetic timing chain initiates and times some arithmetic section operations not controlled by the other computer sequences. The timing chain operates

TABLE 4-11. Increment P-Register Timing

Normal I-Sequence Time	R-Sequence Time			I-Sequence Time Instruction 15 & A Negative	Timing Logic Functions
	Instruction 33 & (A) = (Y) (Adder Equal FF Set)	Instruction 33 & (A) < (Y)	Instruction 17 & Word Counter = 0 (Skip FF Set)		
1.2	5.2	5.2	5.2	5.2	Clear X and D
1.3		5.3	5.3	5.3	Set D to +1
	5.3				Set D to +2
1.3	5.3	5.3	5.3	5.3	P $\longrightarrow$ X
2.2	6.2	6.2	6.2	6.2	Clear P
2.3	6.3	6.3	6.3	6.3	Adder $\longrightarrow$ P

during arithmetic instructions 30 (CLA), 31 (ADD), 32 (SUB), 34 (LGA), 35 (LGM) and 36 (ADB); during instructions 01 (LGN) and 20 (EXC); and during the RCA mode of instruction 06-0 (SHL), 06-1 (DIV), and 06-6 (SUD).

The timing chain consists of three series-connected flip-flops. These flip-flops cycle once and stop each time the timing chain is enabled. When the timing chain is enabled (by the setting of shift control flip-flop 2) during the shift instruction, it cycles through the last two flip-flops only. The timing chain runs concurrently with the sequence in which it is initiated and ends before the sequence. Thus, the main timing chain is not stopped for the arithmetic timing chain (except for the shifting operation). Table 4-12 lists the conditions that start the arithmetic timing chain and the functions performed by the timing-chain outputs.

c. Sequencer Circuits (figures 8-9 through 8-13 and 8-13a, pages 8-19 through 8-29). - The sequence circuits supply enable signals that, combined with main-timing-chain outputs, master clock outputs, and other computer signals, generate signals to execute all computer instructions. Each instruction requires certain groups of enable signals for proper execution. These groups of enable signals are referred to as sequences. A sequence lasts 4 microseconds (six master clock cycles). Paragraph 4-21, page 4-171, lists each computer instruction, shows the sequences required, shows the order in which they are executed, and contains a detailed description of the functions performed by each sequence.

The computer sequences are as follows.

1) I-sequence - reads the instruction from memory and transfers the various portions of the instructions to the proper circuits.

2) M-sequence - adds the contents of an index register to the address portion of most instructions.

TABLE 4-12. Arithmetic Timing Chain

Condition	Timing Chain Function
I-Sequence, Time 4.2 Instruction 01 (LGN)	5.2 Clear X 5.4 Clear A 6.1 $X \oplus D \longrightarrow A$

TABLE 4-12. Arithmetic Timing Chain (continued)

Condition	Timing Chain Function	
I-Sequence, Time 3.2 Instruction 36 (ADB)	4.2 Clear X 4.3 A $\longrightarrow$ X, B $\longrightarrow$ D 4.4 Clear A	
R/W-Sequence, Time 3.2 Instruction 06 (SHF) RCA Mode or SUD	06-0 SHL RCA	06-6 SUD
	4.1 If BT + RC0 = 0: $\overline{X} \longrightarrow D$ If $\overline{BT} \cdot RC0 \neq 0$: $\overline{\overline{X}} \longrightarrow D$ 4.2 Clear X 4.3 A $\longrightarrow$ X 4.4 Clear A 5.1 $\overline{D} \longrightarrow$ A	4.1 $\overline{X}$ D 4.2 Clear X 4.3 A $\longrightarrow$ X 4.4 Clear A 5.1 $\overline{D} \longrightarrow$ A
Shift Terminate, Time Ø4 Set RC1-Sequence	Following Ø2 (T6.2) Clear X, D Ø3 (T6.3) Z $\longrightarrow$ X Ø4 (T6.4) Clear A Ø1 (T1.1) X $\oplus$ D $\longrightarrow$ A	
R-Sequence, Time 3.2 Instructions: 20 (EXC), 30 (CLA), 31 (ADD), 32 (SUB), 34 (LGA), 35 (LGM)	4.1 $\overline{X} \longrightarrow$ D (instructions 20, 30, 32, 35) 4.1 X $\longrightarrow$ D (instructions 31, 34) 4.2 Clear X 4.3 A $\longrightarrow$ X 4.4 Clear A 5.1 $\overline{D} \longrightarrow$ A (instructions 20, 30, 35) 5.1 X $\oplus$ D $\longrightarrow$ A (instruction 34)	
M-Sequence, Time 3.2 Instruction 06-1 (DIV)	4.1 $\overline{X} \longrightarrow$ D 4.2 Clear X 4.3 A $\longrightarrow$ X	
R-Sequence, Time 4.2 Instructions 06-0 (Shift Left, RCA Mode), 06-6 (SUD) if RC0 = 0	5.1 $\overline{X} \longrightarrow$ D 5.2 Clear X 5.3 A $\longrightarrow$ X 5.4 Clear A 6.1 $\overline{D} \longrightarrow$ A	

3) R-sequence - reads the operand from the memory location specified by the instruction address.

4) W-sequence - writes the operand in the memory location specified by the instruction address.

5) RC1-sequence - reads control word #1 from memory. This may be the RCA control word or an input/output control word.

6) RC2-sequence - reads control word #2 from memory. This may be the RCA control word or an input/output control word. The RC2 sequence is initiated only when the word count of control word #1 equals zero.

7) R/W-sequence - reads data from memory for output to peripheral equipment or writes data in memory received from input peripheral equipment.

8) WC-sequence - updates the memory control words. It increments the address, decrements the word count, resets the character count, and writes control word 2 into the address of control word 1.

The sequencer circuits consist of sequence enables and upper and lower-rank sequence flip-flops. Figure 4-16, page 4-47, is a block diagram of these circuits. The sequence-enable circuits monitor the current sequence, the instruction, and the computer conditions encountered while executing the instruction. From this information, they decide which sequence should be executed next. Near the end of the current sequence, a sequence-enable output sets an upper-rank sequence flip-flop that corresponds to the next sequence to be executed.

The upper-rank sequence flip-flops indicate the sequence in process and, near the end of the sequence, indicate the next sequence. There is one flip-flop for each sequence. At time 5.4 of the current sequence, the upper-rank sequence flip-flops clear. At time 6.1 of the current sequence, the flip-flop corresponding to the next sequence is set by an enable signal from the sequence-enable circuits. Upper-rank sequence flip-flop outputs, along with outputs from the lower-rank sequence flip-flops, help perform the sequence functions.

The lower-rank sequence flip-flops indicate the current sequence. There is a flip-flop for each sequence and only one flip-flop is set at any time.

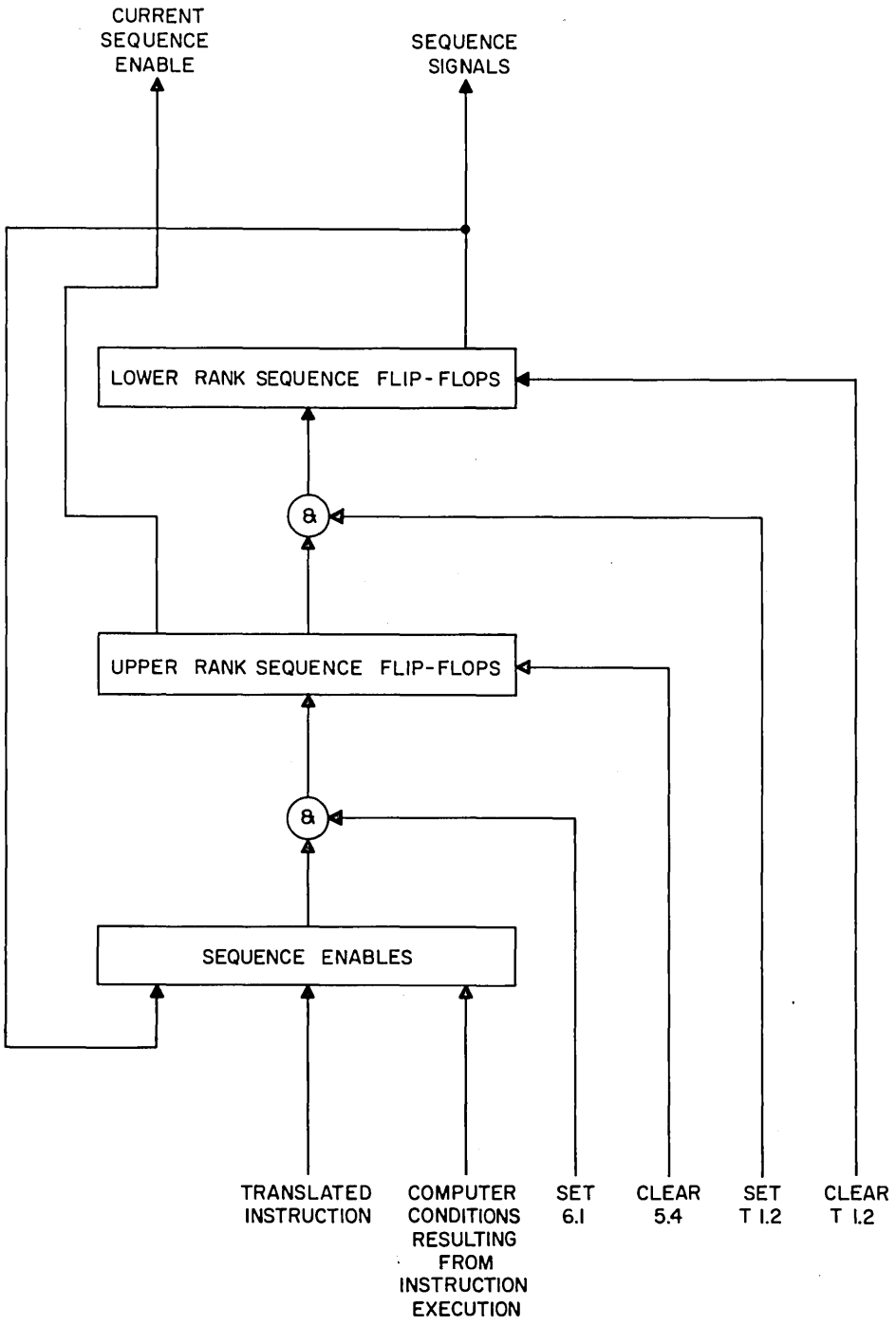


Figure 4-16. Sequencer Circuits

Outputs from the lower-rank sequence flip-flops help perform the sequence functions. The lower-rank sequence flip-flops are updated at time 1.2 of a new sequence. The flip-flop that sets corresponds to the set upper-rank flip-flop; the previously set lower-rank flip-flop is cleared.

The first sequence of an instruction is always the I-sequence. The sequences that follow depend upon the instruction and conditions encountered during the instruction. Input/output operations have priority over the computer program. Any time input or output requests are present, the computer program stops at the end of an instruction and does not start again until all input or output requests are processed. When the operator stops computer operation, the computer stops after executing the I-sequence of the next instruction.

d. Function Circuits.

(1) F-register (figure 8-17, page 8-41). - The F-register holds the function-code portion of the instruction (bits 2^{19} through 2^{23}) while the instruction is being executed. The function code enters the register at time 3.3 of the I-sequence and remains in the register until time 3.2 of the following I-sequence when the register clears. The contents of the F-register are translated to form outputs that represent the various ranges. These outputs go to the translator. With the FUNCTION REPEAT switch in the up (FUNCTION REPEAT) position, the contents of the register do not change and the computer continuously executes the same instruction. The operator clears the F-register by pressing the MASTER CLEAR switch or the FUNCTION Clear pushbutton.

(2) Function code translator (figures 8-18 through 8-20, pages 8-43 through 8-47). - The function code translator consists of a network of AND and OR circuits that combine the F-register outputs into the enable signals necessary to control the execution of the instructions. Figure 4-17, page 4-49, shows typical translating circuits. The F-register supplies four inputs to these translating circuits.

The output of 30F31 is high when the F-register contains function code 31 (ADD); the output of 30F32 is high when the F-register contains function code 32 (SUB); and the output of 30F36 is high when the F-register contains function code 36 (ADB). When any of the three AND circuits (30F31, 30F32, 30F36) are enabled, OR circuit 50F31 generates a low output signal to transfer the contents of the adder to the A-register. When AND circuit 30F31 is enabled, it generates a high output to transfer the contents of the X-register to the D-register. When AND 30F36 is enabled, inverter 40F36

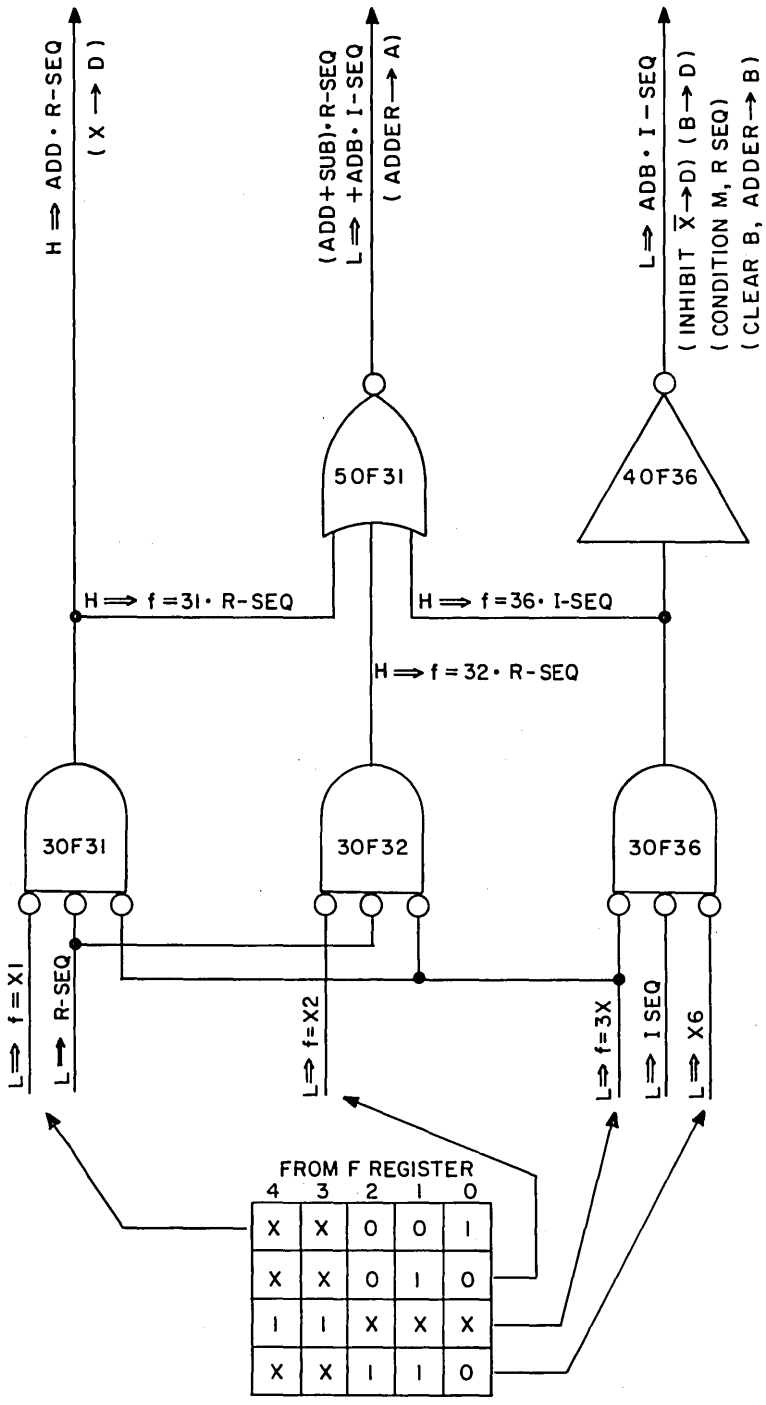


Figure 4-17. Typical Function Translation Circuit

generates a low output. This output inhibits the transfer of the complement of the X-register ($\overline{X}$) to the D-register, transfers the contents of the B-register to the D-register, conditions the M or R-sequences, or transfers the contents of the adder to the B-register.

e. Shift Circuits (figures 8-14, 8-14a, 8-15, and 8-15a, pages 8-31 through 8-37). - There are five different types of shift operations: left-shift, right-shift, multiply, divide, and scaling operands. Shifting is specified by instruction-word function code 06 (SHF). One of seven main categories is selected by the instruction-word sub-order (table 4-2, page 4-12).

(1) Shift left (SHL, 06-0). - The shift left operation is performed in one of two modes: the standard mode and the repeat-clear-add (RCA) mode. Figure 4-18, page 4-51, illustrates the shifting sequence for the SHL operations.

(a) Standard mode. - The standard mode of left shifting is performed if the mode bit (instruction-word bit 11) is a one or if the RCA flip-flop is clear. The instruction word specifies the type of shift (table 4-3, page 4-12) and the number of shifts (shift count, bits 0 through 4). The type and mnemonic codes for left shifting only the A-register are type 00 and 01, SCN and SAN. The type and mnemomic codes for left shifting the index register are type 10 and 11, SXN and SLN. All shifting sequences begin when shift control flip-flop 2 is set (at time 6.2). Setting this flip-flop stops the main timing chain.

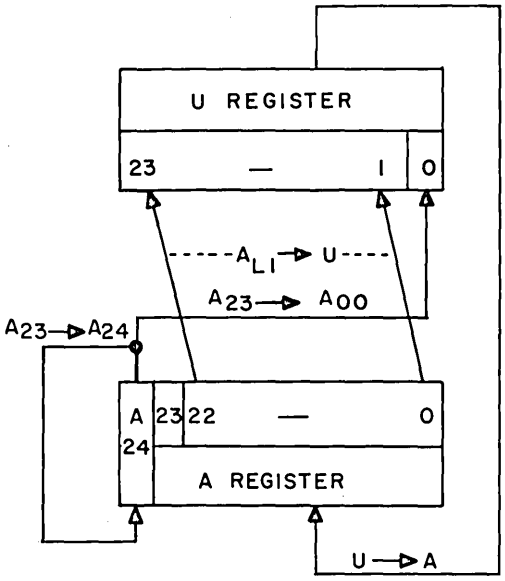
During the I-sequence (figure 4-19, page 4-52), the instruction is read from memory into the Z-register. The shift count (bits 0 through 4) is transferred from Z to the K-register. The index-register address (bits 14 through 18), which is used only for type 10 and 11 shifts, is loaded into the M-register. The type, mode, and sub-order portions of the instruction are set into the type, mode, and CAT flip-flops.

If the instruction is a type 10 or 11 (SXN or SLN), an R-sequence follows the I-sequence. (See figure 4-20, page 4-53.) The R-sequence reads the index register contents from memory into the Z-register and the X-register.

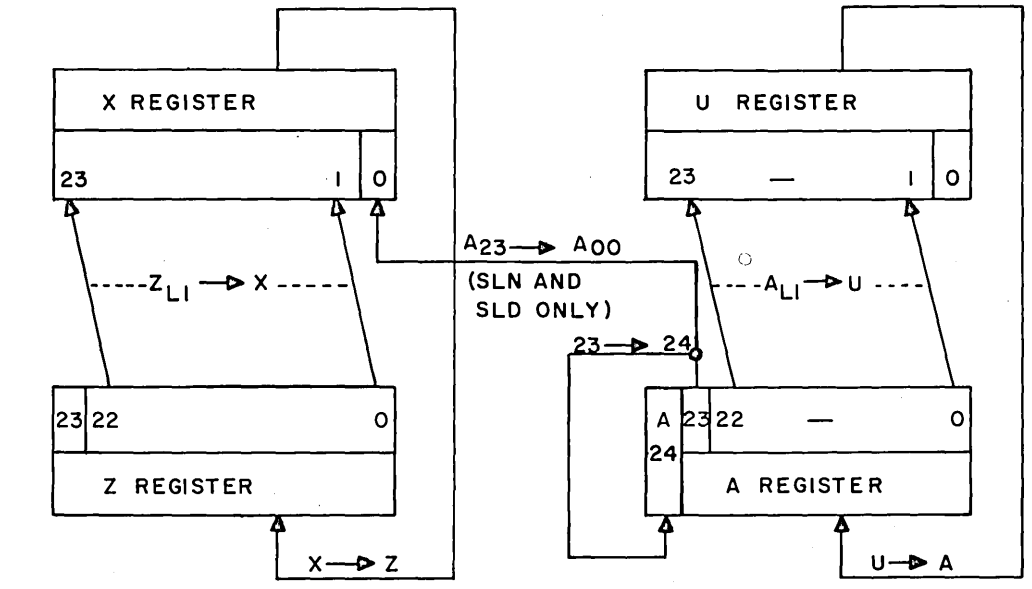
Shifting begins at the end of the I-sequence for a type 00 or 01 instruction and at the end of the R-sequence for a type 10 or 11 instruction. The A-register and/or the index register is shifted left one place and the K-register (shift counter) is decremented by one. K is tested for zero and, if not

OPERATION	FIG. 4-18;
SCN, SCD	A
SAN, SAD	B
SXN, SXD	C
SLN, SLD	B & C

NOTE: THE ABOVE CHART SHOWS THE OPERATIONS THAT USE THE DIFFERENT SHIFTING SEQUENCES ILLUSTRATED IN THIS FIGURE.



A. A-REGISTER END AROUND



C. INDEX REGISTER END OFF

B. A-REGISTER END OFF

Figure 4-18. Left Shifting Sequences

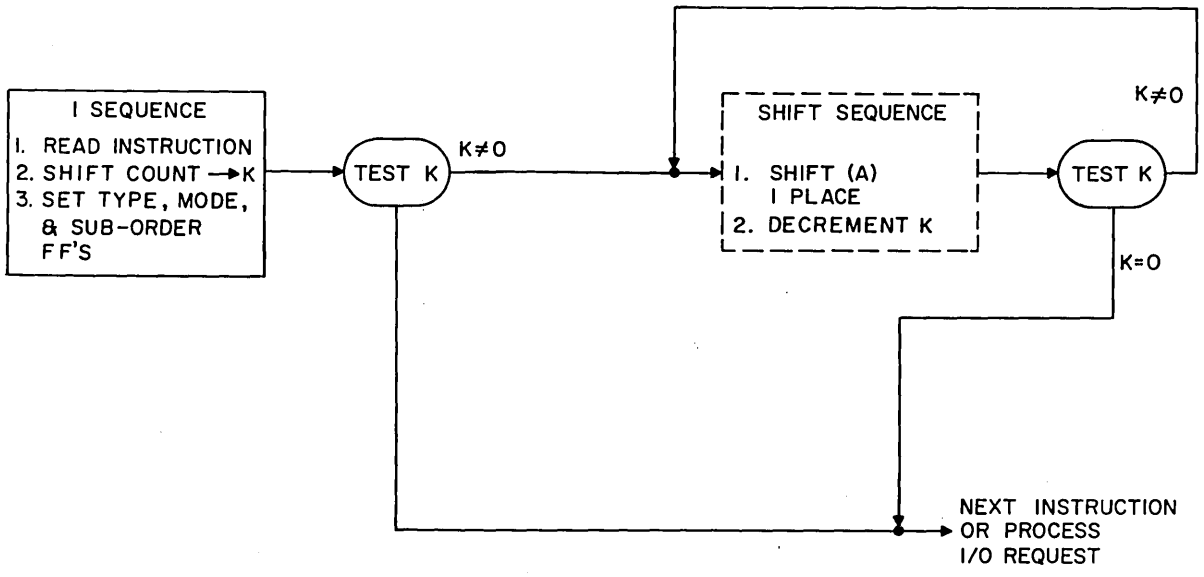


Figure 4-19. Standard Shift Mode, Type 00 or 01 (SCN, SAN, SCR, SAR) Flow Diagram

at zero, another shift is performed. When K reaches zero, indicating the specified number of shifts has been completed, the shifting stops, shift control flip-flops 1 and 2 are cleared, and the main timing chain takes over to execute the next sequence.

If the instruction was a type 10 or 11 (SXN or SLN), a W-sequence is performed to restore the shifted index-register contents to memory and the next I-sequence or I/O operation is enabled. For the SLN instruction, the shifted A-register contents remain in the A-register.

(b) RCA mode. - The RCA mode of shifting is initiated by an RCA (24) instruction, executed by an SHF (06) instruction, and terminated by an ERC (25) instruction.

1. Control word. - The RCA (24) instruction references the contents of a memory location and transfers the contents to memory location 00040. The data stored in memory location 00040 is the first RCA-mode control word (CW1). Memory location 00041 contains the second RCA-mode control word (CW2) (memory location 00041 is loaded by a

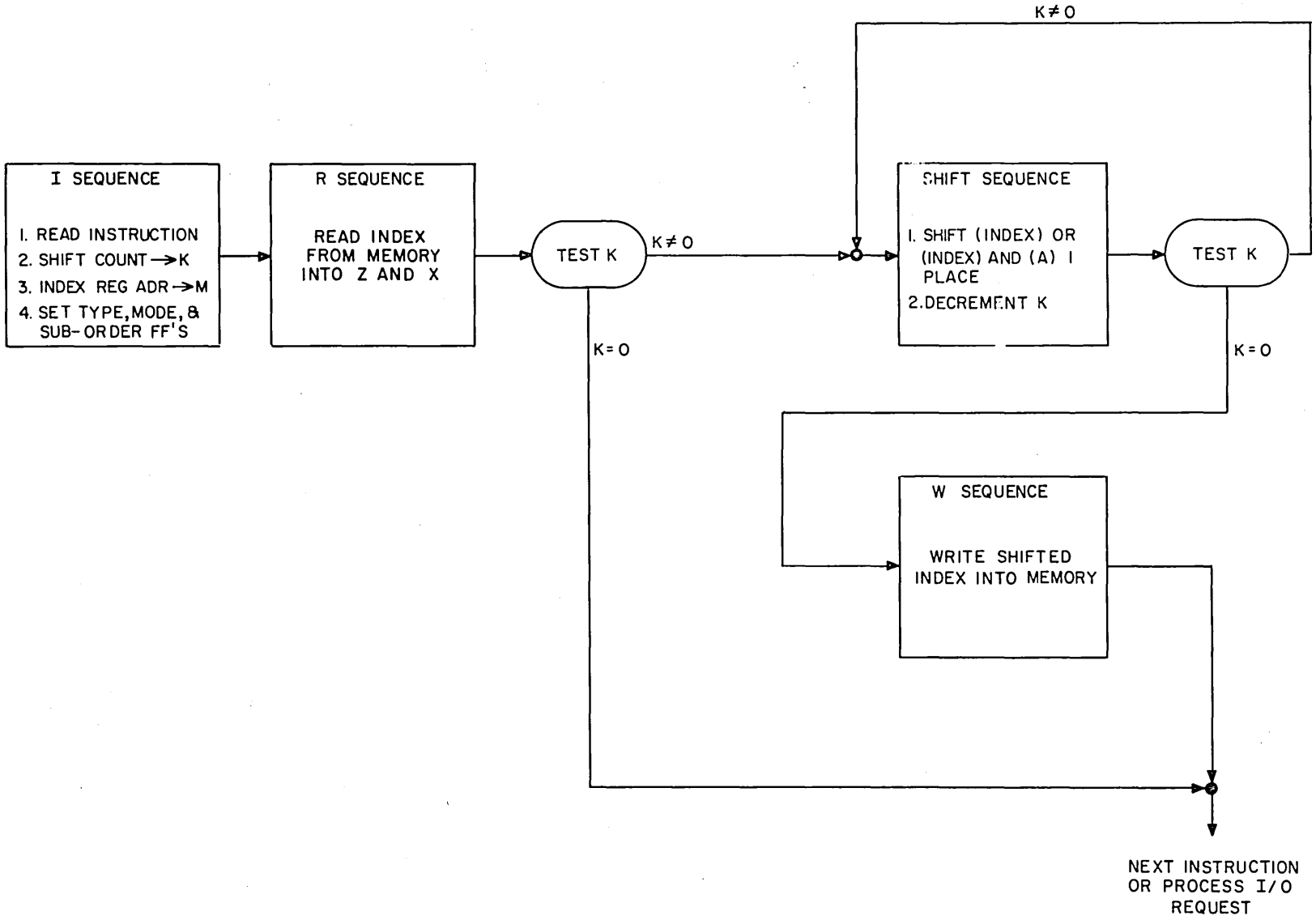


Figure 4-20. Standard Shift Mode, Type 10 or 11 (SXN, SLN, SXR, SLR) Flow Diagram

separate instruction and not by the RCA instruction). The RCA instruction sets the RCA-mode flip-flop, indicating that the shift instruction is to be executed in the RCA mode. Figure 4-21 shows the format of the RCA-mode control word.

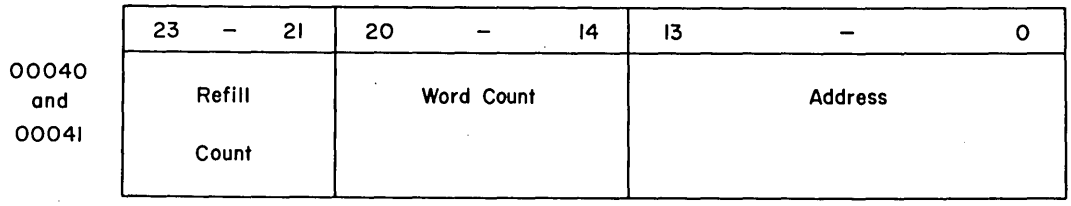


Figure 4-21. RCA-Mode Control Word Format

The RCA control word, which is referenced during the shift instruction, contains an address field (bits 0 through 13), a word-count field (bits 14 through 20), and a refill-count field (bits 21 through 23). The address field specifies the address of the first memory location to be shifted; the word-count field specifies the number of sequential memory locations to be shifted; and the refill-count field specifies the number of times each memory location is to be shifted. An LDX (27) instruction (with bits 9 through 13 = 0) loads the refill count (Y_{0-4}) into the RC-register.

2. Shift operation. - The RCA mode of left shifting is performed if the mode bit (instruction-word bit 11) is a zero and the RCA flip-flop is set (by a previous RCA instruction). The instruction word specifies the type of shift (table 4-3, page 4-12) and the number of shifts (shift count, bits 0 through 4). The type and mnemonic codes for shifting only the A-register are type 00 and type 01, SCD and SAD. The type and mnemonic codes for shifting the index register are type 10 and type 11, SXD and SLD. Figure 4-22, page 4-55, is a flow diagram of a left shift instruction in the RCA mode for type 00 or type 01 (A-register shifting only).

The I-sequence reads the instruction word from memory into the Z-register. The shift-count portion of the instruction is loaded from Z into the K-register. The type, mode, and sub-order portions of the instruction are examined and the appropriate flip-flops are set. The RC-register is examined to see if the refill count is at zero. If RC is zero, the RC1-sequence is performed. (The RC-register could have been loaded by a previous LRC instruction.)

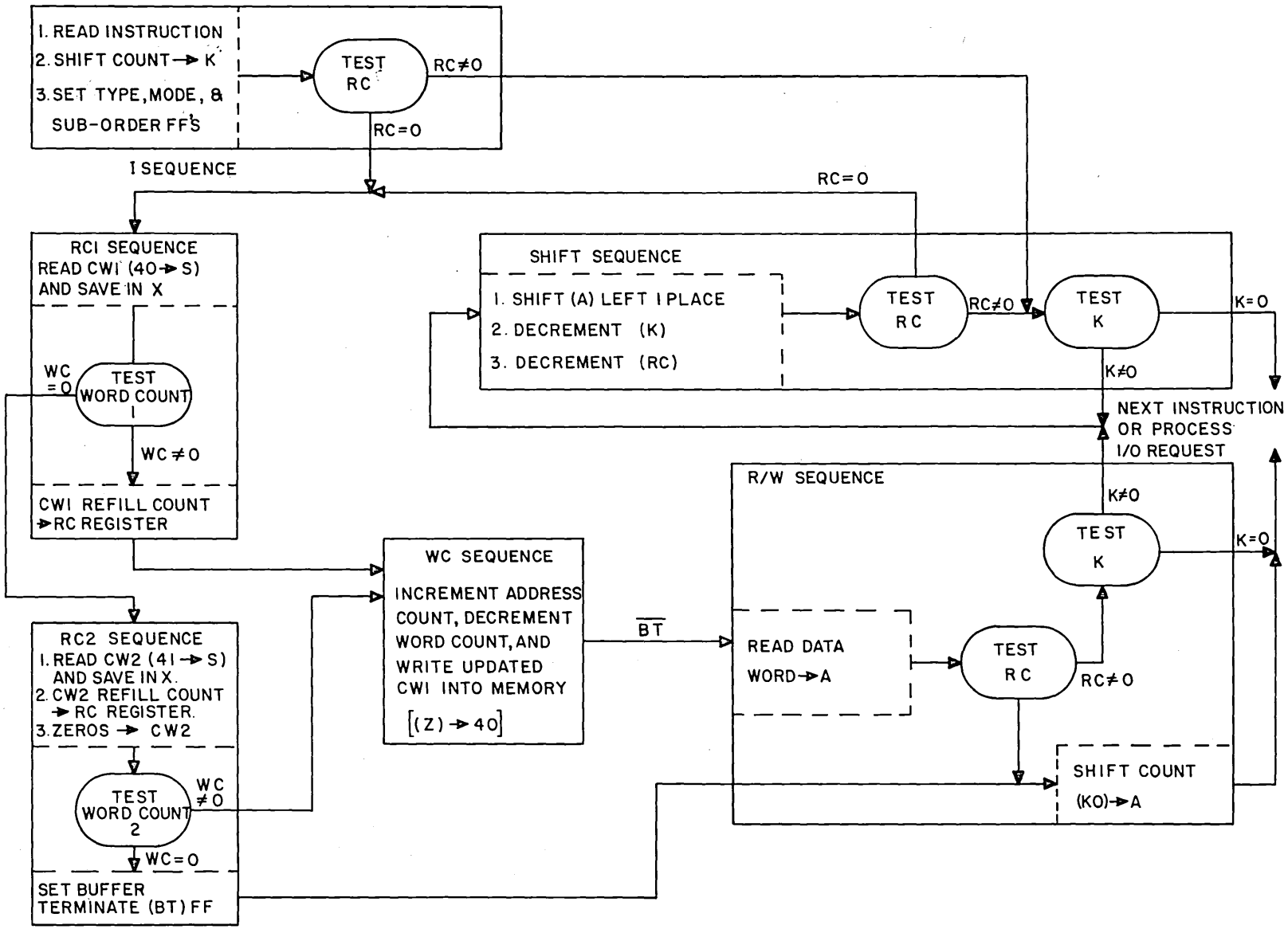


Figure 4-22. Shift Left, RCA-Mode (SCD, SAD) Flow Diagram

The RC1-sequence reads CW1 from memory. If CW1 word count (WC) is greater than zero, the refill count from the control word is loaded into the RC-register (upper three bits) and a WC-sequence is performed. The WC-sequence updates the control word (increments the address and decrements the word count) and loads it back in memory address 00040.

The R/W-sequence reads the data word to be shifted into the A-register. The memory address of the data word (specified by the control word) was stored in the X-register before the control word was updated. If the shift count in K is not zero, the data word in A is shifted left one place, and the shift count (K) and refill count (RC) are decremented. Shifting continues until one of them is decremented to zero.

If the shift-instruction shift-count in K reaches zero first, the instruction is complete. If the refill count reaches zero before, or at the same time as, the shift count, the RC1-sequence is performed. The RC-1 sequence reads the updated CW1 from memory. This control word contains the next sequential memory address of the data word to be shifted. If the word count of CW1 is not zero, CW1 is updated again and returned to memory address 00040 (by the WC-sequence). The new data word is loaded into A by the R/W-sequence and, if (RC) $\neq 0 \cdot$ (K) $\neq 0$, shifting continues.

When the CW1 WC reaches zero, the RC2-sequence is performed. RC2 reads CW2 from memory address 00041, stores it in the X-register, and clears address 00041. The CW2 refill count is placed in the RC-register, and the new word count is tested. If WC is zero, the buffer terminate (BT) flip-flop is set, the R/W-sequence is performed to transfer the shift count from K to the A-register, and the instruction is complete. If WC is not zero, the WC-sequence is performed and the updated CW2 is stored in location 00040.

Figure 4-23, page 4-57, is a flow diagram of a type 10 or 11 left shift instruction in RCA mode (SXD or SLD). The SXD or SLD shift instructions are the same as the SCD or SAD instructions with the following exceptions:

1) An R-sequence is performed immediately after the I-sequence. The index word specified by bits 14 through 18 of the instruction is loaded into the Z-register.

2) During the shift-sequence, the index word in the Z-register, or the index word and the A-register, are shifted.

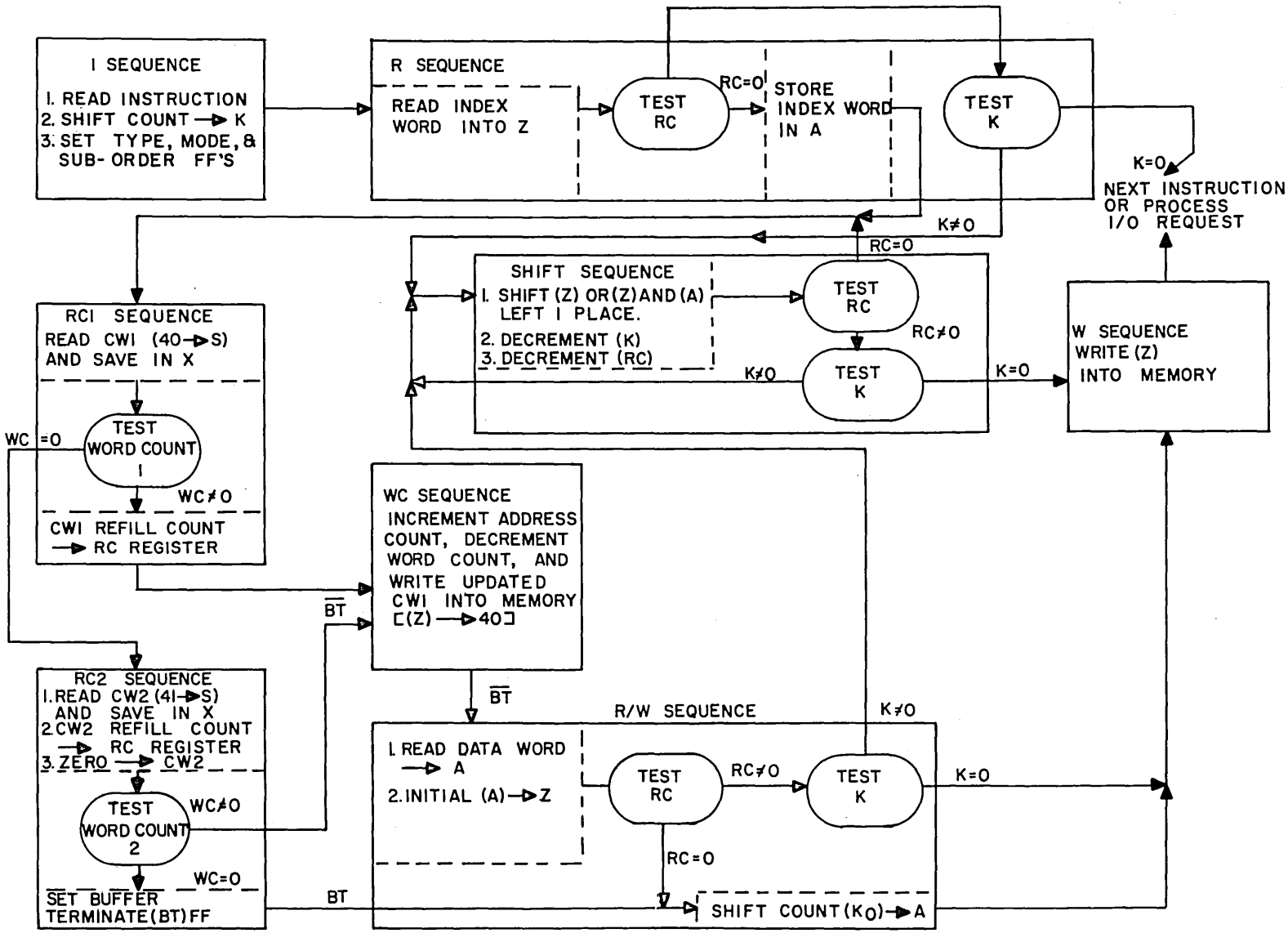


Figure 4-23. Shift Left, RCA-Mode (SXD, SLD) Flow Diagram

3) A W-sequence is performed at the completion of shifting to load the shifted index word back into memory.

The SLD instruction can be used to repack a new word from a memory buffer.

(2) Shift until different (SUD, 06-6). - The SUD operation left-shifts the contents of the A-register (loaded from the memory) until A_{23} and A_{24} are different. The SUD operation is similar to the shift left (SHL, 06-0) operation in RCA mode. The primary difference is that shifting continues until A_{23} and A_{24} are different instead of until the shift count reaches zero. The shift count portion of the instruction word is not used for the SUD operation. A number indicating the total number of shifts performed is stored in an index register at the end of the operation.

A control word, previously loaded into memory location 00040, is referenced during the SUD operation. The address field (bits 0 through 13) of the control word specifies the address of the first memory location to be shifted. The word count (bits 14 through 20) specifies the number of sequential memory locations to be shifted. The refill count (bits 21 through 23) specifies the number of times each memory location is to be shifted.

Figure 4-24, page 4-59, is a flow diagram of the SUD instruction. The I-sequence reads the instruction word from memory into the Z-register. The shift-count, type, and mode portions of the instruction are not used. The sub-order (110_2) portion is examined and the appropriate flip-flops are set. The memory address of an index register (bits 14 through 18) is stored in the M-register.

During the R-sequence, following the I-sequence, the specified index word is loaded into the Z-register. If the repeat count is zero, the index word is put into A, the initiate-SUD flip-flop is set, and the RC1-sequence is performed. If RC is not zero, A_{23} and A_{24} are tested and the shift-sequence is performed.

During the RC1-sequence, the first control word (CW1) is read from memory location 00040. The word count (WC) portion of CW1 is examined: if WC is zero, the RC2-sequence reads the second control word (CW2); if WC is not zero, the refill count (RC) portion of CW1 is loaded into the RC-register, and the WC-sequence is performed. The RC2-sequence reads CW2 from memory location 00041 and stores zeros in that location. The refill count portion of CW2 is loaded into the RC-register, and the word count

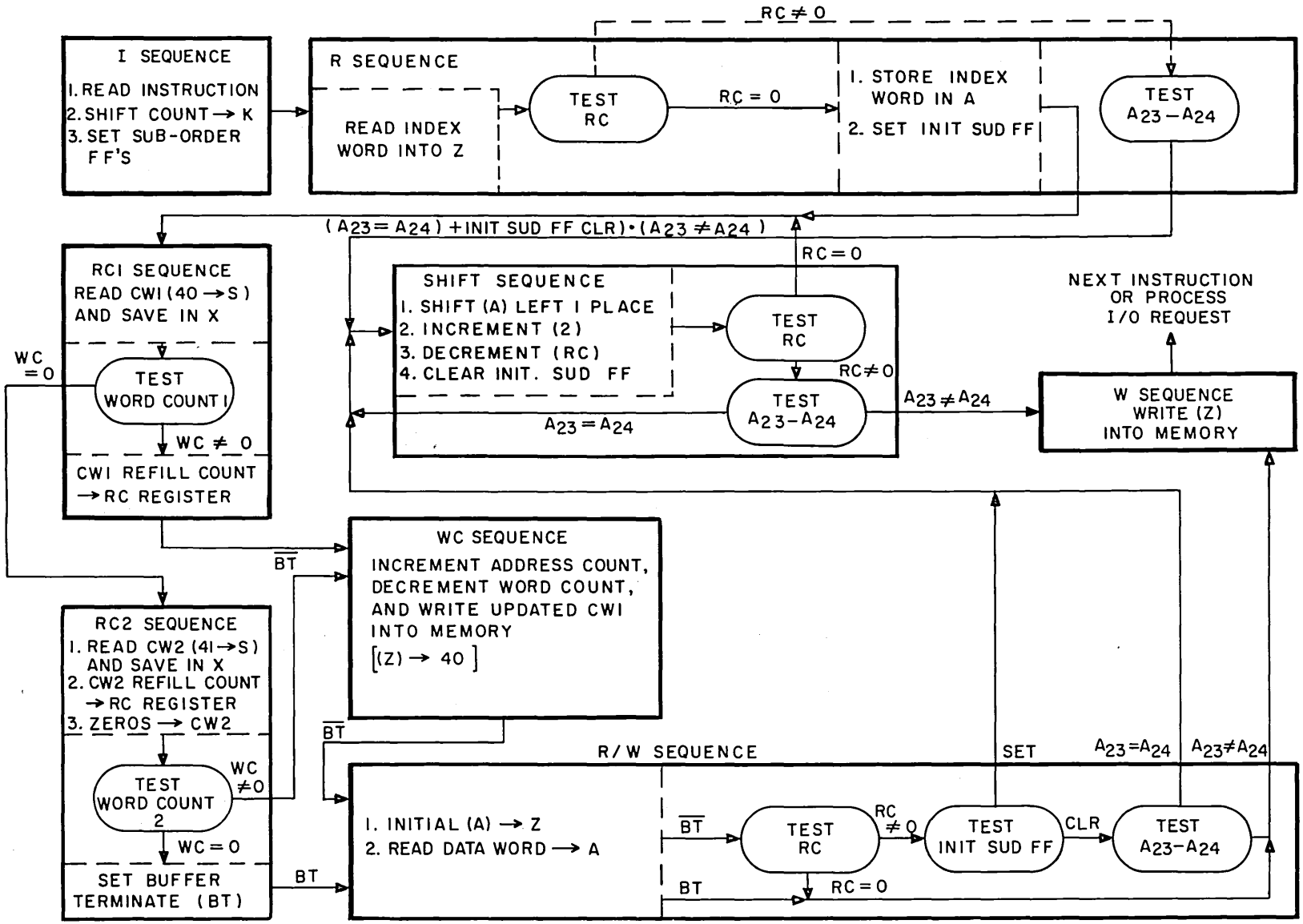


Figure 4-24. Shift Until Different (SUD), Flow Diagram

from CW2 is tested. If this word count is zero, the buffer terminate (BT) flip-flop is set and the R/W-sequence is performed. If the word count is not zero, the WC-sequence is performed before the R/W-sequence.

The WC-sequence updates the CW (increments address count and decrements WC) and restores it to the CW1 location in memory. The R/W-sequence reads the data word to be shifted from memory and loads it in the A-register, using the X-register which contains the CW with the non-incremented address, if the previous sequence was WC. If the previous sequence was RC2, the incremented address is used.

If (RC = 0) + BT + (INIT SUD FF clear) · ($A_{23} \neq A_{24}$), the W-sequence is performed and the operation is complete. The shift-sequence is performed if: (RC ≠ 0) · ($\overline{BT}$) · (INIT SUD FF set + $A_{23} = A_{24}$). The shift sequence adds one to the index word stored in Z for each shift. The RC-register is decremented, and RC and A_{23} and A_{24} are tested. (In actual logic implementation, the pre-shifted A_{22} and A_{23} are tested.) If RC is decremented to zero, the RC1-sequence is performed to read the updated CW1 from memory. The next sequential memory data word is loaded into A by the R/W-sequence, and the CW1 is again updated and placed back in 00040 by the WC-sequence.

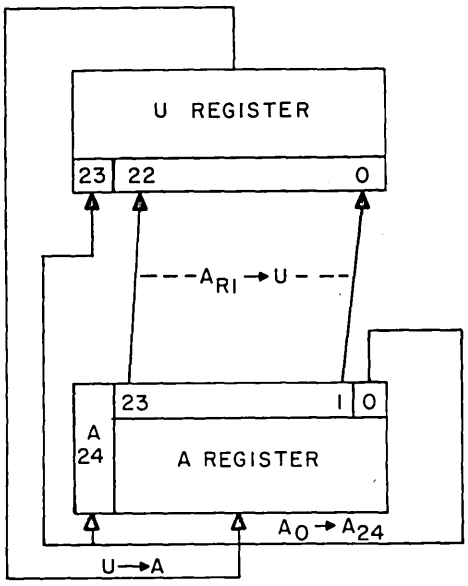
When a difference between A_{23} and A_{24} is obtained (equivalent to pre-shifted $A_{22} \neq A_{23}$), the W-sequence is performed to store the index word containing the number of shifts performed to its original memory location, and the operation is complete.

The SUD instruction is used to count the number of continuous ones or zeros in a memory buffer. An index register is used to register that number and therefore the index register, or index word, in a SUD operation has a different meaning as compared to the normal use of indexing (address modification) procedures.

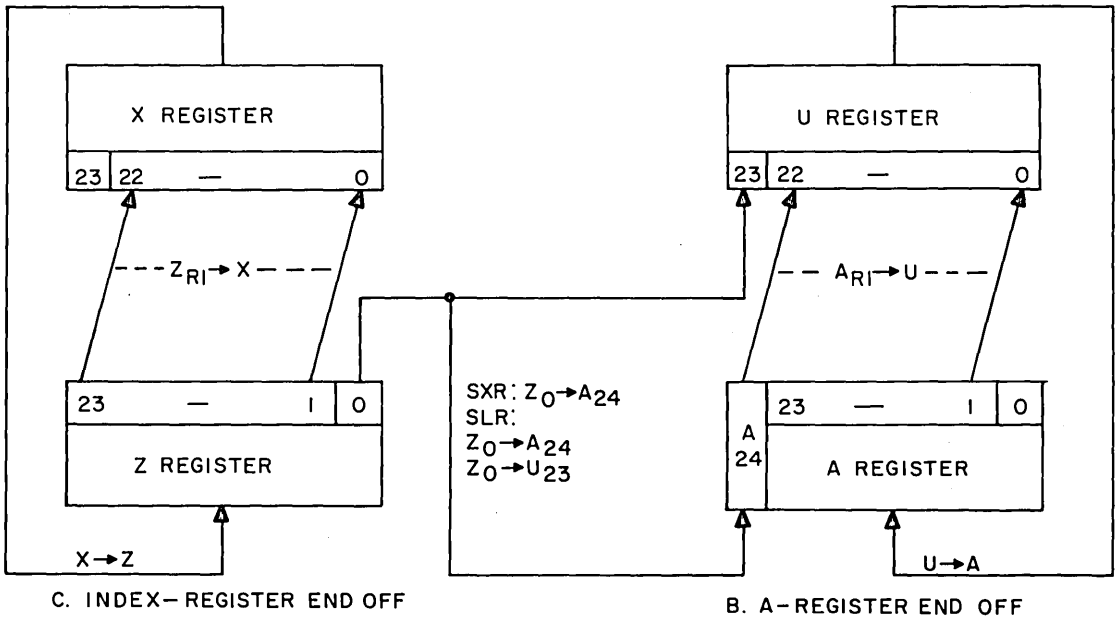
(3) Shift right (SHR, 06-4). - The shift right operation is performed in the standard mode only; the repeat-clear-add (RCA) mode is not used. The instruction word specifies the type of shift (table 4-3, page 4-12) and the number of shifts (shift count, bits 0 through 4). The type and mnemonic codes for right shifting only the A-register are type 00 and type 01, SCR and SAR. The type and mnemonic codes for shifting the index register are type 10 and 11, SXR and SLR. Figure 4-25, page 4-61, illustrates the shifting sequence for the SHR operations. The right-shift operation is performed in the same manner as the left-shift operation; refer to paragraph 4-16e(1)(a), page 4-50, and figure 4-19, page 4-52).

OPERATION	FIGURE 4-25
SCR SAR SXR SLR	A B C B AND C

NOTE: THE ABOVE CHART SHOWS THE OPERATIONS THAT USE THE DIFFERENT SHIFTING SEQUENCES ILLUSTRATED IN THIS FIGURE.



A. A-REGISTER END AROUND



C. INDEX-REGISTER END OFF

B. A-REGISTER END OFF

Figure 4-25. Right Shifting Sequences

(4) Scale accumulator (SCA, 06-2). - The scale accumulator operation shifts the contents of the accumulator (A-register) left until the two high-order bits are different. The number of shifts is limited by the instruction-word shift count; if the shift count is decremented to zero before a difference between the high-order bits is obtained, the shifting stops.

The index-register-address portion of the instruction word (bits 14 through 18) is not used for the SCA operation. A refill count (normally 24_{10}) is assumed to have been previously loaded into the repeat counter (RC-register), and the operand is assumed to have been previously loaded into the A-register.

During the I-sequence (figure 4-26, page 4-63), the instruction is read from memory into the Z-register and the sub-order portion of the instruction (010) is set into the appropriate CAT flip-flops. The shift count (K) is loaded with the five lower order bits of the instruction. A_{22} and A_{23} are tested at the completion of the I-sequence. If the operand in the A-register is already scaled, no shifting is performed, and the repeat counter is not changed; if the operand is not already scaled and the shift count is not zero, the shift sequence begins.

During the shift sequence, A is shifted left (circular) one bit into U, and the shifted contents of U are loaded back into A. The K and RC-registers are decremented by one. The decremented contents of K are tested for zero, and the shifted U_{22} and U_{23} are tested for difference. Shifting continues until K is decremented to zero or until the two high-order bits in the U register are different.

At the completion of the operation, the number of shifts performed is indicated by the difference between the initial and final contents of the repeat counter.

(5) Scale index and accumulator (SCL, 06-3). - This shift-instruction sub-order scales a 48-bit operand contained in the index register high-order 24 bits) and the accumulator (low-order 24 bits). The 48-bit operand is shifted left (cyclic) until bits 21 and 22 of the index register are different or the shift counter decrements to zero. See figure 4-27, page 4-63.

The index register to be scaled is specified by bits 14 through 18 of the instruction word. The accumulator (A-register) is assumed to have been previously loaded. A refill count (31_{10} maximum) is assumed to have been previously loaded into the repeat counter (RC-register). The shift count is specified by bits 0 through 4 of the instruction word.

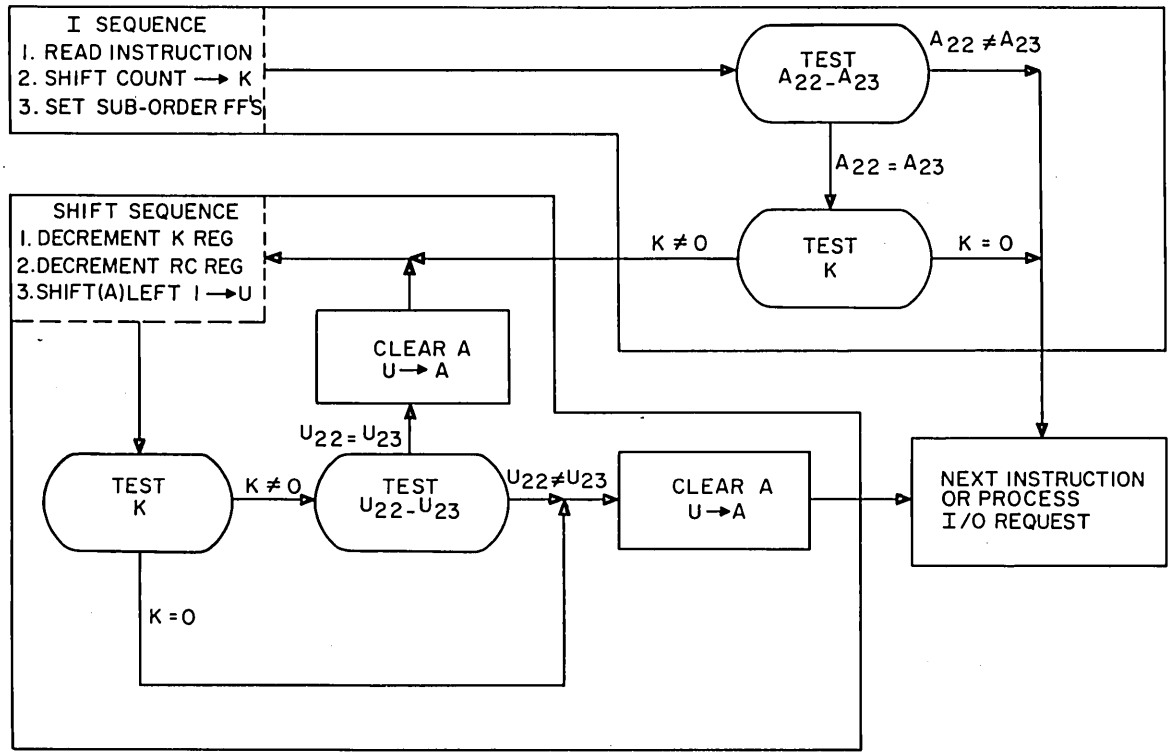


Figure 4-26. Scale Accumulator (SCA), Flow Diagram

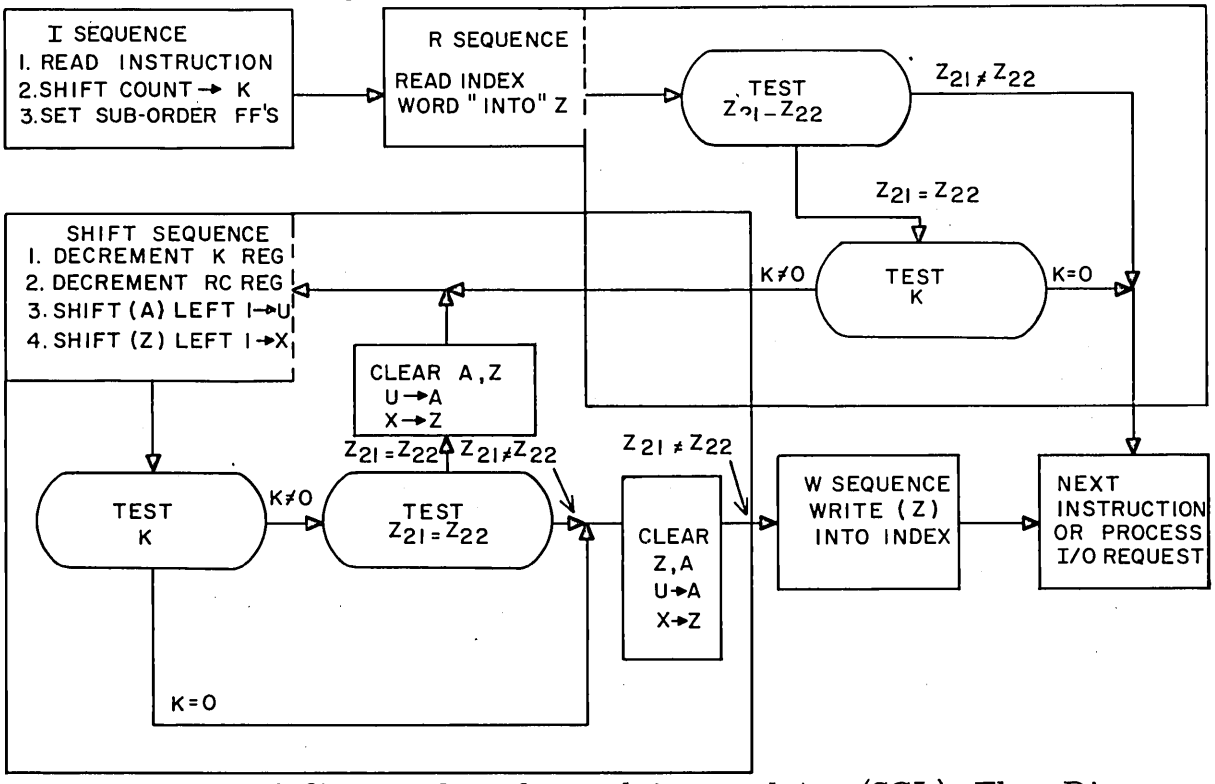


Figure 4-27. Scale Index and Accumulator (SCL), Flow Diagram

During the I-sequence (figure 4-28, page 4-65), the instruction is read from memory and the sub-order portion of the instruction (011) is set into the appropriate CAT flip-flops. An R-sequence is performed to load the specified index word into the Z-register. Z_{21} and Z_{22} are tested; if the operand in the Z-register is already scaled, no shifting is performed and the repeat counter is not changed. If the operand is not scaled, and the shift count is not at zero, the shift sequence begins.

During the shift sequence, A and Z are shifted left one bit (cyclic) and the K and RC registers are decremented by one. The shifted Z_{21} and Z_{22} are tested for difference (in actual logic implementation, the preshifted Z_{20} and Z_{21} are tested), and K is tested for zero. Shifting continues until K is decremented to zero or Z_{21} and Z_{22} are different.

At the completion of shifting operation, a W-sequence is performed to load the shifted index contents back into memory. The number of shifts performed is indicated by the difference between the initial and final contents of the repeat counter.

(6) Multiply (MUL, 06-5). - The multiply sub-order forms a 46-bit product of two 23-bit operands. The operands must be positive numbers (bit 23 a zero). One operand (the multiplier) is assumed to have been previously loaded in the A-register. The other operand (the multiplicand) is located in the index register specified by bits 14 through 18 of the instruction word. During the operation, the multiplicand is loaded into the D-register.

Multiplication is performed in the following manner. When the least significant bit of the multiplier (in the A-register) is zero, the partial product (in the Z-register) and the multiplier are shifted right one place without adding the multiplicand. When the least significant bit of the multiplier is one, the multiplicand is added to the partial product (in the Z-register) and then Z and A are shifted right one place. This procedure is repeated 24 times (until K decrements from 24 to 0). The resulting product is in the Z and A-registers.

Figures 4-28 and 4-29, pages 4-65 and 4-66, illustrate the multiply operation. The I-sequence reads the instruction, loads the shift count portion of the instruction in the K-register, and sets the appropriate sub-order flip-flops. The R-sequence is performed after the I-sequence to read the multiplicand from an index register and put it in the D-register. The shift count and A_0 are tested; and, since at this time the Z-register still holds the multiplicand for $A_0 = 0$ condition, Z is cleared before shifting is performed.

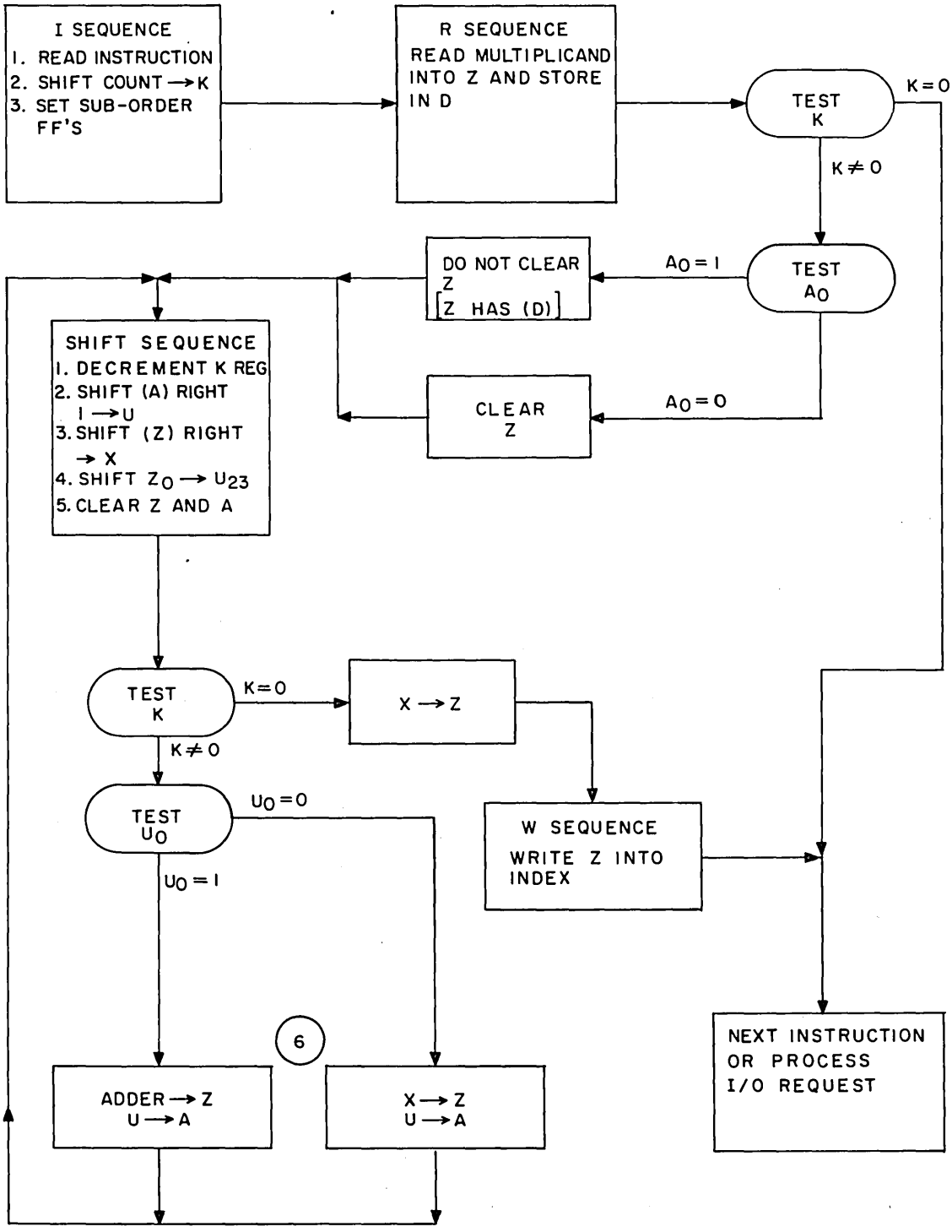


Figure 4-28. Multiply (MUL), Flow Diagram

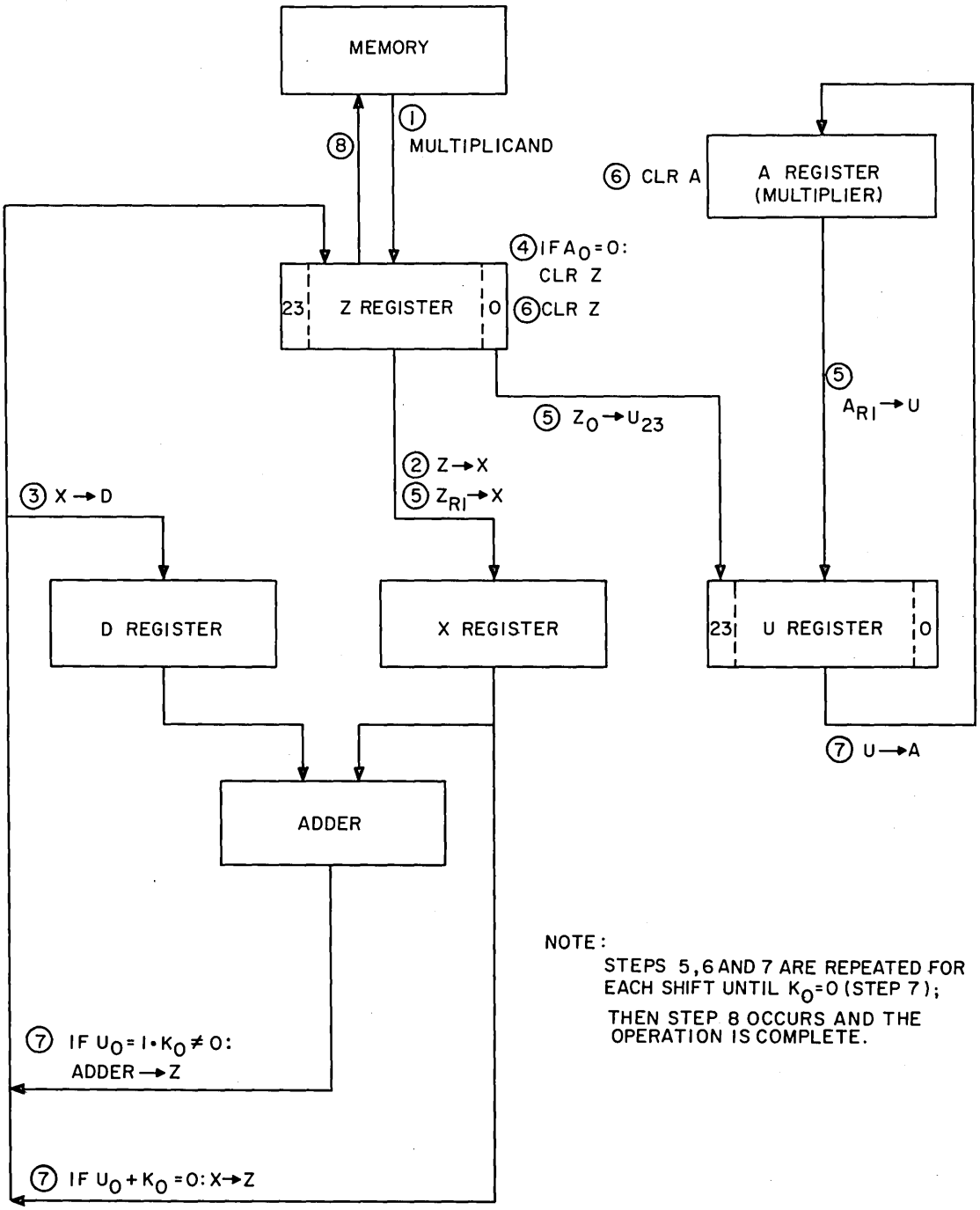


Figure 4-29. Multiply (MUL) Operation Shifting Sequence

If $A_0 = 1$, Z is shifted without clearing (the multiplicand is already added to the original partial product, which is zero).

During the shift-sequence, Z and A are shifted right one place into X and U, respectively, and Z_0 is shifted to U_{23}. K and A_0 ($U_0 = A_0$) are tested again; and, if $K \neq 0$ and $U_0 = 0$, the partial product (in the X-register) is loaded into Z without adding the multiplicand. If $K \neq 0$ and $U_0 = 1$, the sum (in the adder) of the partial product and the multiplicand is loaded into Z. The contents of U are always loaded into A. This process continues until the K-register decrements to zero (normally 24_{10} shifts). The resulting product is contained in Z and A. The contents of Z (the high-order 22 bits of the product) are loaded back into the original index register from which the multiplicand was obtained. The low-order 24 bits of the product remain in the accumulator (A-register).

(7) Divide (DIV, 06-1). - The divide sub-order divides a 46-bit operand by a 23-bit operand and forms a 23-bit quotient plus a 23-bit remainder. All operands must be positive numbers. The low-order 24 bits of the dividend are presumed to have been previously loaded into the accumulator (A-register). The high-order 22 bits of the dividend are located in the index register specified by bits 9 through 13 of the instruction word. The divisor is located in the register specified by bits 14 through 18 of the instruction word.

Division is performed in the following manner. For each step of division, the dividend (in the Z and A-registers) is shifted left one position. The high-order bits (in the Z-register) are shifted left into the X-register, and the low-order bits (in the A-register) are shifted left into the U-register. The shifted contents of Z are compared with the divisor. If they are less than the divisor, the shifted dividend is loaded back into the Z and A-registers, and the lowest-order bit of the dividend (A_0) is set to zero. If the high-order bits (Z-register contents) are equal to or greater than the divisor, the divisor is subtracted from the shifted dividend, and the result is loaded back into the Z and A-registers. Bit A_0 is set to one.

Figures 4-30 and 4-31, pages 4-68 and 4-69, illustrate the divide operation. The I-sequence reads the instruction, stores the shift-count portion of the instruction in the K-register, and sets the appropriate sub-order flip-flops. The address of the index register containing the divisor (bits 14 through 18) is stored in the M-register, and the address of the index register containing the high-order bits of the dividend is stored in the X-register. The contents of the M-register are examined; if they are not zero, an M-sequence is performed.

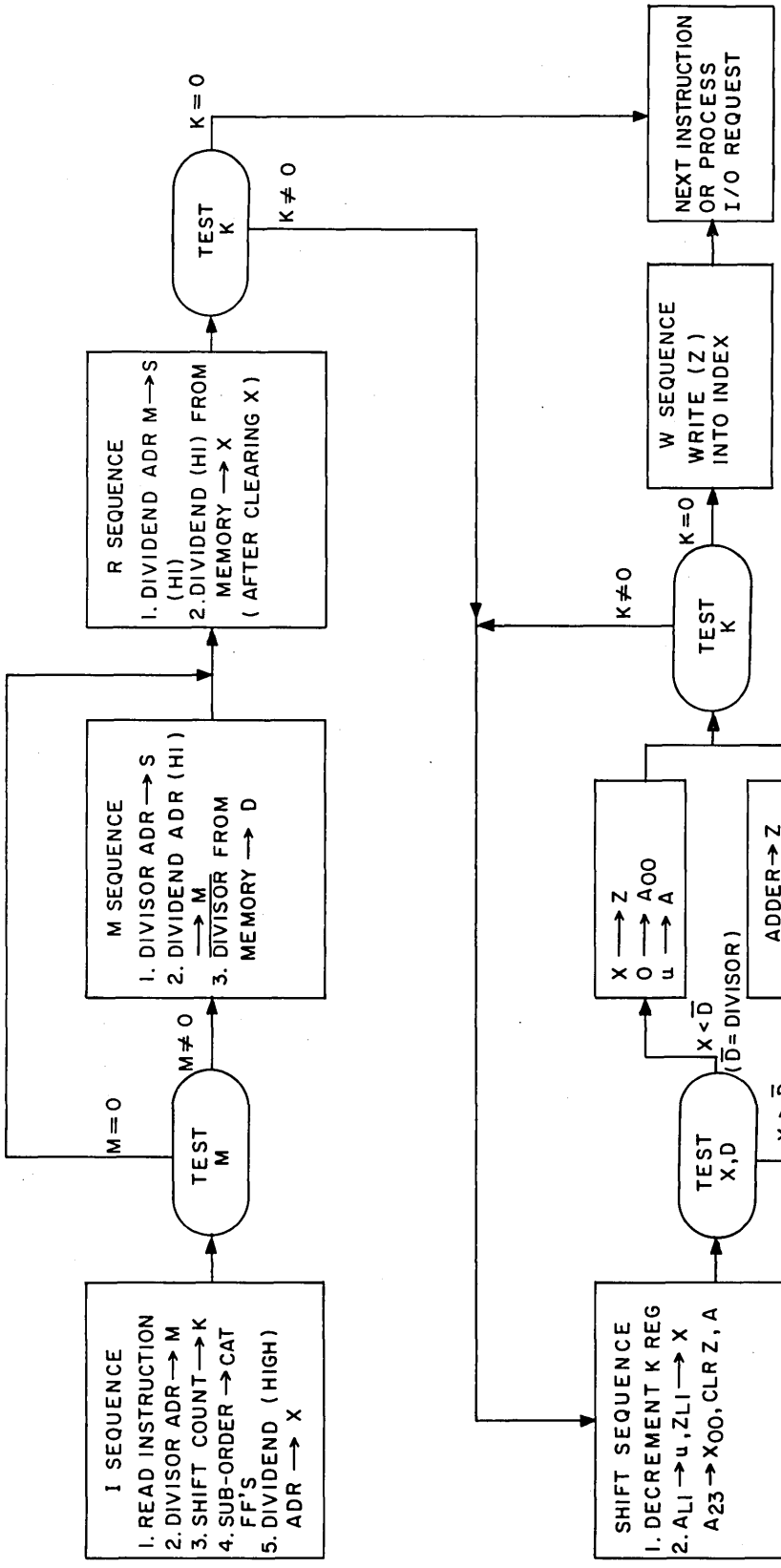


Figure 4-30. Divide (DIV), Flow Diagram

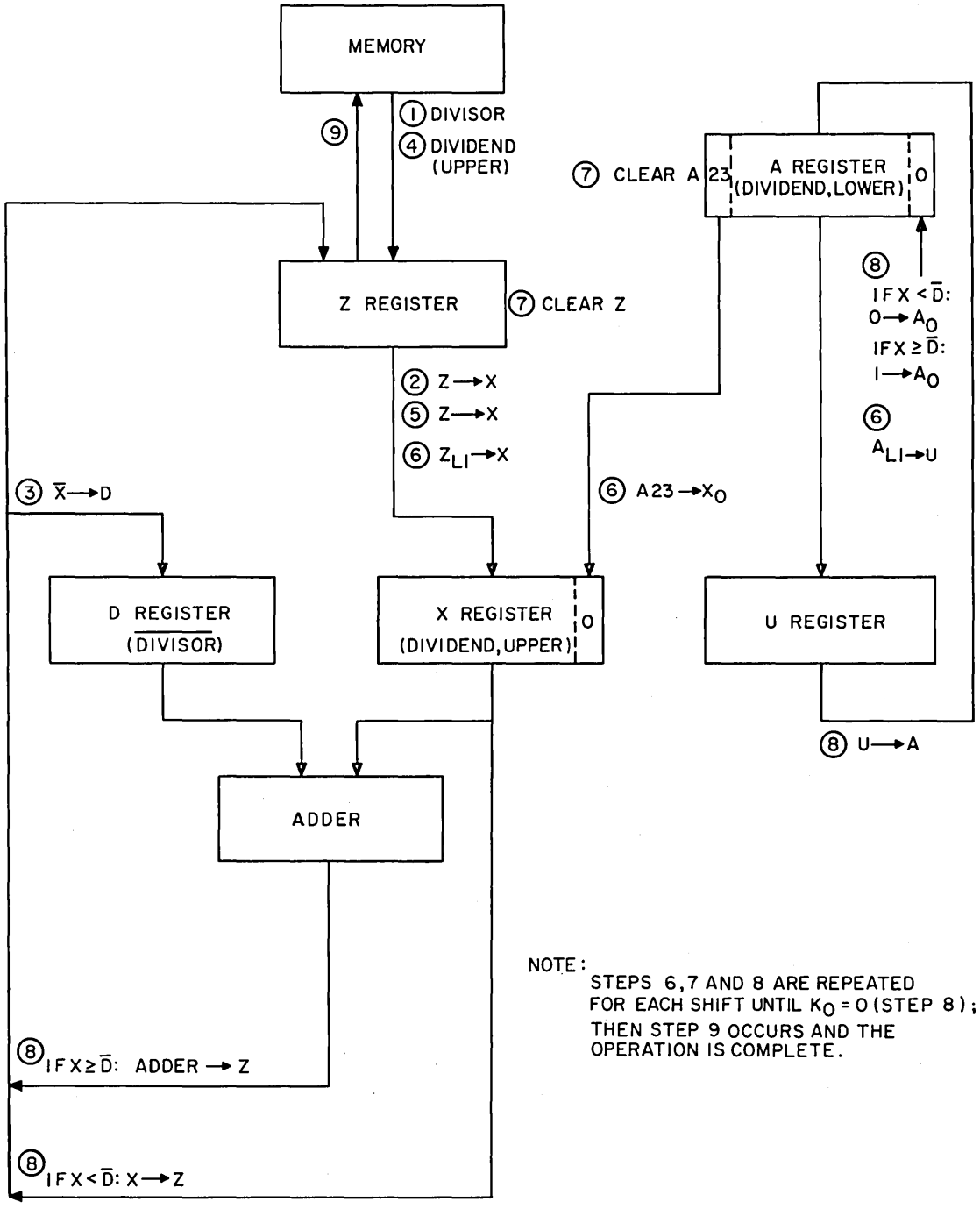


Figure 4-31. Divide (DIV) Operation Shifting Sequence

The M-sequence references the address in the M-register and reads the divisor from memory. The complement of the divisor is stored in the D-register. The address of the high-order half of the dividend is loaded into the M-register.

The R-sequence, which follows the M-sequence, references the address of the high-order half of the dividend (now in the M-register) and reads it from memory. The shift count is tested; and, if it is not zero, the shift sequence is performed.

The shift sequence decrements the shift count by one and performs one subtraction step. The low-order half of the dividend in the A-register is shifted left to the U-register and loaded back in the A-register. The high-order half of the dividend in the Z-register is shifted left into the X-register. If the contents of the X-register are equal to or greater than the divisor, the D-register contents are added to the X-register contents and a one is set into A_0. Since the D-register contained the complement of the divisor, the result is to subtract the divisor from the dividend. The adder contents are then loaded back into the Z-register. If the contents of the X-register are less than the divisor, the shifted X-register contents are loaded back into the Z-register and a zero is set into A_0.

The decremented shift count is tested after each shift-sequence. If the shift count (K) is not equal to zero, another shift-sequence is performed. When the shift count is decremented to zero, a W-sequence is performed. The W-sequence writes the Z-register contents (now the remainder) into the memory location that originally contained the high-order bits of the dividend. The A-register now contains the 23-bit quotient.

(8) Shift function register (figures 8-14 and 8-14a, pages 8-31 and 8-33). - The shift function register stores the type, mode, and sub-order portions of the shift instruction (06). The three CAT flip-flops (figure 8-14, page 8-31) and their associated circuits receive instruction-word bits 5, 6, and 7 from the Z-register, store this data in the flip-flops, and decode the sub-order. Table 4-2, page 4-12, lists the seven sub-orders.

The two type flip-flops (figure 8-14a, page 8-33) and their associated circuits receive instruction-word bits 12 and 13 from the Z-register, store this data in the flip-flops, and decode the type shift. The four types, and the sub-orders in which they are used, are listed in table 4-3, page 4-12. The mode flip-flop is controlled by bit 11 of the shift instruction. When it

is set, the repeat counter is not decremented. Shifting stops when the K-register (shift counter) reaches zero. If the mode flip-flop is cleared, the repeat counter is decremented; when it reaches zero, the reload sequence starts.

(9) Shift control (figures 8-15 and 8-15a, pages 8-35 and 8-37). - Shift control consists of a group of flip-flops and associated circuits that control the shift operations. Two shift-control flip-flops and two shift-cycle flip-flops form a shift timing chain. Outputs from these flip-flops generate enable signals that transfer the data to be shifted through the various registers. The two shift-cycle flip-flops are used only for the multiply, divide, and shift-until-different shift operations.

The bits-different flip-flop is set during the SUD operation when the two high-order bits in the accumulator are different; this clears the shift control flip-flops to stop shifting. The bits-different flip-flop is also set during the SCL operation when bits 45 and 46 of the 48-bit operand are different; this sets the W-sequence and inhibits the I-sequence. The initiate-SUD flip-flop is set during the R-sequence of a SUD operation or an RCA type 1X shift operation when the repeat counter equals zero; this enables setting shift-control flip-flop 1.

The reload request flip-flop is set when refill-count is zero during either a type 0X shift-left instruction in RCA mode (SCD, SAD) or a SUD instruction. The reload-request flip-flop enables the RC1-sequence. The reload flip-flop is set during the RC1-sequence to provide enables for the RC2, R/W, and W-sequences.

The RCA flip-flop sets when the repeat-clear-add instruction (24) is executed and remains set until an end-repeat-count instruction (25) is executed, the word count of the second RCA-mode control word equals zero, or the refill count in an RCA-control word is zero. Outputs from the RCA flip-flop control the repeat counter and also indicate to shift control that the RCA operation can be performed.

(10) Shift counter (figures 8-21a and 8-22, pages 8-51 and 8-53). - The shift counter (K-register) is a five-bit, double-rank decremental counter. The K-register holds the five-bit shift count specified in the shift instruction. The shift count enters the K-register during the I-sequence of the shift instruction. The register contents are decremented by one each time a shift is performed. The K-register outputs go to the shift control logic to indicate when the counter is equal to zero and when it is not equal

to zero. The K-register enables (figure 8-21a, page 8-51) generate the signals to clear and load the shift counter.

(11) Repeat counter (figures 8-21a and 8-23, pages 8-51 and 8-55).- The repeat counter (RC-register) is a five-bit, double-rank decremental counter. During the shift-left (06-0) instruction in RCA mode and the shift-until-different (06-6) instruction, the RC-register holds the refill count specifying the number of times each memory location is to be shifted. During the scale accumulator (06-2) and scale index and accumulator (06-3) instructions, the previously filled counter is used to indicate the number of shifts performed.

The RC-register is loaded with the lower five bits of the 27 (LDX) instruction when no index or B-register is specified, or with the refill-count portion of the RCA-mode or SUD shifting control word. The RC-register is decremented by one each time a shift is performed during the 06-0, 06-2, 06-3, and 06-6 instructions. Outputs from the repeat counter go to the shift control logic to indicate when the counter is equal to zero and when it is not equal to zero. Other outputs from the counter go to the Z-register and are stored in memory during a 26 (STX) instruction when no index register is specified (bits 9 through 13 = 0).

The RC-register enables (figure 8-21a, page 8-51) generate the signals to clear and load the repeat counter.

f. Address Circuits. - The address circuits consist of four registers (S, P, M, and B) and their associated enable circuits. The registers, along with the arithmetic and input/output sections, generate and temporarily store memory addresses. There are five types of memory addresses generated and/or stored by the address circuits: instruction, instruction operand, index register, I/O control word, and input/output.

The instruction address is the address of the next instruction to be executed. The instruction operand address is the address of the location where instruction information is to be read from or stored. The index register address is the address of one of the 37_8 index registers. The I/O control word address is the address of the I/O control word for the peripheral equipment that wants to send or receive data. The input/output address (specified by the I/O control word) specifies where input data from peripheral equipment should be stored and from where output data for peripheral equipment should be removed. Figure 4-32, page 4-73, is a block diagram of the address circuits.

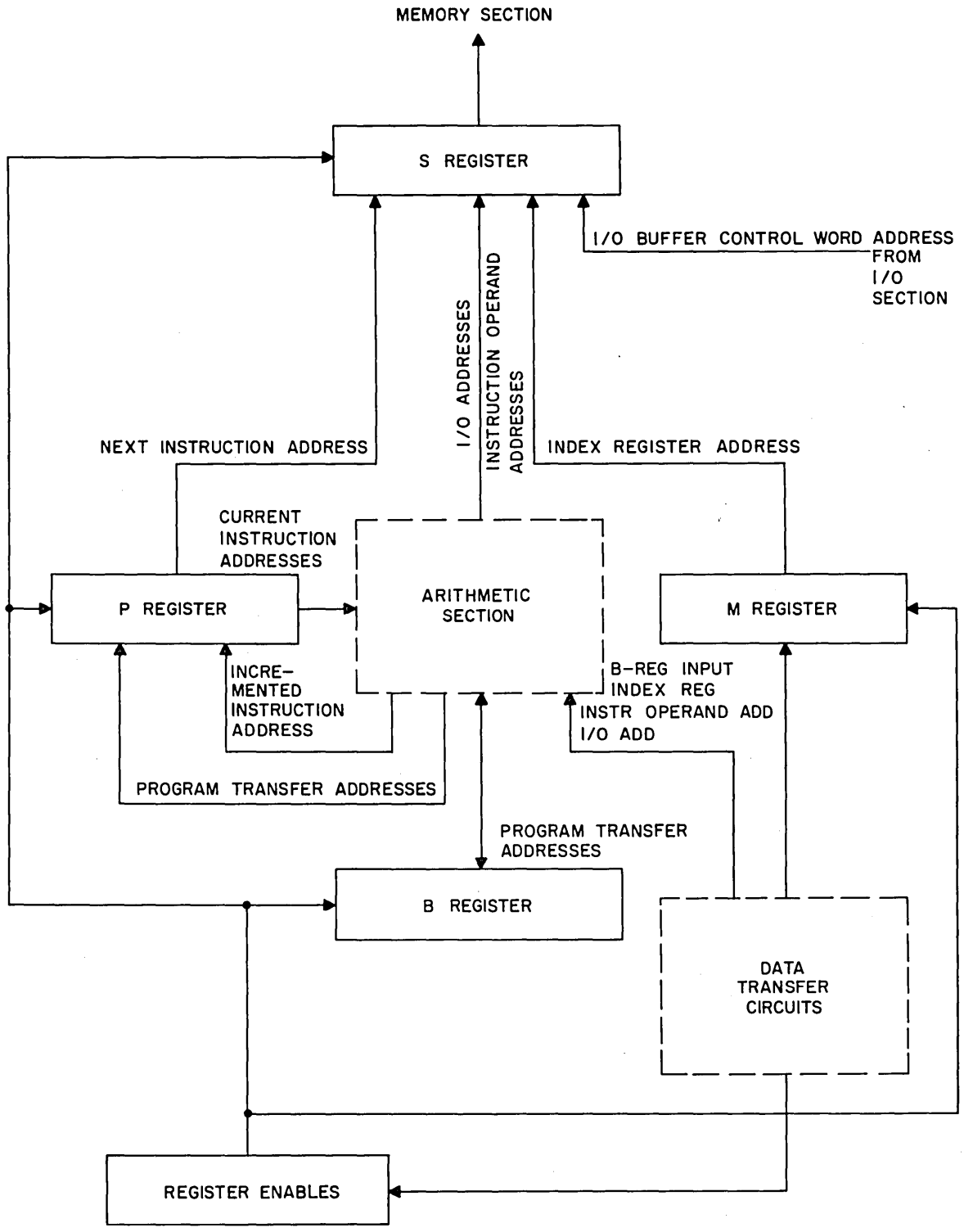


Figure 4-32. Address Circuits

(1) S-register (figures 8-29 through 8-31, pages 8-67 through 8-71). - The S-register is the 14-bit memory address register. The S-register receives instruction addresses from the P-register, input/output and instruction operand addresses from the arithmetic section, index register addresses from the M-register, and I/O buffer control words from the input/output section. The S-register contents go to the memory section for translation. S-register-enable circuits (figure 8-29, page 8-67) generate the signals to clear and load the S-register.

(2) P-register (figures 8-24 through 8-26, pages 8-57 through 8-61). - The P-register is the 14-bit program address register which holds the address of the next instruction. The P-register receives the next instruction address from either of two sources. When a program transfer instruction is executed and the transfer condition is satisfied, the P-register receives the next instruction address from the D-register in the arithmetic section. The D-register receives the address from the data transfer circuits; refer to paragraph 4-17a(2), page 4-85. When no program transfer condition exists, the P-register receives the next instruction address from the adder in the arithmetic section. The adder increments the current instruction address. The P-register contents go to the S-register and the X-register in the arithmetic section. The input to the S-register is the next instruction address. This address also goes to the X-register to be incremented and returned to the P-register. The P-register-enable circuits (figure 8-24, page 8-57) generate the signals to clear and load the P-register.

(3) M-register (index) (figure 8-21, page 8-49). - The 5-bit M-register holds the address of the index register specified by an instruction. The M-register receives the 5-bit address via the Z-register when the instruction is read from memory. The index register address goes to the S-register during the M-sequence. Then, when the index register contents are read from memory, they go to the arithmetic section via the data transfer circuit. In the arithmetic section the contents of the index register are added to an instruction operand address. This address then goes from the arithmetic section to the S-register as an instruction operand address. The M-register-enable circuits (figure 8-16, page 8-39) generate the signal to clear and load the M-register.

(4) B-register (figures 8-24, 8-27, and 8-28, pages 8-57, 8-63, and 8-65). - The 14-bit B-register holds a value referenced by some instructions to modify an instruction operand address. The register receives

the modifying value from memory via the data transfer circuits and arithmetic section. When an instruction references the B-register, the arithmetic section adds the B-register contents to an instruction operand address. This address then goes to the S-register as an instruction operand address. The B-register-enable circuits (figure 8-24, page 8-57) generate the signals to clear and load the B-register.

(5) Register enable circuits. - The register-enable circuits control the inputs to the address registers. Figure 4-33, page 4-76, shows the logic to clear P and load P with the contents of the D-register. During the W-sequence of the 03 (TSR) instruction, AND circuit 07N02 is enabled. The P-register clears at time 2.2 of the W-sequence and, at time 2.3, is loaded with the contents of the D-register. During the R-sequence of a 04 (TRX) or 05 (TAX) instruction when bits 14 through 23 of the Z-register are not equal to zero, AND circuit 05N22 is enabled. The P-register clears at time 3.2 of the R-sequence and, at time 3.3, is loaded with the contents of the D-register. The instruction timing charts in paragraph 4-21, page 4-171, show the time and sequence for the clearing and loading of the address registers during each instruction.

g. Data Transfer Circuits. - The data transfer circuits distribute information read from memory to other computer circuits and peripheral equipment, and collect information from computer circuits and peripheral equipments to store in memory. The data transfer circuits also add correct parity to the data stored in memory and then check the parity of all data read from memory. The data transfer circuits consist of the Z-register, selector, and parity circuits.

(1) Z-register (figures 8-54 through 8-58, pages 8-123 through 8-131). - The 24-bit Z-register is a memory input/output register. All data read from memory enter the Z-register. The Z-register also receives data from the X-register, the RC-register, and the adder. The data goes to memory via the selector.

The Z-register distributes data read from memory to the registers and circuits shown in figure A-3, page A-7. A of figure A-3, page A-7, shows the Z-register outputs going to the C-register during 8-bit output data transfers to various peripheral equipments. B of figure A-3, page A-7, shows the Z-register outputs going to the C-register during 6-bit output data transfers. C of figure A-3, page A-7, shows the Z-register outputs to the F, M, and K-registers when the Z-register holds an instruction

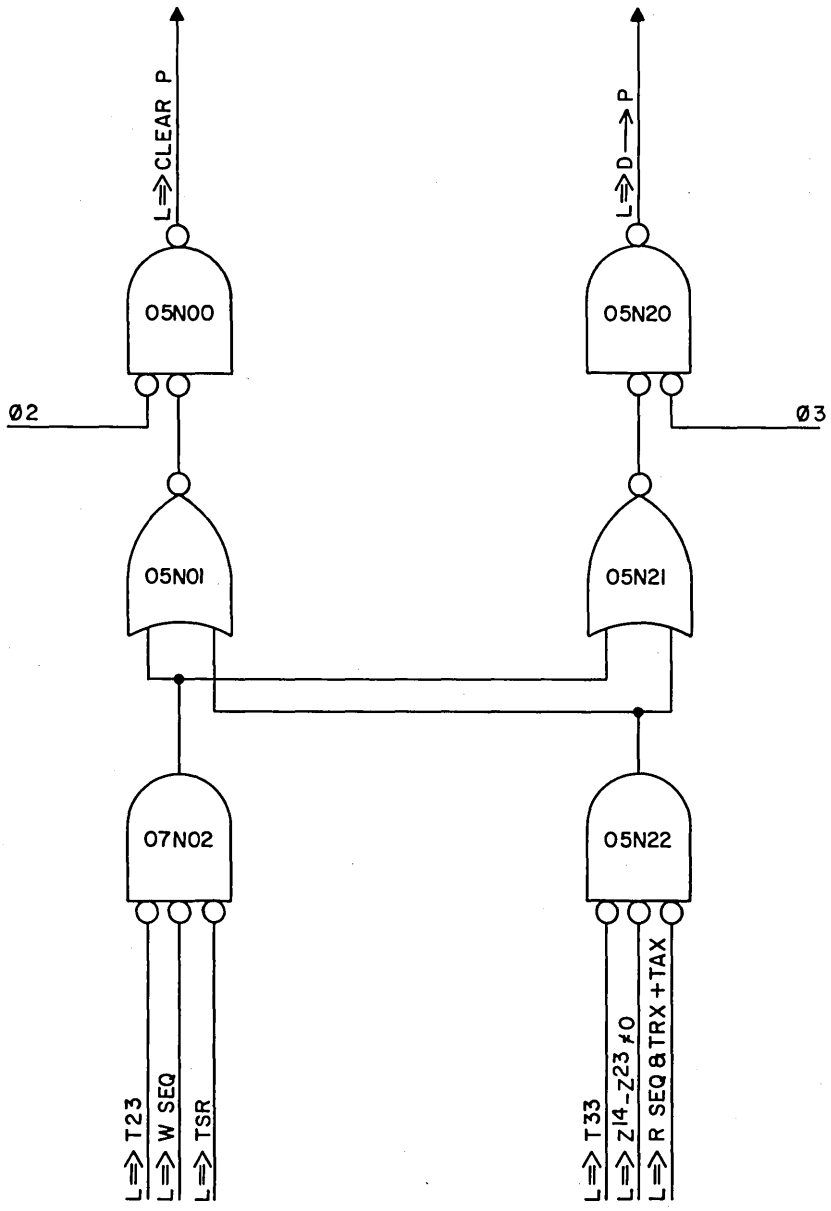


Figure 4-33. Typical Register Enable Circuit

word. D of figure A-3, page A-7, shows the Z-register outputs to the RC-register for the 27 (LDX) instruction, the paper tape unit enables for the 07 (EXF) instruction, the shift type and mode flip-flops for the 06 (SHF) instruction, and the sequence-enable and console-data-terminate circuits when console serial data input is performed. E of figure A-3, page A-7, shows Z-register outputs to sensing circuits. These circuits constantly check the contents of bits 14 through 23 of the Z-register and indicate the following.

1) Index address = 0
2) Index address = 37
3) Word count = 0
4) $Z_{14} - Z_{23} \neq 0$

F, G, and H of figure A-3, page A-7, show the Z-register outputs to the selector for left-shifting, right-shifting, or transferring Z-register data to memory without shifting.

(2) Selector (figures 8-59 through 8-65, pages 8-133 through 8-145). - The selector is a 24-bit word assembler and memory input gate. All data for memory enters the selector from either the Z-register (internal data) or data input gates (external data). Figure A-4, page A-9, shows the selector inputs.

A, B, and C of figure A-4, page A-9, show the selector inputs from the Z-register for left-shifting, right-shifting, or transferring data to memory without shifting. D of figure A-4, page A-9, shows the K-register input to the selector; this input is used during some shift operations to transfer the shift count from the K-register to the A-register. E, F, and G of figure A-4, page A-9, show the selector input from the Z-register and the consoles for one, two, and three-bit data transfers. H of figure A-4, page A-9, shows the selector inputs from the data input gates during 6-bit input data transfers. I of figure A-4, page A-9, shows the selector inputs from the data input gates during 8-bit input data transfers.

Selector outputs go to memory, X-register, and parity circuits. The parity circuits receive the same data as memory and generate parity bits for the data to be stored in memory. The selector outputs to the X-register are operands read from memory and transferred to the arithmetic section via the Z-register, selector, and X-register.

(3) Parity circuits. - The parity circuits have four functions:

1) Add parity bits to each half-word written into memory.

2) Check the parity of each half-word read from memory.

3) Add a parity bit to each 6-bit character transferred to the RD-277A or TCU.

4) Generate the necessary control signals when a parity fault occurs.

The parity circuits assure that the parity of the data read from memory is the same as the parity of the data written into memory. If not, they indicate a parity error. However, the parity circuits cannot detect a parity error if an even number of significant bits (ones) are dropped or picked up during a memory cycle. The parity circuits consist of lower parity check, upper parity check, and parity alarm. Figure 4-34, page 4-79, shows the parity circuits, and the associated circuits.

(a) Lower parity check (figure 8-66, page 8-147). - The computer recognizes odd parity as valid parity; that is, each half-word written into or read from memory must contain an odd number of ones, including the parity bit. The lower-parity circuits check the number of ones in the lower half (bits 0 through 11) of the word being written into memory via the Z-register and selector. If the number of ones is odd, a zero from the lower parity circuit accompanies the 12-bit half-word to lower memory. If the number of one bits is even, a one from the lower parity circuit accompanies the 12-bit half-word to lower memory.

The lower parity circuit also checks the number of ones in the lower half of each word read from memory. When a word is read from memory, each half-word, minus the parity bit, goes to the selector and lower parity circuit via the Z-register. The parity bit goes to the parity alarm circuit. The lower parity circuit checks the number of ones in the lower half of the selector and sends an odd or even signal to the parity fault circuit where it is compared with the parity bit. If the parity changed, a parity error signal is generated. The lower parity circuit also checks the parity of 6-bit characters transferred from lower memory to the computer. If the number of ones in the character is odd, the lower parity circuit sends a zero to position 2^6 of the C-register.

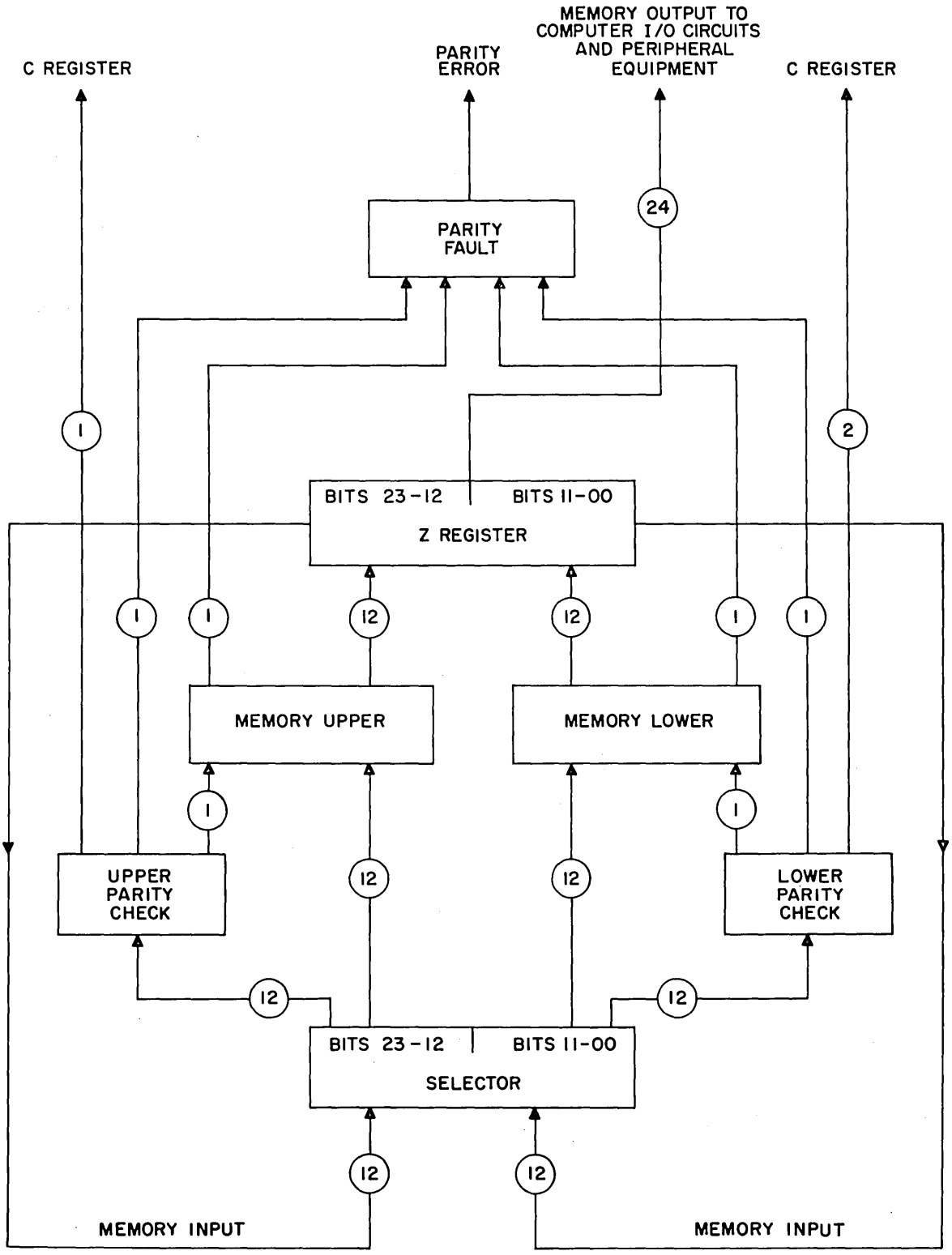


Figure 4-34. Parity and Associated Circuits

(b) Upper parity check (figure 8-67, page 8-149). - These circuits function the same as the lower parity circuits except they generate and check parity for the upper 12-bits of the words written into and read from upper memory.

(c) Parity fault (figure 8-90, C5, page 8-195). - The parity fault circuits detect parity errors and control computer operation when one occurs (see paragraph 4-16i, page 4-82). A parity error can occur during an I-sequence when the instruction is read from memory, during the M-sequence when the contents of the specified index register are read from memory, or during the R-sequence when instruction operands are read from memory. The parity fault circuits compare the outputs of the two parity check circuits with the two parity bits (one for each half-word) read from memory. A parity error in either of the half-words read from memory sets the parity-fault flip-flop and the following occurs:

1) Computer operation stops, providing HALT DISCONNECT switch is not in up (HALT DISCONNECT) position.

2) FAULT indicator on power control panel is lighted and horn sounds.

3) Computer fault is gated to the consoles.

h. Status Circuits. - The status circuits store status signals from the TCU and auxiliary computer and internal status signals. When the computer executes the 02 (TRF) instruction, the status circuits compare the status-check-code portion of the instruction with the specified status signal. If the status signal specified by the instruction is present, the status circuits generate a signal from the control section to continue the computer program in normal sequence. If the status signal specified by the instruction is not present, the status circuits generate a signal from the control section to jump the computer program from its present position in memory to the memory location specified by the address portion of the 02 (TRF) instruction. Table 4-5, page 4-18, lists the status check codes of the 02 (TRF) instruction and the status conditions that are checked with the codes. The M-register (index) holds the status check codes during the instruction. The status circuits consist of status detectors and a status translator.

(1) Status detectors (figures 8-79 and 8-80, pages 8-173 and 8-175). - There are three sets of status detectors: one for TCU status

signals, one for auxiliary-computer-status signals, and one for console-status signals.

The TCU status detectors for control error, transport ready, data transfer error, and tape mark operate the same. When the computer is master cleared, flip-flop 7XV05 sets and flip-flop 7XV00 clears. The two flip-flops remain in this state until TCU sends the tape-mark signal. Then, flip-flop 7XV00 sets at time 5.3 of any following sequence. One phase later flip-flop 7XV05 clears. The flip-flops remain in this state until TCU removes the tape-mark signal or the 02 (TRF) instruction, specifying the tape-mark status line, is executed. If TCU removes the tape-mark signal before the instruction is executed, flip-flop 7XV05 again sets in preparation for the next tape-mark signal. If the 02 (TRF) instruction is executed and the tape-mark status line is specified, flip-flop 7XV00 clears at time 6.2 of the I-sequence of the 02 (TRF) instruction. Flip-flop 7XV00 remains clear until TCU removes the tape-mark signal. With the tape-mark signal gone, flip-flop 7XV05 sets and the tape-mark detector is ready to receive the next tape-mark signal. The TCU input-overflow detector, flip-flop 7XV20 sets when the computer honors a TCU input request and the memory area for TCU input data is full (buffer-terminate condition). The flip-flop remains set until it is sensed by the 02 (TRF) instruction. The flip-flop clears at time 6.2 of the I-sequence of the 02 (TRF) instruction. The TCU busy detector sends the signal directly to the status translation circuits as long as TCU sends the busy signal.

The auxiliary-computer-status detectors consist of flip-flops 7XV50 and 7XV55. Flip-flop 7XV50 is for the input-busy-status signal, and flip-flop 7XV55 is for the initiate-status signal. There is no flip-flop for the output-busy signal as the signal is generated by the input busy flip-flop of the auxiliary computer. Flip-flops 7XV50 and 7XV55 set when the auxiliary computer sends an external function code of 300_8 to the computer. Flip-flop 7XV55 remains set until the computer (not auxiliary computer) executes an external-function code of 100_8. Flip-flop 7XV50 remains set until the auxiliary computer requests an output character from the computer and all characters in the memory area have been transferred, (resulting in a terminate code of 200_8 sent to the auxiliary computer) or until the memory area in the auxiliary computer is full and the auxiliary computer sends the terminate code of 200_8.

The console status detectors consist of flip-flops 7XV60, and 7XV71 through 7XV74. Flip-flop 7XV60 detects the completion of a console switch input word. Flip-flop 7XV60 sets when a console-switch-input character is

received by the computer, and the I/O control word has a character count equal to 10_2. A character count of 10_2 indicates that memory location specified by the address portion of the I/O control word is filled with three console-switch-input characters. Flip-flop 7XV60 sets at time 4.3 of the RC1-sequence and remains set until it is sensed by the TRF instruction.

Flip-flops 7XV71 through 7XV14 detect and store the status of the first I/O control word assigned to each console input data operation. Flip-flop 7XV71 sets when the computer accepts a data character from console O, and the memory area specified by console-data I/O control-word 1 is full. One of the flip-flops, 7XV71 through 7XV74, depending on the console request, sets at time 4.3 of the RC2-sequence and remains set until sensed by the 02 (TRF) instruction.

(2) Status translator (figure 8-81, page 8-177). - The status translator compares the status-check-code portion of the 02 (TRF) instruction with the specified status line or flip-flop output. If the specified status line is active or the flip-flop is set, flip-flop 0XM46 remains clear and no transfer of the computer program occurs. If the specified status line is not active or the specified flip-flop is not set, flip-flop 0XM46 sets and a signal from the flip-flop goes to the control section to jump the computer program from its present position to the memory location specified by the address portion of the 02 (TRF) instruction.

i. Fault Circuits (figure 8-90, page 8-195). - The fault circuits detect and display faults in the input/output section and errors in data read from memory (parity errors).

The input/output faults detected and displayed by the fault circuits are data overflow, switch overflow, and keyboard overflow. The data-overflow flip-flop is set when the memory area for console input data is full (word count of control words 1 and 2 equals 0) and the console attempts to send more data to the computer. The switch-overflow flip-flop is set when the memory area for console switch input is full and the console attempts to send more switch data to the computer. The keyboard-overflow flip-flop is set when the memory area for console keyboard input is full and the console attempts to send more keyboard data to the computer. The three overflow flip-flops clear when the computer is master cleared, the FAULT INDICATORS Clear switch is pressed, or the start signal is activated at the beginning of an operation.

A parity error occurs when either of the half-words, including the parity bit, read from memory does not contain an odd number of one bits. The parity fault circuits consist of lower-parity, upper-parity, and parity-fault flip-flops. The lower-parity flip-flop sets when the parity bit for the lower 12 bits of the word read from memory is a one. The upper-parity flip-flop sets when the parity bit for the upper 12 bits of the word read from memory is a one. The parity-fault flip-flop sets at time 4.2 of an I, M, or R-sequence to signify a parity fault. If the lower-parity flip-flop is set, indicating the parity bit is a one, and the lower half-word contains an odd number of ones, the parity-fault flip-flop sets. If the lower-parity flip-flop remains clear, indicating that the parity bit is a zero, and the lower half-word contains an even number of ones, the parity-fault flip-flop sets. The upper-parity flip-flop operates the same way. When any of the described faults and errors or the halt error occur, the FAULT indicator on the power control panel is lighted, the horn sounds (if not disabled), the appropriate error indicator on logic panel A2 is lighted, and a fault control signal is gated to each console. In addition, if a parity or halt error occurs and the HALT DISCONNECT switch is not in the up (HALT DISCONNECT) position, computer operation stops.

4-17. ARITHMETIC SECTION. - The arithmetic section performs arithmetic and logical operations. Arithmetic operations consist of algebraic addition, subtraction, multiplication, and division. In algebraic addition and subtraction, results include all borrows. Logical operations consist of shifting, negation, logical addition, and logical multiplication. In logical addition and multiplication, results do not include any borrows that may be generated. The following paragraphs contains a functional description of each part of the arithmetic section and a description of each arithmetic section operation.

a. Function Sections. - The arithmetic section consists of the following sections: X-register, D-register, adder, A-register, and U-register. Figure 4-35, page 4-84, is a functional block diagram of the arithmetic section.

(1) X-register (figures 8-32 through 8-36, pages 8-73 through 8-81). - The X-register is the data exchange register between the memory and the arithmetic section. All data from memory enters the arithmetic section via the X-register. Data to memory leaves the arithmetic section via the X-register or adder. Data leaving the arithmetic section via the adder is data resulting from an add, subtract, or logical operation involving a memory value. Data leaving the arithmetic section via the X-register is data that has not been operated on by the adder. This data includes

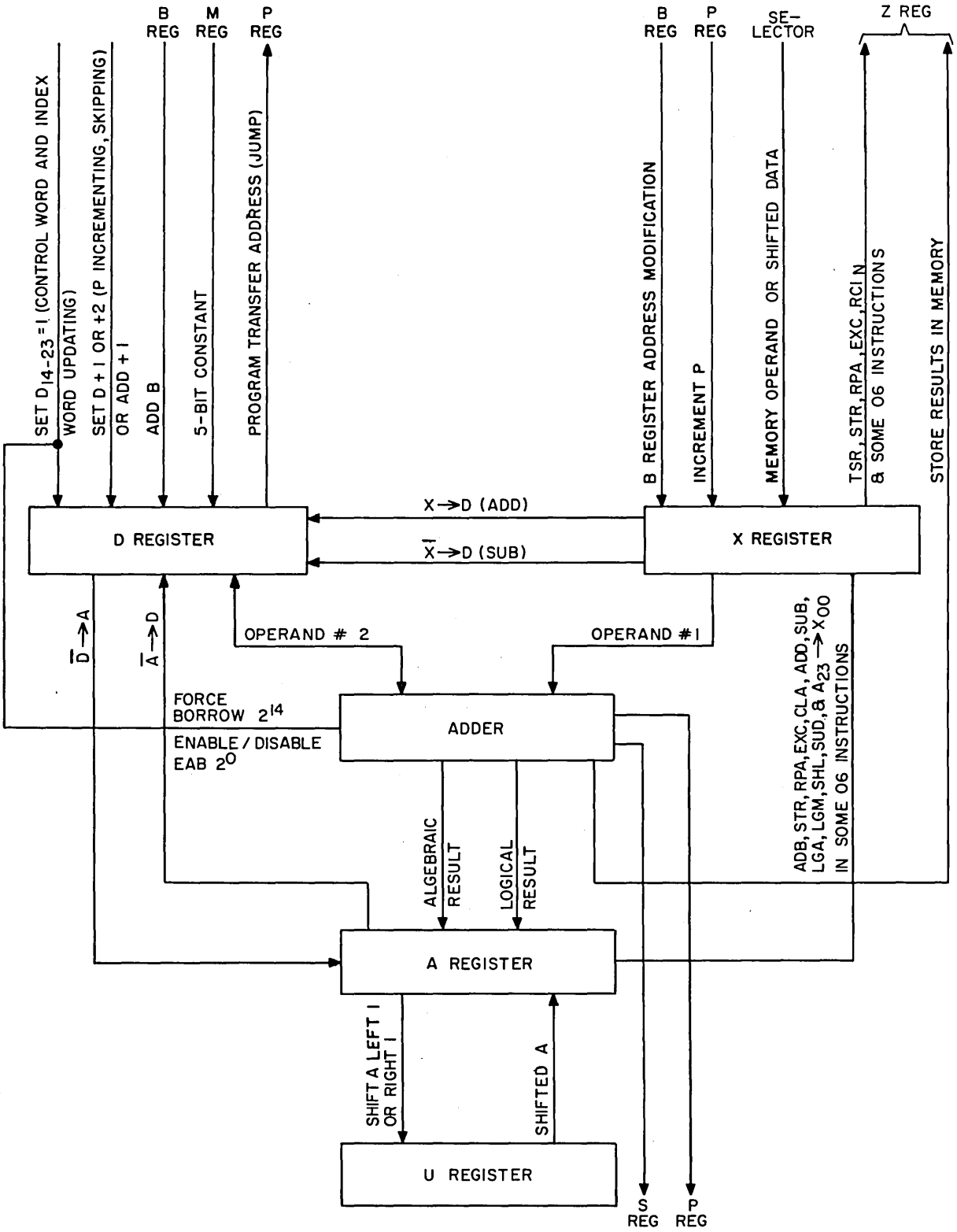


Figure 4-35. Arithmetic Section, Functional Block Diagram

store-the-contents-of-A, replace-an-address, and exchange-the-contents-of-A. The X-register also receives the shifted data from the Z-register.

Other X-register inputs are from the P, B, and A-registers. The P-register input occurs every time the P-register must be incremented. The B-register input occurs every time the instruction specifies B-register modification of the address in the instruction. A-register inputs occur at three different times:

1) During the STR (12) and RPA (13) operations when the contents of A or the lower 14 bits of A are stored in memory.

2) During the EXC (20), CLA (30), ADD (31), SUB (32), LGA (34), LGM (35) R-sequence operations, the ADB (36) I-sequence operation, and the 06-0 RCA mode and 06-6 R/W-sequence operations when the contents of A are required to be exchanged with the contents of a memory location (EXC), the original contents of A are transferred to X (CLA, ADD, SUB, LGA, LGM); or the contents of A are to be added together with the contents of B(ADB).

3) During some shifting sequences, A_{23} enters X_{00} when required. The other X-register output is to the D-register. Refer to paragraph 4-17a(2), below.

The X-register-enable circuits (figure 8-32, page 8-73) generate the signals to clear and load the X-register at the proper times. Paragraph 4-21, page 4-171, contains timing charts for each instruction. These timing charts show when the X-register is loaded, what it is loaded with, the destination of X-register outputs, and when these outputs leave the X-register.

(2) D-register (figures 8-37 through 8-42, pages 8-83 through 8-93). - The D-register holds one of the operands to be added or subtracted. During transfer instructions the D-register holds the transfer address.

The D-register inputs are from the X, A, M, and B-registers and also from control logic. The D-register receives operands from the X-register. During the add operation, the D-register input from the X-register is a straight X to D transfer. During the subtract operation, this transfer is $\overline{X}$ (complement of X) to D. During the logical negation (01), compare (33), and logical multiply (35) operations, the complement of A is transferred to D. The M-register input occurs only during the ADC instruction when

bits 14 through 18 of the instruction are added to the contents of a memory location. The B-register input occurs during the ADB instruction when the contents of the B and A-registers are added. Control logic inserts values into the D-register when the following occur.

1) One is added to a operand.

2) P-register is incremented.

3) Input/output and RCA control words are updated.

4) Index words are augmented.

Control logic sets the D-register to +1 when one is added to a memory location and to +1 or +2 when the instruction address (P-register) is incremented. Control logic sets bits 14 through 23 of the D-register to all ones when the word-count portion of input/output and RCA control words and the tally portion of the index words is to be decremented by one. Other enables which are generated when bits 14 through 18 of the D-register are set to ones, go to the adder to increment the address portion if required.

The D-register-enable circuits (figures 8-37 and 8-38, pages 8-83 and 8-85) generate the signals to clear and load the D-register at the proper times. Paragraph 4-21, page 4-171, contains timing charts for each instruction. These timing charts show when the D-register is loaded, what it is loaded with, the destination of D-register outputs, and when these outputs leave the D-register.

(3) Adder (figures 8-43 through 8-47, pages 8-95 through 8-103). - The adder (figure A-5, page A-11) is a subtractive type adder. It subtracts the complement of the D-register contents from the X-register contents to perform the addition. The adder automatically complements the D-register input. The adder inputs are not gated; therefore, the output is always the sum of the contents of the X-register and the contents of the D-register. The adder has two types of outputs: the half-subtract output and the full-subtract output. The half-subtract output is the difference between the X-register and the complemented contents of the D-register without consideration to any borrows that may be generated. The full-subtract output is the difference between the X-register and the complemented contents of the D-register with all borrows satisfied.

Operation of the subtractive adder is exactly the same for addition and subtraction. For addition, the addend is obtained by a straight X-to-D transfer. The D input to the adder is automatically complemented. This complemented addend ($\overline{D}$) is subtracted from the augend (X). The difference output from the subtractive adder is actually the sum of X and D. For subtraction, because the adder is actually a subtracter, no complementing should be needed. However, to compensate for the automatic D-to-adder complementing, an $\overline{X}$-to-D transfer occurs. This complements the addend before it enters D. Then when the automatic D-to-adder complementing occurs, the contents of D is recomplemented so that the original addend enters the adder. Now when the addend is subtracted from the augend, the subtractive adder output is the difference of X and D.

The subtractive adder consists of four parts: half-subtracters, difference generators, borrow generators, and group borrow logic. There are 24 stages, each consisting of a half-subtracter, a difference generator, and a borrow generator. Each stage corresponds to a bit and six stages comprise a group. Figure A-5, page A-11, is a simplified block diagram showing the first of four groups.

(a) Half-subtracter. - Figure 4-36, page 4-88, shows a half-subtracter stage. The 30A circuits are the half-subtracters of each stage. They compare the corresponding bits of the X and D registers and effectively subtract the subtrahend ($\overline{D}$) from the minuend (X), disregarding borrows.

Note: - The inputs being compared by the half-subtracter are from the opposite sides of the X and D-register flip-flops. Effectively, this is the same as comparing $\overline{X}$ and $\overline{D}$. If the same sides of the flip-flops were compared, it would be a comparison of X and D.

When X and $\overline{D}$ are equal [both ones (L) or zeros (H)] the half-subtracter outputs a zero (H). When X and $\overline{D}$ are not equal, the output is a one (L). This logic corresponds to normal binary subtraction, disregarding borrows.

(b) Borrow generator. - Figure 4-37, page 4-89, shows an odd and even bit borrow-generator stage. The 40A circuits are the borrow-generators of each stage, and determine if a borrow is required from the next higher stage. The borrow-generator logic reverses at each stage. A zero (H) output from the odd-numbered 40A circuits implies that a borrow is required from the next higher stage. A one (L) output from the even-numbered 40A circuit implies that a borrow is required from the next

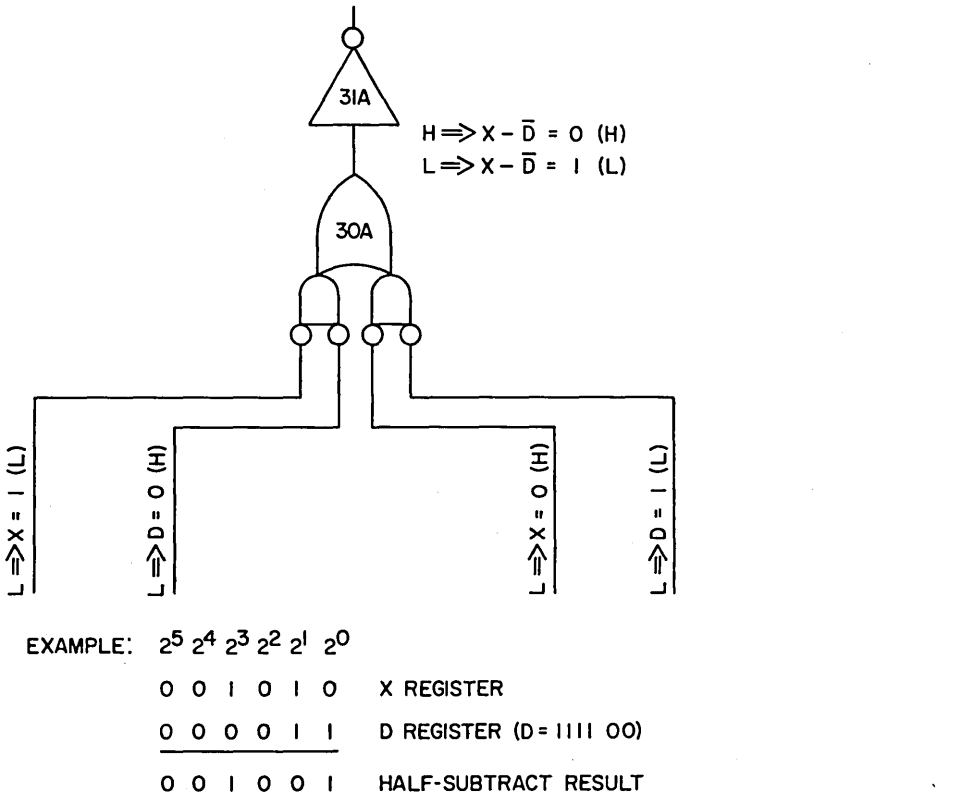


Figure 4-36. Half-Subtracter

higher stage. The odd-numbered 40A circuits produce a zero (H) output when the result of the half-subtract is a zero (H) (indicating $X = \overline{D}$) and a borrow is required from the previous stage or the result of the half-subtract is a one (indicating $X \neq \overline{D}$) and $\overline{D}$ is a one (L).

The even-numbered 40A circuits produce a one (L) output when the half-subtracter indicates a borrow may be required ($X \neq \overline{D}$) and $\overline{D}$ is a one (L) or when the previous stage requires a borrow and either $\overline{D}$ is a one (L) or X is a zero (H).

Note: - If a stage requires a borrow, because $\overline{D} > X$, it can satisfy a borrow from the previous stage. If a stage does not require a borrow, it cannot satisfy the borrow from a previous stage and it propagates to the next higher stage.

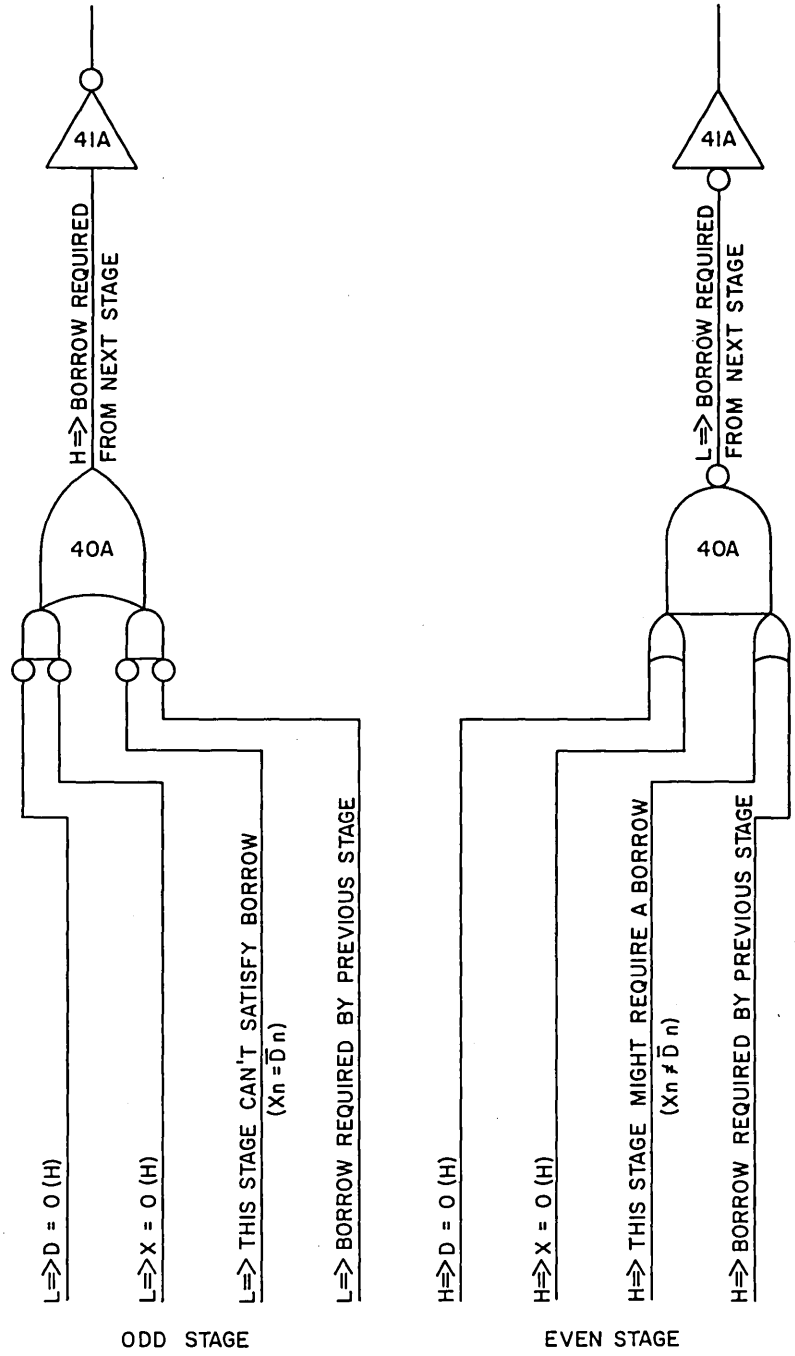


Figure 4-37. Borrow Generator

Referring to the example below, stages 2^1 and 2^2 require borrows.

Example:	2^5	2^4	2^3	2^2	2^1	2^0	
	0	0	1	0	0	1	X
	0	0	1	1	1	0	$\overline{D}$
	0	0	0	1	1	1	Half-Subtract (30A)
	1	1	1	1	0	1	Borrows (40A)
	1	1	1	0	1	0	Full-Subtract (70A)

Because 2^2 requires a borrow, it satisfies the borrow required by 2^1. Also, 2^3, 2^4, and 2^5 do not require borrows and cannot satisfy a borrow. Thus, the borrow required from 2^2 must propagate end-around and be satisfied by 2^0. Any time a borrow propagates through a stage that cannot satisfy it, the half-subtract result is complemented in the final result.

(c) Difference generator. - Figure 4-38, page 4-91, shows the difference-generator stages. The 70A circuits are the difference generators of each stage and compare the output of the half-subtracter with the output of the borrow generator of the previous stage. The output from these circuits is the final result of the arithmetic operation.

The difference generator output is a one (L) if the output from the half-subtracter is a one (L) and the previous stage does not require a borrow or if the output from the half-subtracter is a zero (H) and the previous stage requires a borrow. The difference-generator output is a zero (H) if the output from the half-subtracter is a one (L) and the previous stage requires a borrow, or if the output from the half-subtracter is a zero (H) and the previous stage does not require a borrow.

(d) Group borrow logic (figure 8-43, page 8-95). - The group borrow logic reduces the time required to perform a full-subtract operation when borrows are required. It is possible during a full-subtract operation that the low-order stage (2^0) may require a borrow and this borrow can only be satisfied by the high-order stage (2^{23}). The group-borrow logic reduces the time consumed propagating this borrow through all stages of the adder until it reaches stage 2^{23}. The group-borrow logic consists of four group-borrow-enable circuits, and four group-borrow circuits. Figure A-6, page

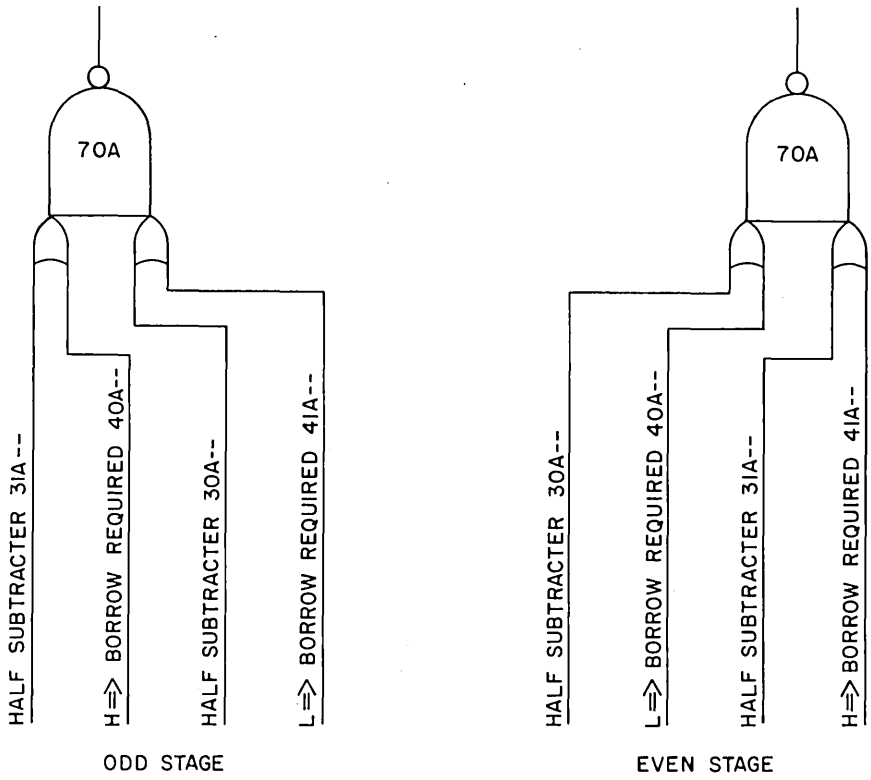


Figure 4-38. Difference Generator

A-13, shows these circuits along with simplified blocks of the adder and the X and D-registers.

Each group-borrow-enable circuit monitors the half-subtract outputs of a 6-bit adder group. When the half-subtract outputs from a group indicate that the contents of X and $\overline{D}$ are equal [all zeros (H) or all ones (L)], the group-borrow-enable circuit generates a borrow-enable signal. The signal indicates that the adder group does not require a borrow and thus cannot satisfy a borrow. The borrow-enable signals are combined to indicate which adder groups cannot satisfy borrows. The combined signals go to the group-borrow circuits.

The group-borrow circuits, one for each group, monitor the borrow-enable signals and control the propagation of the group borrows. For example, if group one requires a borrow and group two cannot satisfy it, but group three can, the borrow from group one bypasses group two and immediately starts propagating through group three, where it is satisfied. Also, if group one requires a borrow and groups two, three, and four cannot satisfy the borrow, it bypasses these groups and immediately begins propagating through group one where it is satisfied as an end-around borrow. The same operation occurs for any combinations of groups requiring borrows and any

combinations of groups not able to satisfy borrows. Anytime a group is bypassed because it cannot satisfy an existing borrow, the full-subtract output [all zeros (H)] is complemented to all ones(L).

(4) A-register (figures 8-48 through 8-52, pages 8-105 through 8-113). - The A-register (accumulator) receives two different outputs from the adder during normal arithmetic operations: the logical difference between the contents of the X-register and the complemented contents of the D-register, and the algebraic difference between the contents of the X-register and the complemented contents of the D-register. The A-register operates in conjunction with the U-register to left-shift the contents of the A-register. The A-register also operates in conjunction with the D-register to perform the logical negation, logical multiply, compare, exchange, clear add, RCA shift, and SUD shift instructions and the R/W reload sequence.

The A-register-enable circuits (figure 8-48, page 8-105) generate the signals to clear and load the A-register at the proper times. Paragraph 4-21, page 4-171, contains timing charts for each instruction. These timing charts show when the A-register is loaded, what it is loaded with, the destination of the outputs, and when these outputs leave the A-register.

(5) U-register (figures 8-53a, 8-53b and 8-53c, pages 8-117 through 8-121). - The U-register serves as the lower rank for the A-register during shifting operations. The contents of the A-register are right-shifted or left-shifted by sending the shifted contents of A to U, and returning the contents of U to A. The U-register enable circuits (figure 8-53a, page 8-117) generate the signals to clear and load the U-register at the proper times. Paragraph 4-21, page 4-171, contains timing charts that show when the U-register is loaded from the A-register and the time when the U-register is transferred to the A-register.

b. Description of Operation. - The following paragraphs describe the arithmetic and logical operations performed by the arithmetic section.

(1) Control word and index register updating. - Figure 4-39, page 4-93, shows how the arithmetic section updates input/output control words, RCA control words, and index registers. The input/output control words and RCA control words consist of a word count and an address. During computer operation these control words are updated. The word count is decremented by one and the address is incremented by one. The index words consist of a tally field and an address field. During the execution of a 05 (TAX) instruction (and tally field not equal to zero), the tally field is

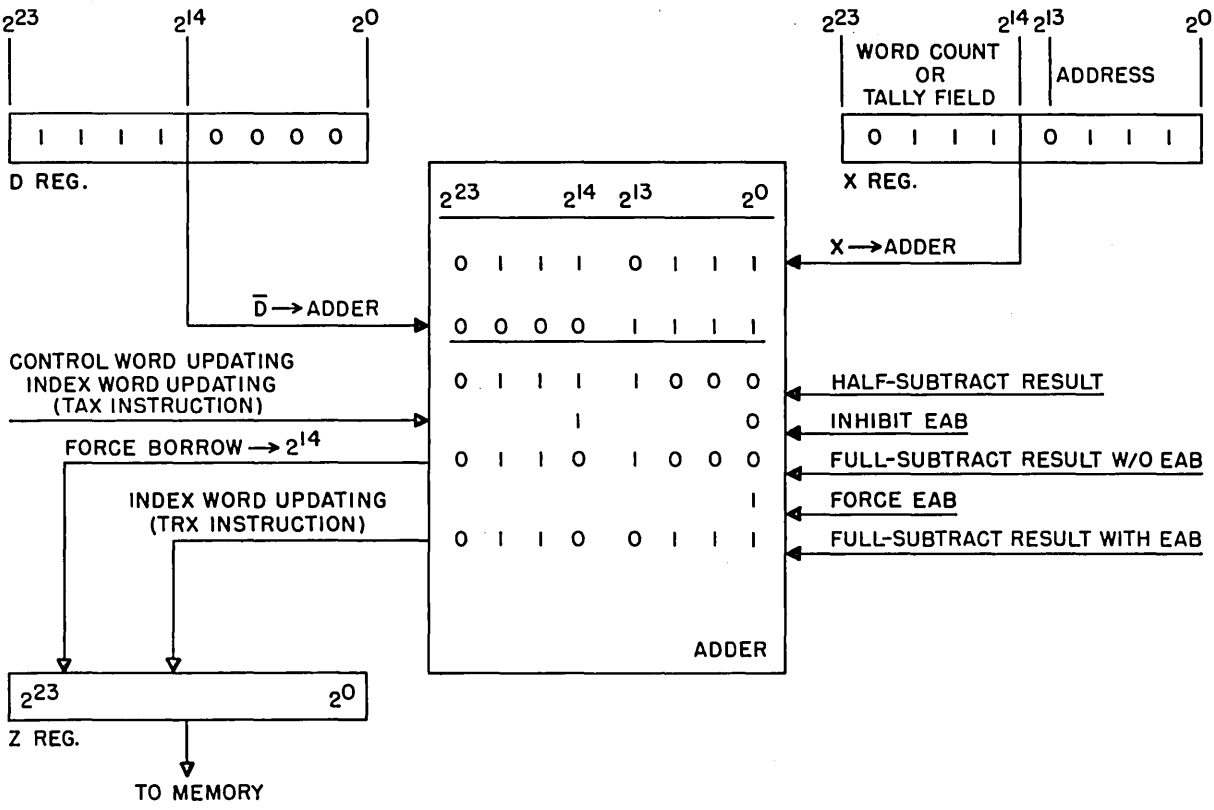


Figure 4-39. Control Word and Index Word Updating

decremented by one and the address field is incremented by one. During the execution of a 04 (TRX) instruction (and tally field not equal to zero), the tally field is decremented by one but the address field remains constant.

The X register holds the word to be updated. In this example, the word count equals 7 and the address equals 7. Bits 14 through 23 of the D-register are set to all ones. The contents of the X and D-registers enter the adder. The adder automatically complements the D-register contents.

If the word being updated during the 05 (TAX) instruction is a control word or index word, two signals are generated for the adder to alter the half-subtract result of X and $\overline{D}$. These signals are force-borrow $\longrightarrow 2^{14}$ and inhibit-end-around-borrow. The force-borrow signal simulates a borrow from bit position 2^{13}, regardless of the value of the address portion of the control or index word, to decrement the word count or tally field to 6. Also, since the half-subtract result of the address portion of the control word or index word and bits 2^{0} through 2^{13} of $\overline{D}$ is always one larger than the initial address, an inhibit-end-around-borrow signal is generated. This signal ensures that no end-around-borrow occurs to alter the incremented

address of 8. If the index word is being updated during the 04 (TRX) instruction, the force-borrow $\longrightarrow 2^{14}$ and force-end-around-borrow signals are generated for the adder to alter the half-subtract result of X and D. The force-borrow decrements the tally field to 6 as in a 05 (TAX) instruction. The force-end-around-borrow signal simulates an end-around-borrow signal to subtract one from the incremented address, returning the address portion of the index word to its initial value of 7.

(2) P-register incrementing. - Figure 4-40, page 4-95, shows how the arithmetic section increments the P-register. The P-register contents go to the X-register, the D-register is set to +1 or +2 (depending upon whether the P-register is to incremented by one or two), and the results of the addition return to the P-register.

(3) Index register address modification. - Figure 4-41, page 4-95, shows how the arithmetic section adds the contents of an index register to the address of an instruction. First, the instruction is read from memory into the Z-register. Then the address portion of the instruction goes to the X-register and on to the D-register. The index register contents are read from memory and the lower 14 bits go to the X-register. The adder output is the sum of the two values in X and D. This modified address specifies the memory location of an operand.

(4) B-register address modification. - Figure 4-42, page 4-96, shows how the arithmetic section adds the contents of the B-register to the address of an instruction. First the instruction is read from memory into the Z-register. Then the address portion of the instruction goes to the X-register and on to the D-register. The B-register contents then go to the X-register. The adder output is the sum of the 14-bit B-register contents and the 9-bit address in the D-register. This modified address specifies the memory location of an operand.

(5) Add one to memory. - Figure 4-43, page 4-96, shows how the arithmetic section adds one to a memory location for a 22 (ADO) instruction. The X-register holds the contents of the specified memory location and the D-register is set to +1. The adder output goes to the selector and returns to memory.

(6) Add constant to memory. - Figure 4-44, page 4-97, shows how the arithmetic section adds a 5-bit constant to the contents of a memory location for a 21 (ADC) instruction. The 5-bit constant is specified in

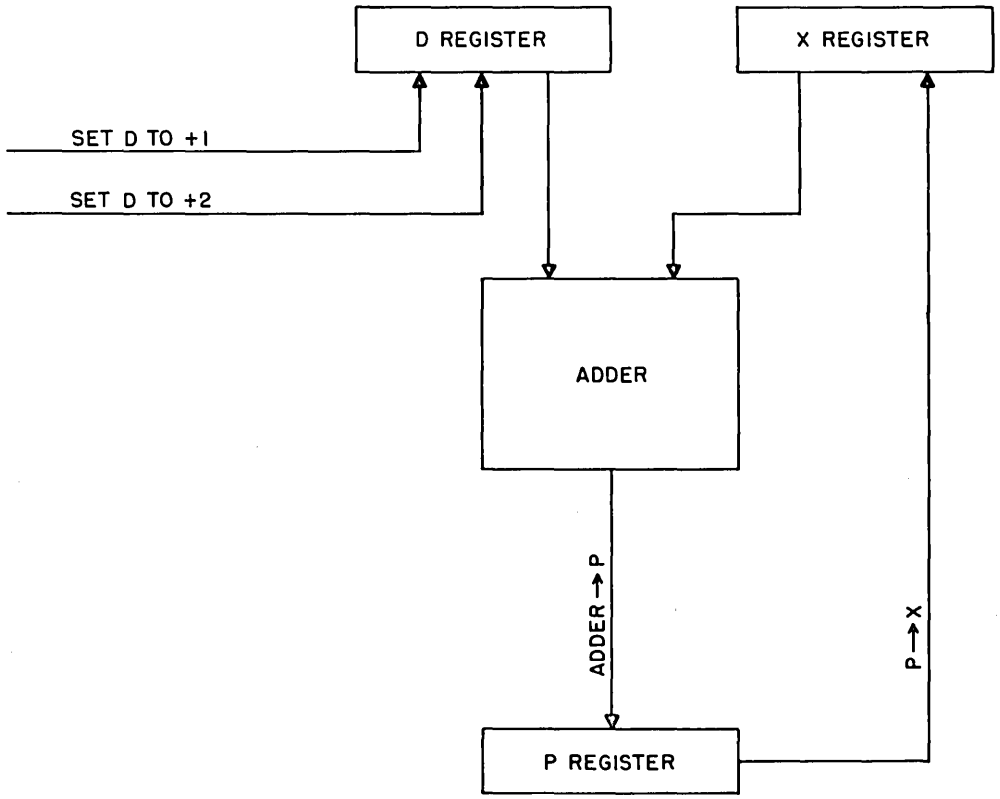


Figure 4-40. P-Register Incrementing

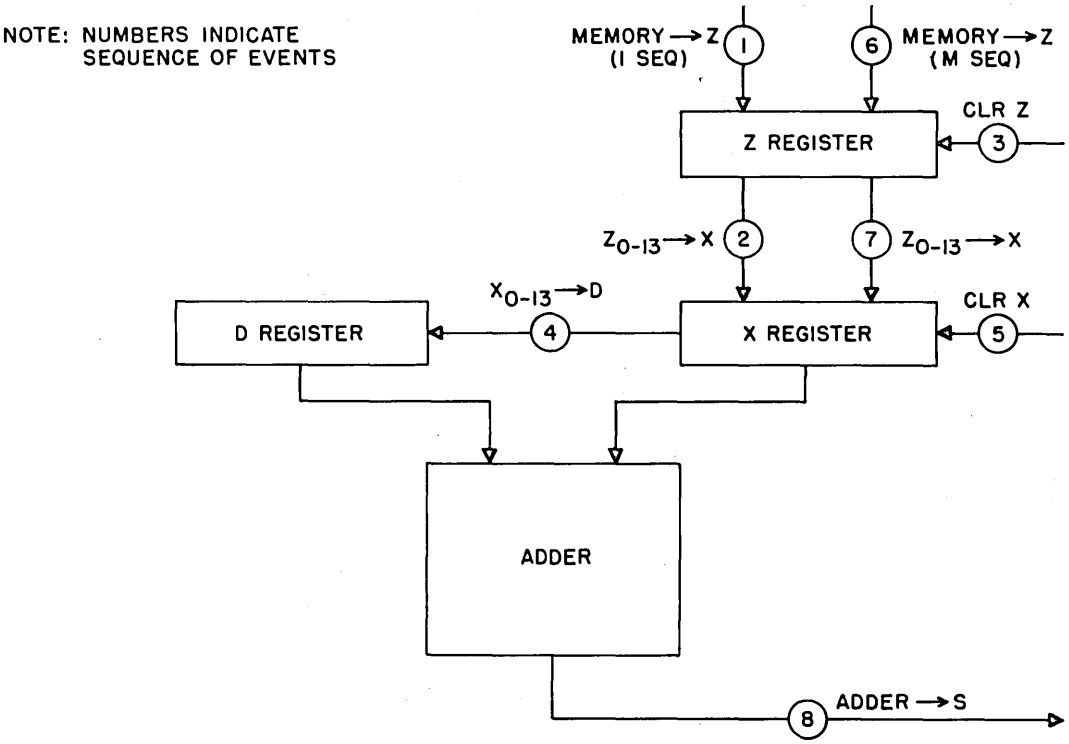


Figure 4-41. Index Register Address Modification

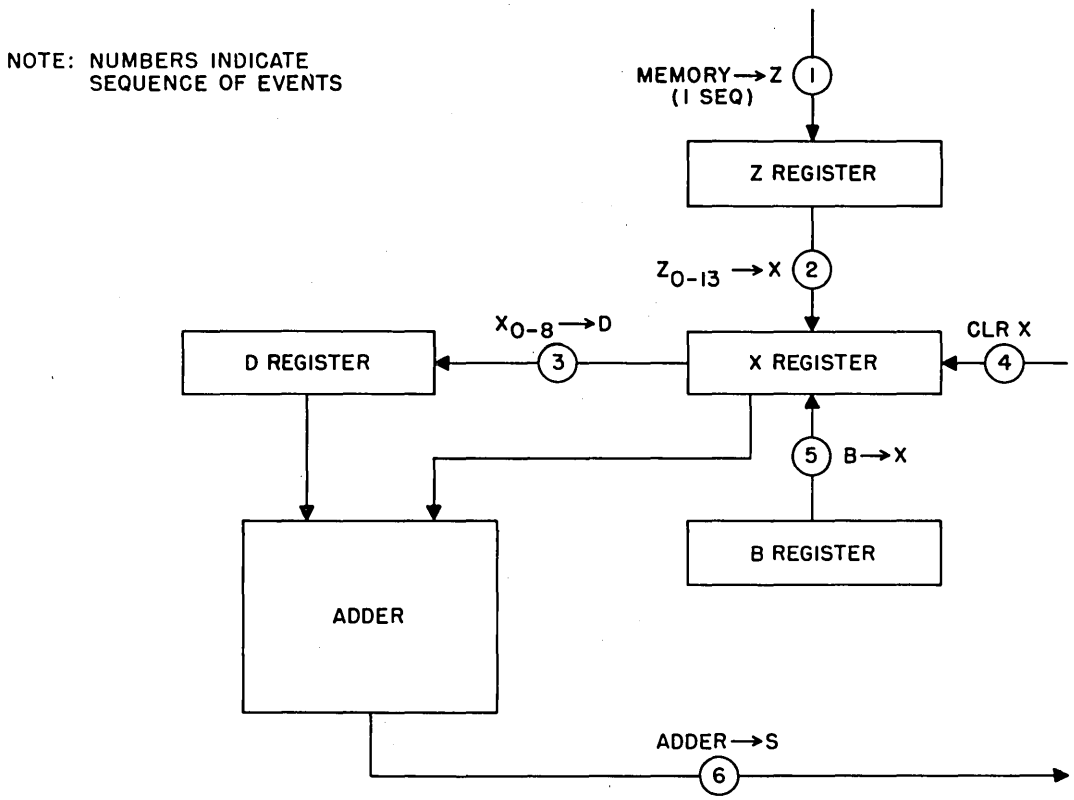


Figure 4-42. B-Register Address Modification

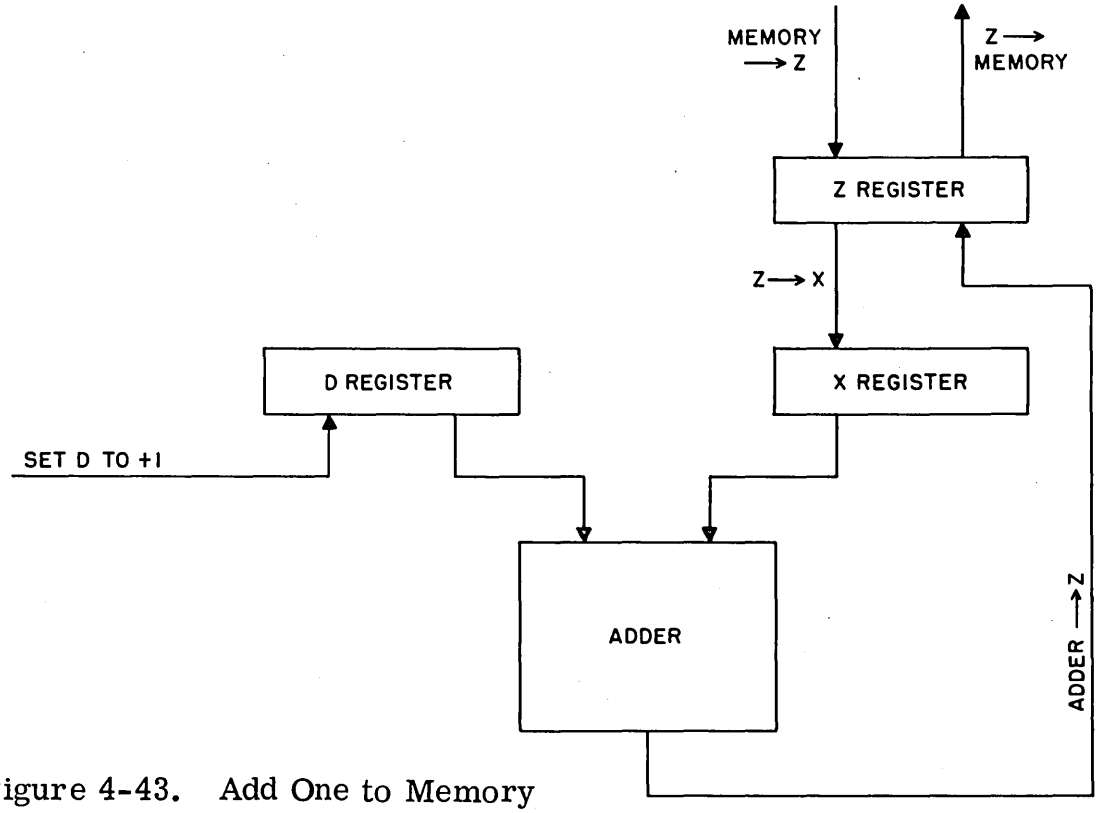


Figure 4-43. Add One to Memory

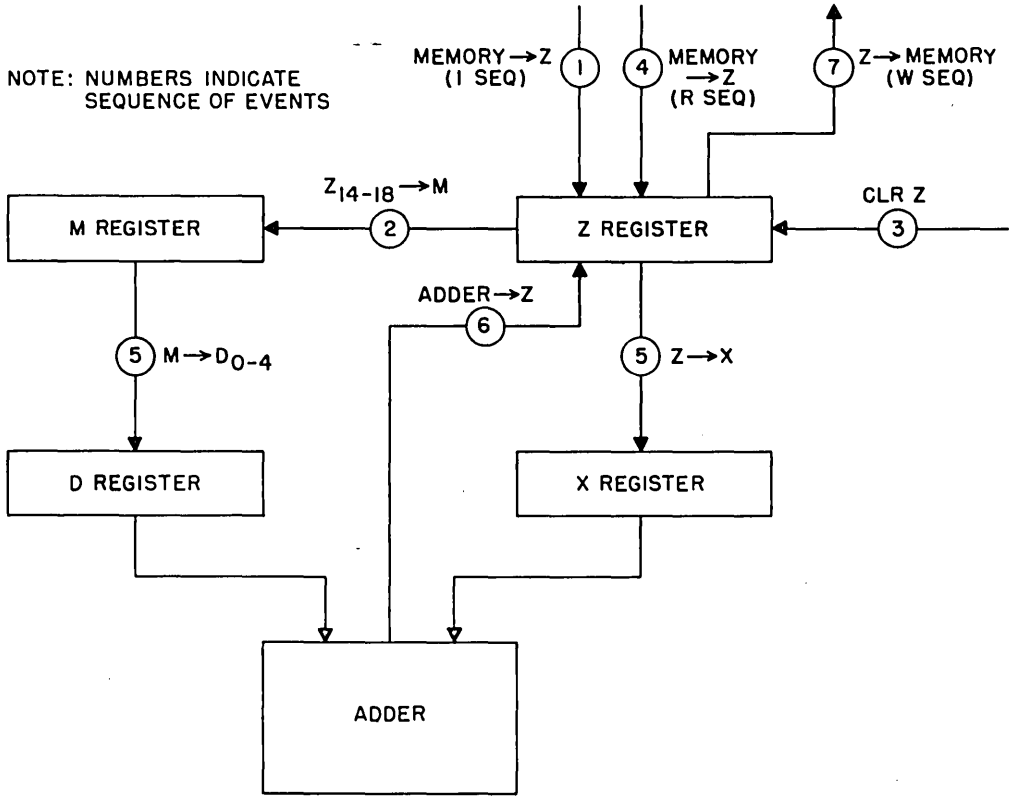


Figure 4-44. Add Constant to Memory

the instruction. First the instruction is read from memory into the Z-register. The 5-bit constant then goes to the M-register. Next, the contents of the specified memory location are read from memory into the Z-register and go on to the X-register. The 5-bit constant in the M-register goes to the D-register. The adder output which is the sum of the contents of the memory location and the constant goes to the selector and returns to memory.

(7) Add A and B-registers. - Figure 4-45, page 4-98, shows how the arithmetic section adds the contents of the B and A-registers for a 36 (ADB) instruction. The 24-bit A-register contents go to the X-register and the 14-bit B-register contents go to the D-register. The sum from the adder goes to both the A and B-registers. The A-register receives the 24-bit sum. The B-register receives the lower 14 bits of the sum.

(8) Add, subtract memory and A-register contents. - Figure 4-46, page 4-98, shows how the arithmetic section performs the algebraic add, algebraic subtract, and logical add operations involving the contents of a memory location and the contents of the A-register. First, the contents of the specified memory location are read from memory into the Z-register. The memory contents then go through the X-register to the

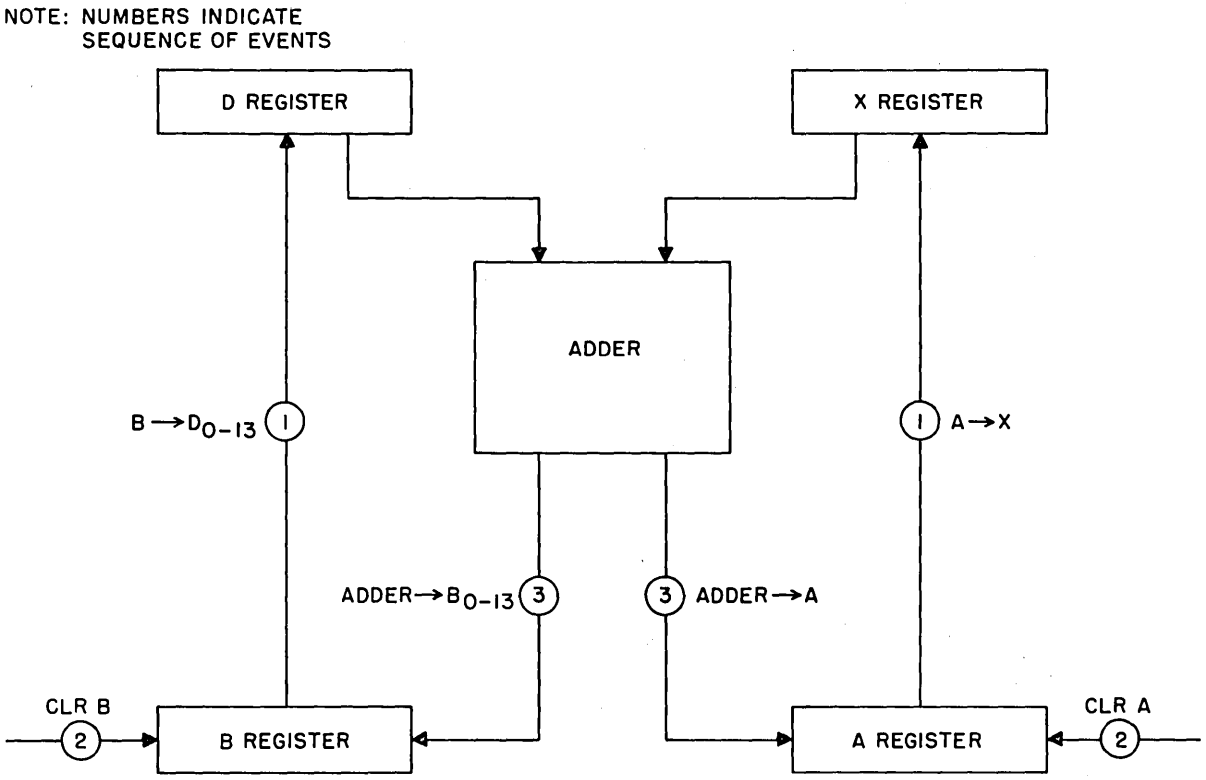


Figure 4-45. Add A and B-Register Contents

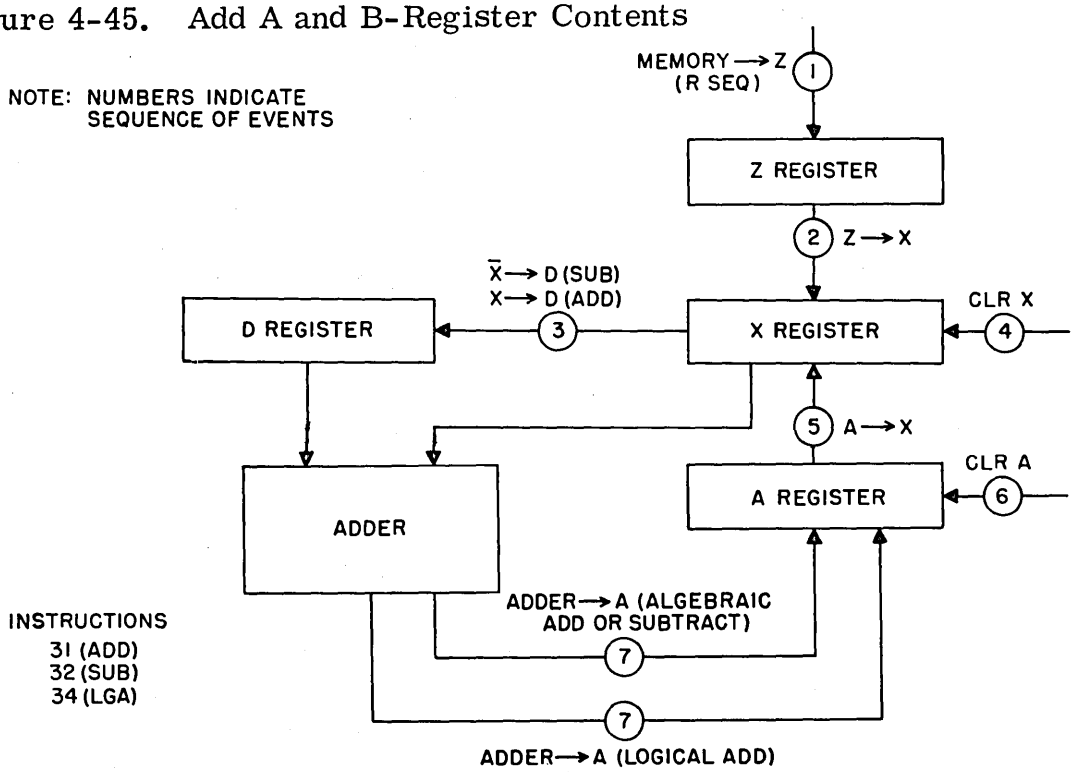


Figure 4-46. Add, Subtract Memory Contents and A-Register Contents

D-register. The X-register clears and the A-register contents go to the X-register; the A-register then clears. The adder output (result of the operation) goes to the A-register. The adder output may be an algebraic or a logical output.

(9) Logical negation. - Figure 4-47, page 4-100, shows how the arithmetic section performs the 01 (LGN) logical-negation instruction.

(10) Logical multiply. - Figure 4-48, page 4-100, shows how the arithmetic section performs the 35 (LGM) logical-multiply instruction. One of the values to be multiplied is in the A-register. The other value comes from memory into the X-register via the Z-register and selector; the complement of this value then goes to the D-register, and the complement of the contents of the A-register goes to the D-register. The complement of the contents in D, then, is sent back to the A-register. Thus, the A-register contains the logical-multiply result of the original A-register contents and the contents of the memory location specified by the instruction.

(11) Exchange. - Figure 4-49, page 4-100, shows how the arithmetic section exchanges the contents of the A-register with the contents of a memory location specified by the address portion of a 20 (EXC) instruction. The contents of a memory location are read into the X-register through the Z-register and the selector during an R-sequence. The X-register contents are complemented and sent to the D-register. Then, the A-register contents go to the X-register. The contents of the D-register are recomplemented ($\overline{D}$) and sent to the A-register. During a W-sequence, the original A-register contents go to the Z-register where they are read into the memory location.

(12) Clear add. - Figure 4-50, page 4-101, shows how the arithmetic section replaces the contents of the A-register with the contents of a memory location specified by the address portion of a 30 (CLA) clear add instruction. First, the contents of a memory location are read through the Z-register into the X-register. Then, the complement of the contents in the X-register ($\overline{X}$) goes to the D-register. Then, the complement of the contents in the D-register ($\overline{D}$) goes to the A-register.

(13) Shift A-register. - Figures 4-18 and 4-25, pages 4-51 and 4-61, show how the arithmetic section performs the A-register shift.

(14) Multiply. - Figures 4-28 and 4-29, pages 4-65 and 4-66, illustrate the multiply operation.

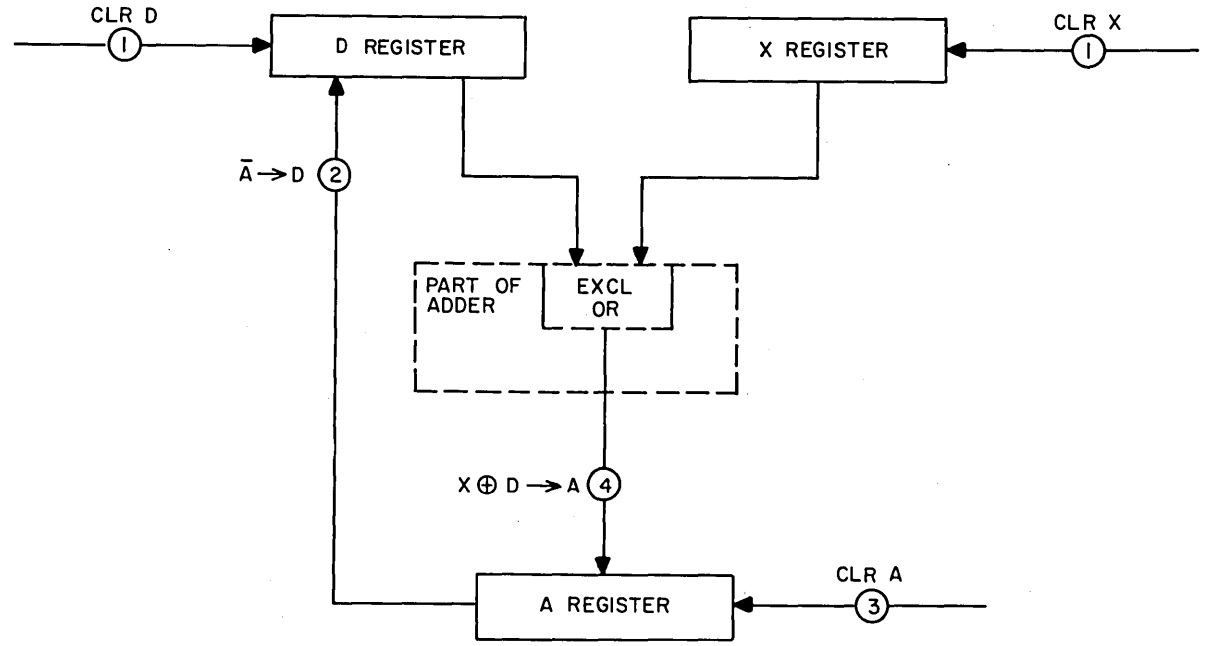


Figure 4-47. Logical Negation, Instruction 01

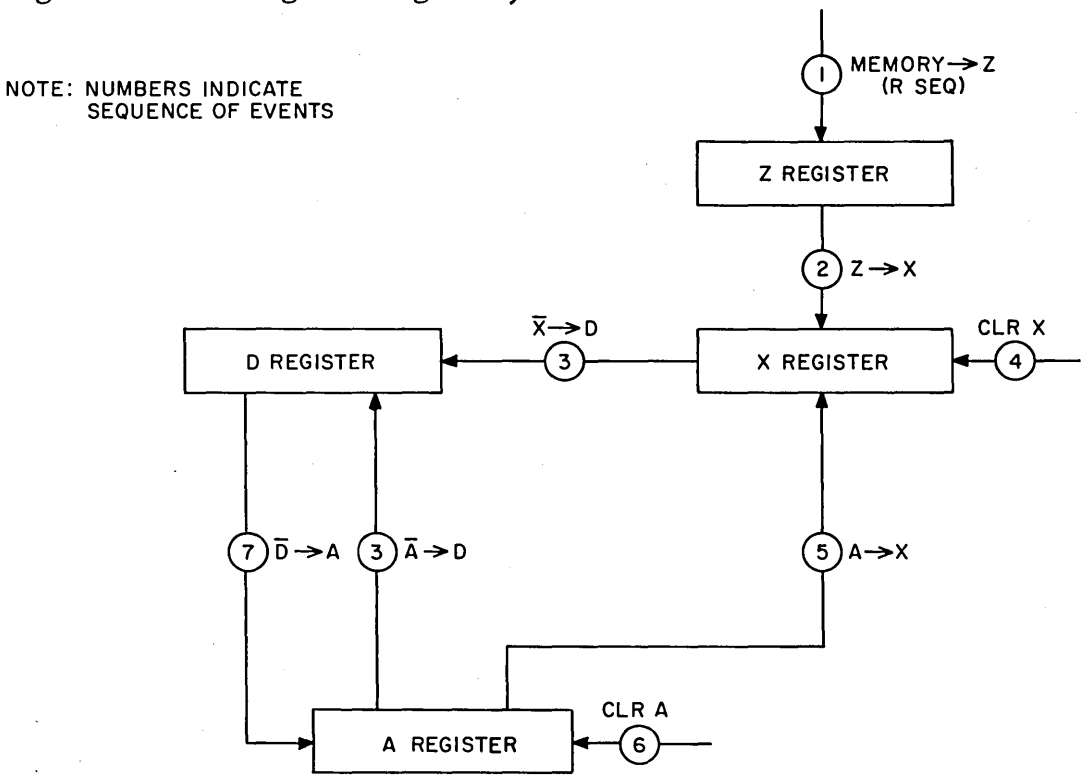


Figure 4-48. Logical Multiply, A-Register

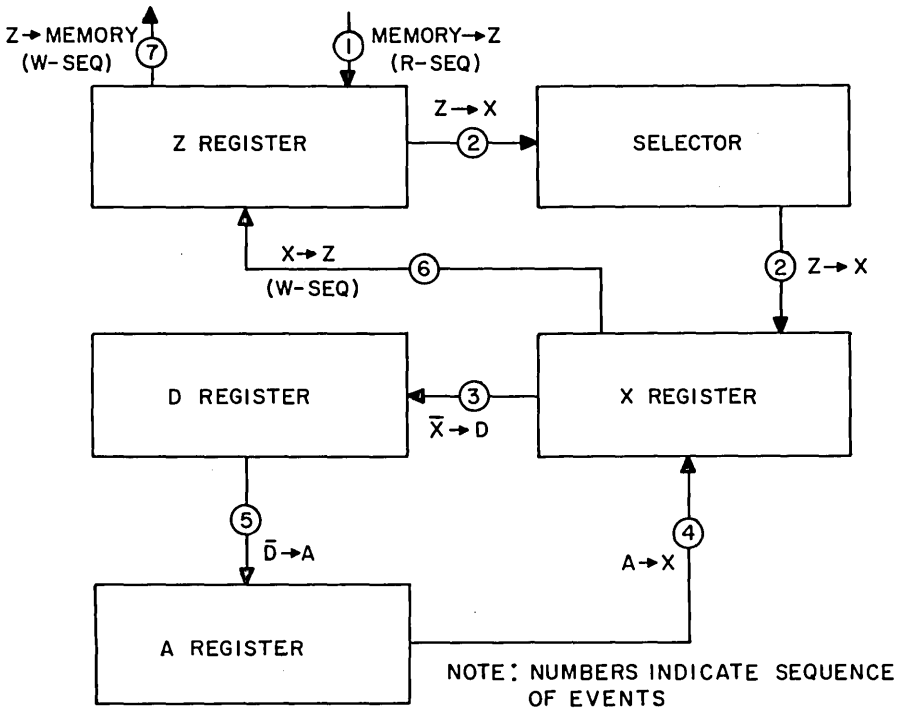


Figure 4-49. Exchange

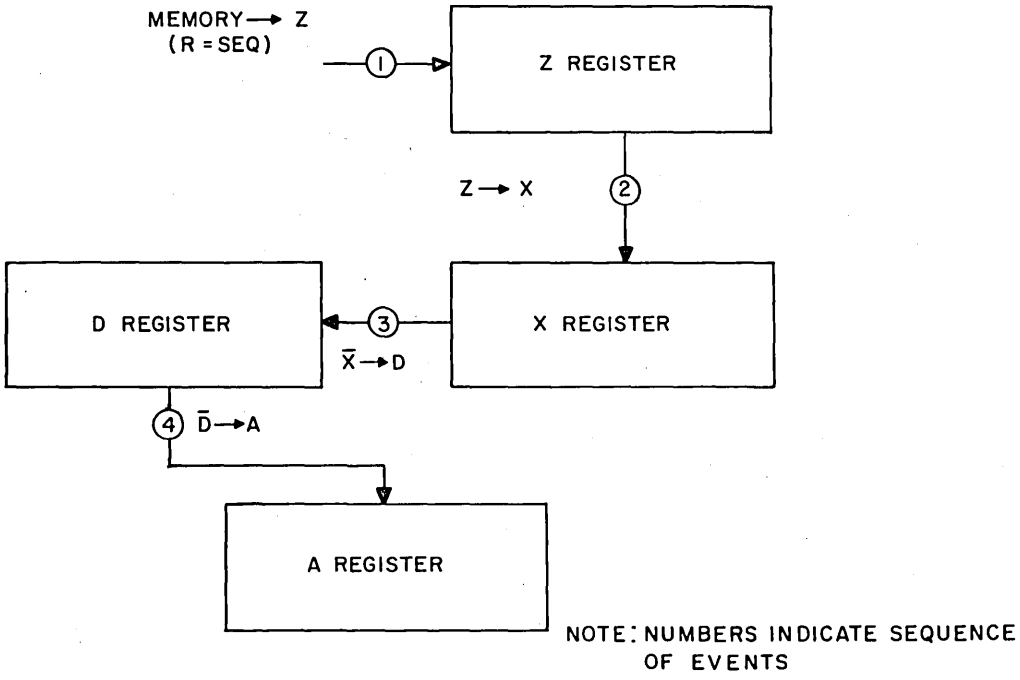


Figure 4-50. Clear Add

(15) Divide. - Figures 4-30 and 4-31, pages 4-68 and 4-69, show the divide operation.

4-18. INPUT/OUTPUT SECTION. - The computer has eight input/output channels that connect to peripheral equipments (figure 4-51, page 4-103). Table 4-13 lists the types of peripheral equipment.

The computer controls all peripheral equipments except the consoles. The consoles send data to the computer and request data from the computer. The computer controls all data transfers. For example, if the computer wants to send data to the TCU, the computer executes the 07 (EXF) instruction with a peripheral unit code that instructs the TCU unit to request data from the computer. If the computer wants to input data from the RD-277A unit, the computer executes the 07 (EXF) instruction with a peripheral unit code that instructs the RD-277A to read data into the computer.

Request signals from the peripheral equipment and acknowledge signals from the computer initiate data transfers between the computer and peripheral equipment. A request signal indicates that a peripheral equipment has data ready for transmission to the computer (input request) or can accept data from the computer (output request). An acknowledge signal is the computer response to a request signal. If the request was an input request, the acknowledge signal indicates that the computer has accepted the input data. If the request was an output request, the acknowledge signal indicates that the computer has placed data on the I/O lines for the requesting peripheral equipment.

TABLE 4-13. Peripheral Equipment

Input	Output	Input/Output
*Keyboard	PCU	TCU
*Switches	*Monitor printers	RD-277A (PTU)
*Time generator	*Control printers	Auxiliary computer
*Console data generator	*Status indicators	Consoles
*Spare device		
*Contained in console		

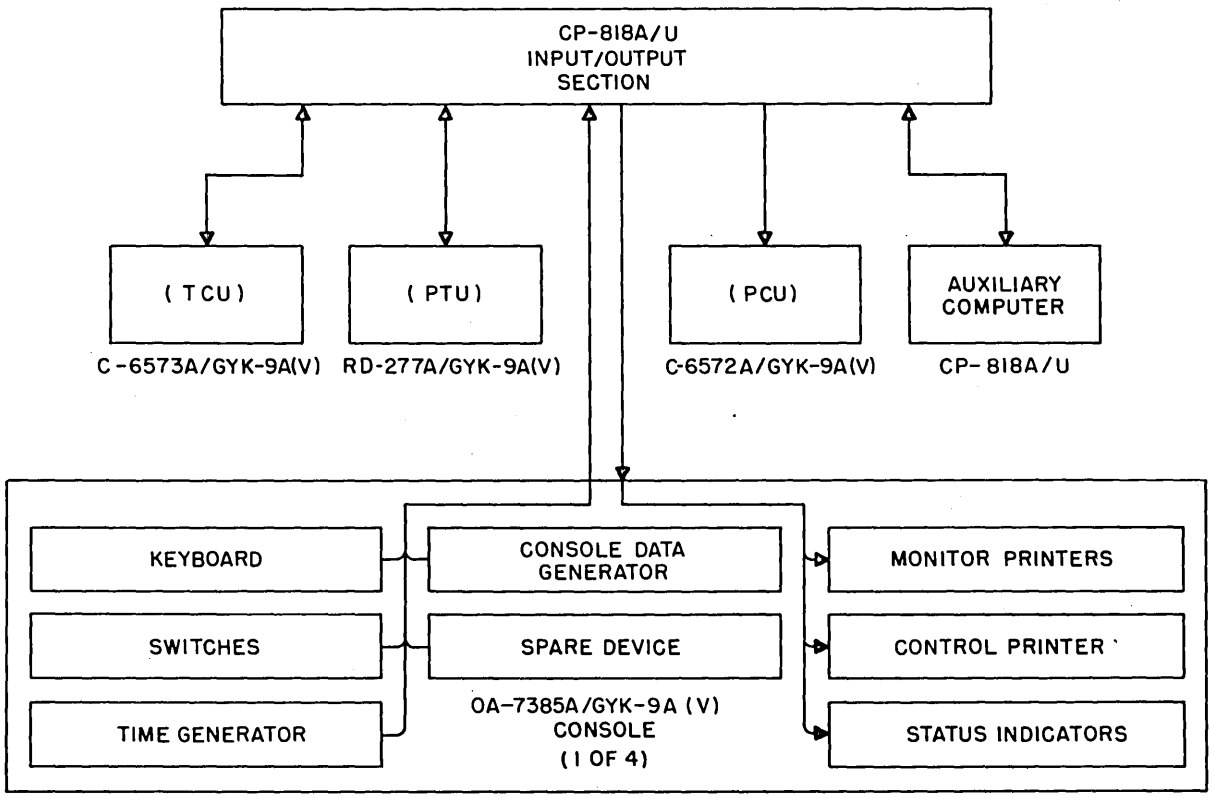


Figure 4-51. Peripheral Equipment

The input/output section monitors the request signals from the peripheral equipment. When a peripheral equipment has data for the computer or is requesting data from the computer, the input/output section sends an I/O enable to the control section. As soon as the current computer instruction is completed, the computer program stops and the peripheral equipments requesting data or sending data to the computer are serviced. Then the computer program resumes and continues until the input/output section detects another request from a peripheral unit.

a. Interface. - Figures 4-52 through 4-56, pages 4-105 through 4-107, show the data lines, control lines, and status lines between the computer and the peripheral equipment. The following paragraphs describe the lines common to all peripheral equipment.

(1) Data, request, and acknowledge lines. - All data lines carry input data to the computer or output data from the computer to the peripheral equipment.

The request lines carry request signals to the computer. A request signal from the PCU indicates that it is ready to accept a character from the computer. A request signal from the console indicates that the console either has a character for the computer or wants a character from the computer. The accompanying 5-bit address determines the type of request (input or output) and part of the control word address. All input request signals from the other equipments indicate that the peripheral equipment has placed a data character on the computer input lines. Output request signals indicate that the peripheral equipment can accept a data character from the computer.

The acknowledge lines carry acknowledge signals to the peripheral equipment. An acknowledge signal to the PCU indicates that the computer has a character for the PCU.

An acknowledge signal to the console indicates that the computer has either accepted an input character or placed an output character on the data lines to the console. The output acknowledge signals to the other peripheral equipment indicate that the computer has placed a data character on the output lines.

(2) Computer - TCU (figure 4-52, page 4-105).

1) Tape mark - indicates that the TCU read a tape-mark character from magnetic tape.

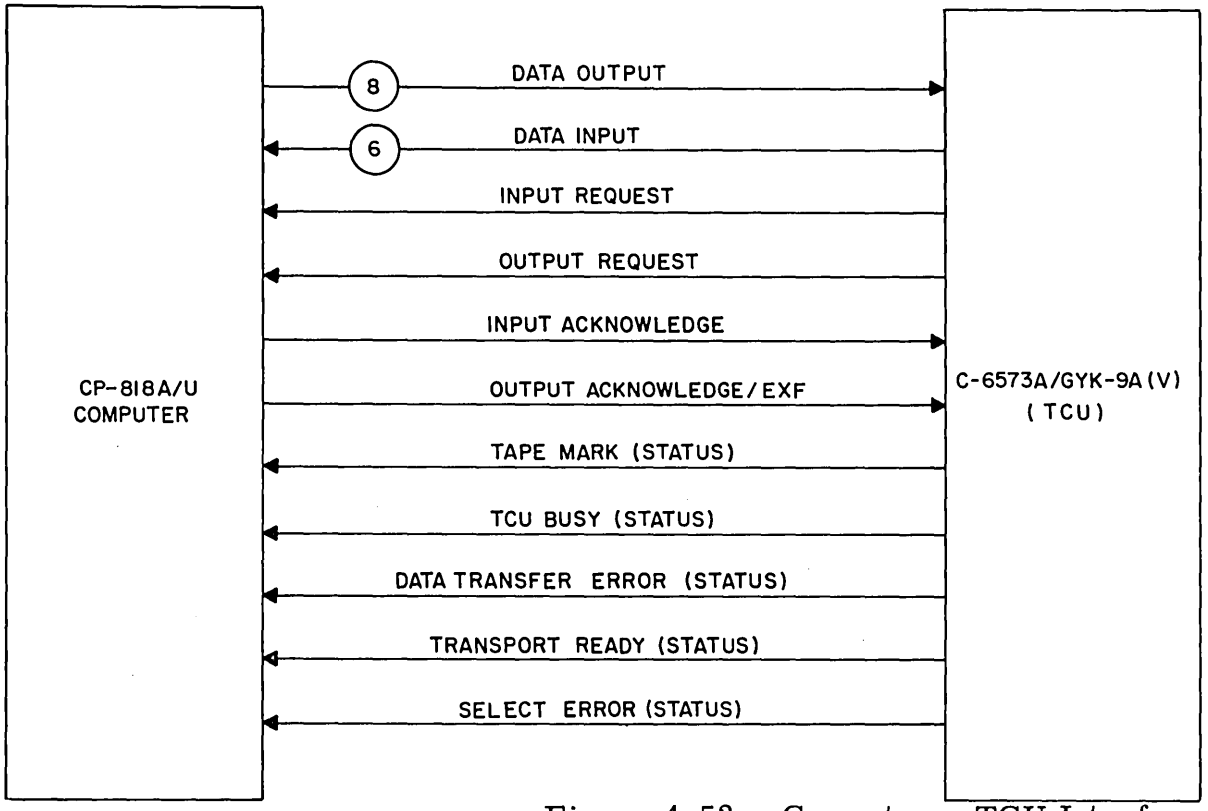


Figure 4-52. Computer - TCU Interface

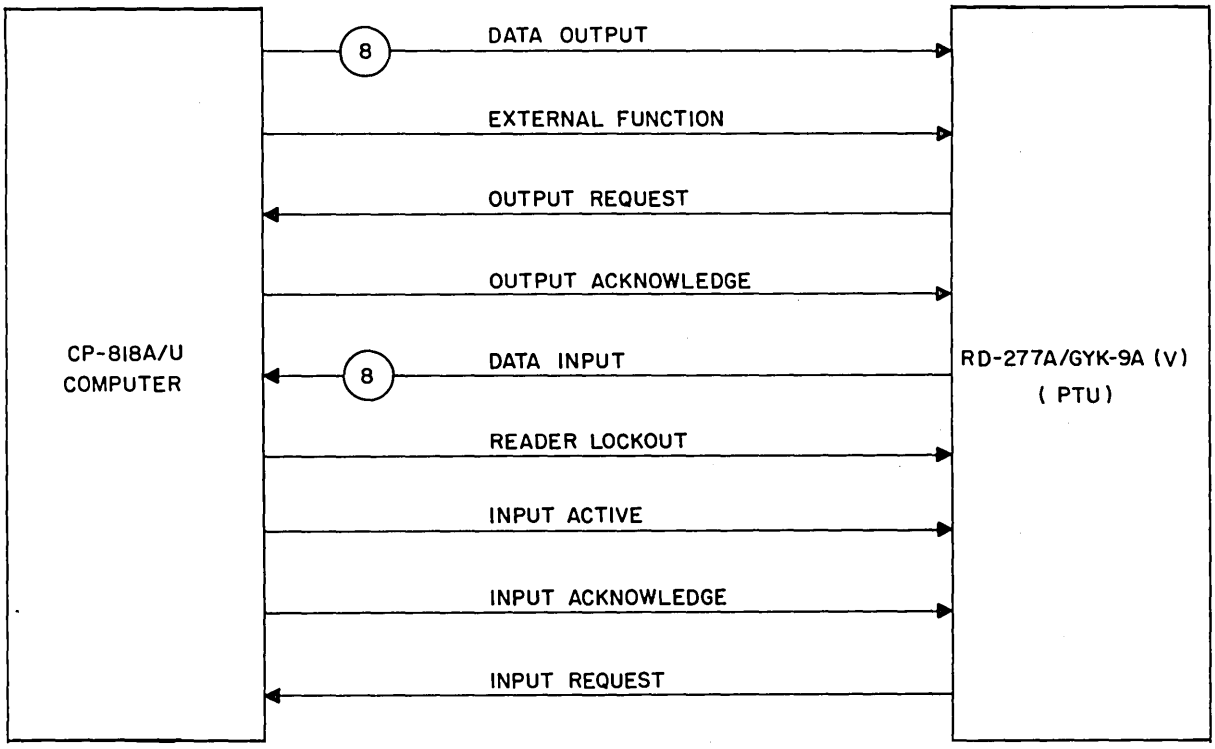


Figure 4-53. Computer - RD-277A Interface

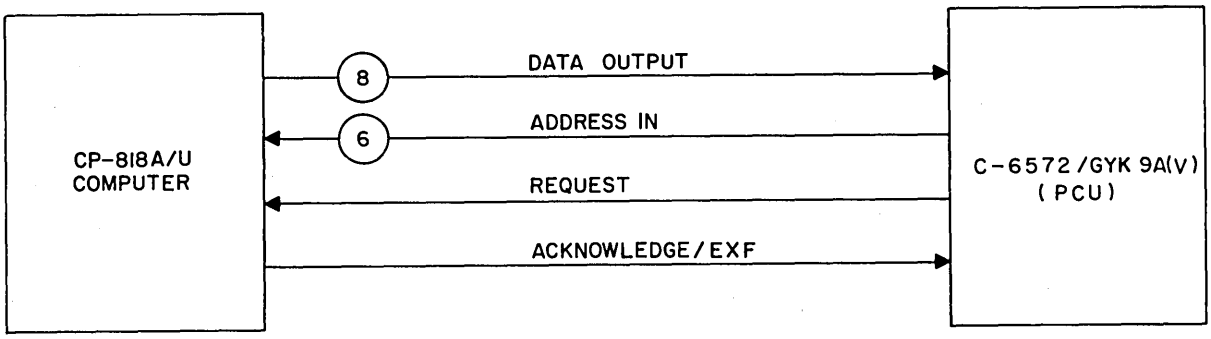


Figure 4-54. Computer - PCU Interface

2) TCU busy - indicates that the TCU is busy with an operation and cannot start a new one.

3) Data transfer error - indicates that the TCU detected an echo-check, output-timing, input-timing, read-parity, or output-parity error.

4) Transport ready - indicates that the tape transport selected by an external function can accept or send data.

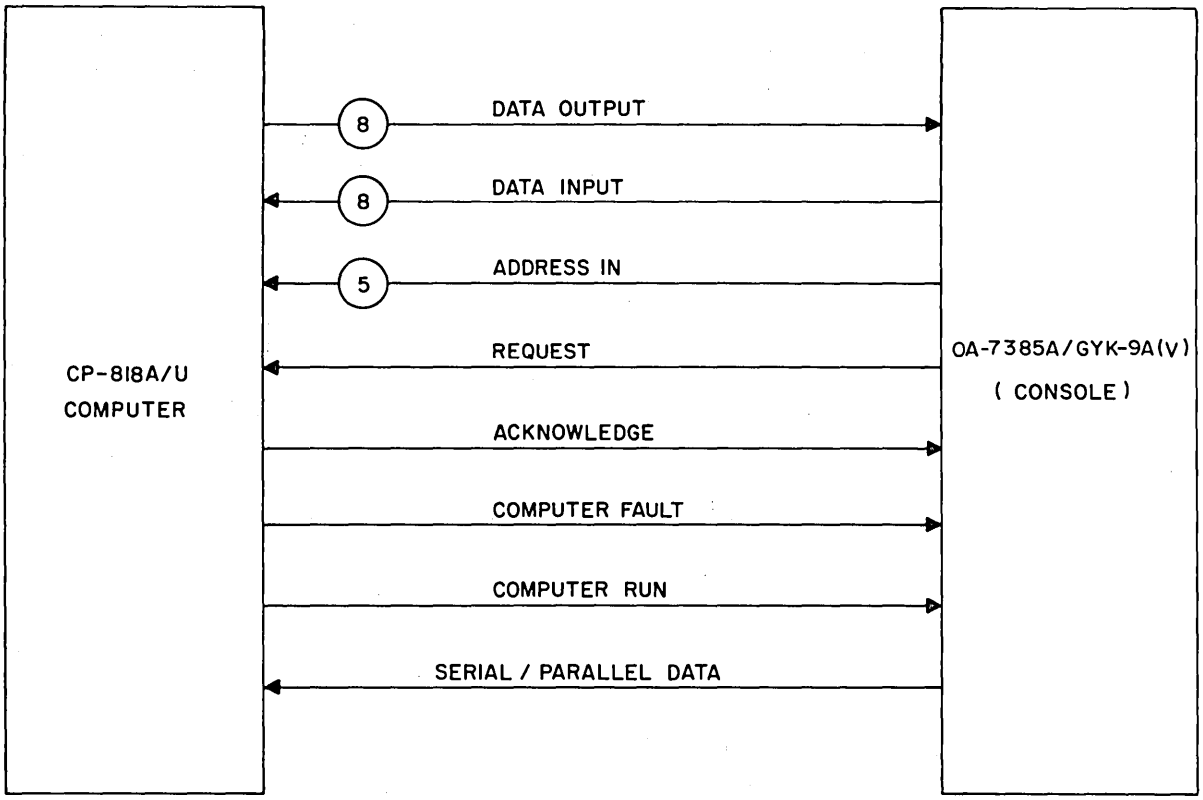


Figure 4-55. Computer - Console Interface

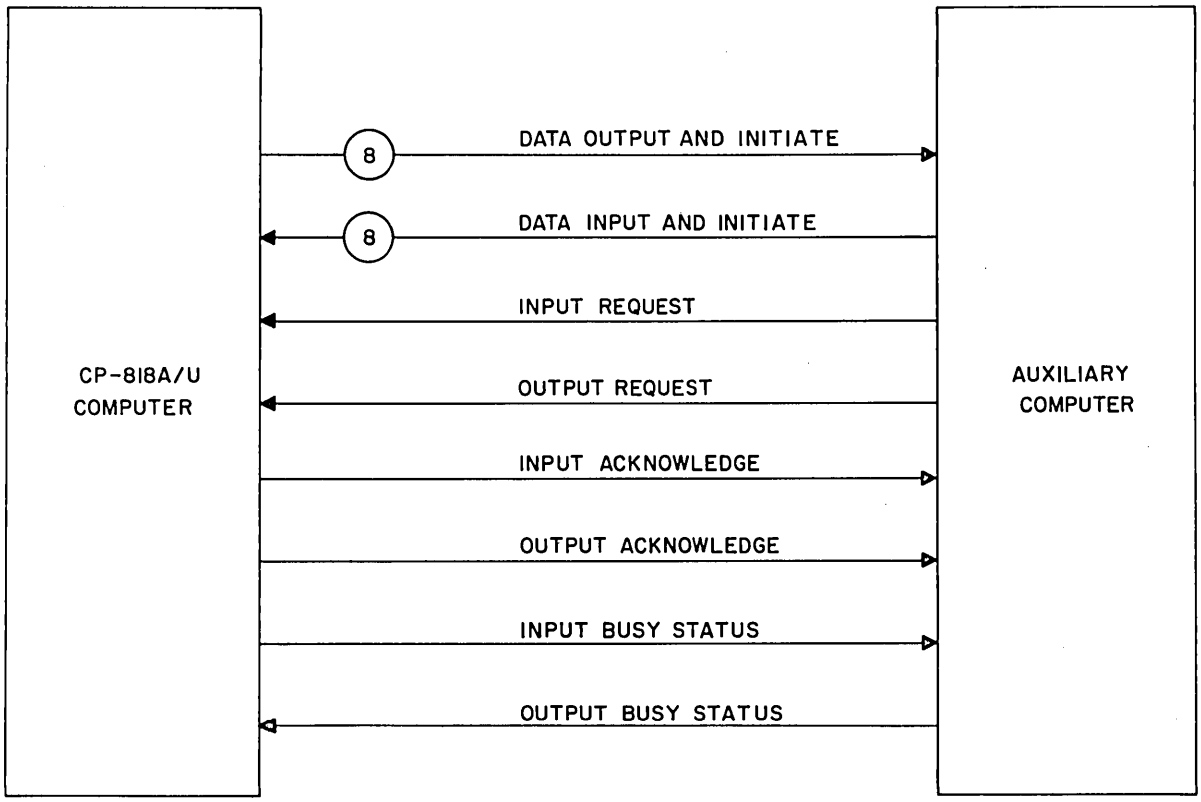


Figure 4-56. Computer - Auxiliary Computer Interface

5) Control error - occurs for any of three conditions: the computer instructs the TCU to perform an operation when the TCU is performing an operation; the computer instructs the TCU to perform a write operation on a tape transport that does not have a file protect ring on; or the computer instructs the TCU to perform an operation on a tape transport that is not ready for operation.

(3) Computer - RD-277A(PTU) (figure 4-53, page 4-105).

1) External function - indicates to the RD-277A that the information on the data lines is a function code and not a data character. The function code specifies the operation to be performed by the RD-277A.

2) Reader lockout - when present, the RD-277A stops when the input buffer is no longer active. The operator must then manually restart the reader for further reader operation.

3) Input active - indicates to the RD-277A that the input buffer memory area assigned to the RD-277A is not yet full.

(4) Computer - PCU (figure 4-54, page 4-106). - The address-in lines carry a 6-bit address to the computer when the PCU requests a character. This address specifies part of the memory address of the control word associated with the requesting punch. The address-in bits 2^0 through 2^5 specify bits 2^1 through 2^6 of the memory address.

(5) Computer - console (figure 4-55, page 4-106).

1) Address in - provide a 5-bit address to the computer when the console sends data to the computer or requests data from the computer. This address specifies part of the memory address of the control word associated with the request. The address in bits 2^0 through 2^4 specifies bits 2^1 through 2^5 of the memory address.

2) Computer fault - indicates to the console that one of the computer faults has occurred: halt, parity, console keyboard-overflow, console-data-overflow, and console-switch-overflow.

3) Computer run - indicates to the console that the computer is operating in the normal, high-speed run mode.

4) Serial/parallel data - a high signal (0v) indicates that the computer will accept console data in a parallel mode and store three 8-bit or four 6-bit console data characters in each memory location. A low signal (-6v) or an open line indicates that the computer will accept console data in a serial mode and store 24 one-bit, 12 two-bit, or 8 three-bit console data characters in each memory location.

(6) Computer - auxiliary computer (figure 4-56, page 4-107).

1) Initiate - indicates that the computer wants to send data to the auxiliary computer and sets the busy status line in the auxiliary computer. See paragraph 4-18c(3), page 4-150, for more information on this signal.

2) Busy status - accompanies the initiate signal and causes the auxiliary computer to return a busy status. Indicates to both computer programs that an I/O operation is in process.

b. Functional Sections. - Figure 4-57, page 4-110, is a functional block diagram of the input/output section.

(1) Input/output control. - The control section circuits generate most of the signals that control the operation of the input/output section.

(a) Scan timing (figure 8-68, page 8-151). - Scan timing generates the timing enables that gate input and output request signals from the peripheral equipment into the I/O request logic (figures 8-69 and 8-70, pages 8-153 and 8-155). Scan timing also disables the console translation logic during the time input and output requests enter the I/O request logic to prevent translation when the requests are changing. Scan timing consists of a scan flip-flop, request-enable circuits, and a console-translation-timing flip-flop.

The scan flip-flop determines when requests enter the I/O request logic. It sets at time 3.4 of most computer sequences. It does not set during the RC1 or RC2-sequences or when the computer operates in the function repeat condition. Also, the scan flip-flop does not set during the WC-sequence of a shift instruction, or R/W sequence when the buffer terminate flip-flop is clear and other conditions met. The scan flip-flop remains set for one clock cycle. During this time, it enables the request-enable circuits.

The request-enable circuits generate the signals that clear and load the I/O request circuits with the input and output requests from the peripheral equipment. The request-enable circuits generate the following signals.

Time	Function
4.2 of Scan	Clear Resync flip-flops
4.3 of Scan	Load Resync flip-flops
1.3 of R/W Sequence	Clear Resync One-Shot flip-flops

The console-translation-timing flip-flop disables the console translation logic (figure 8-77, page 8-169) during the time input and output requests enter the I/O request logic. It sets with the scan flip-flop and remains set for approximately two clock cycles.

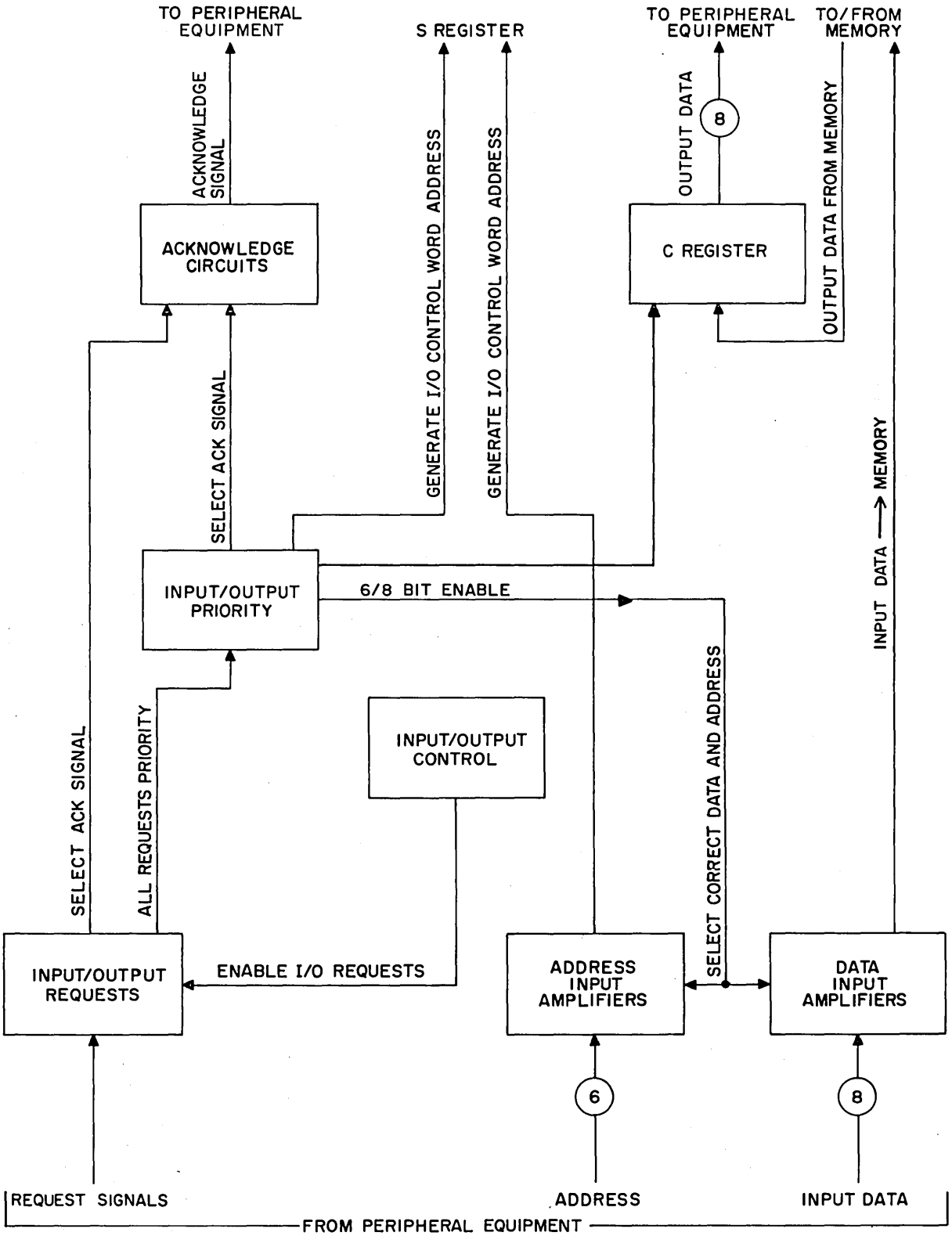


Figure 4-57. Input/Output Section, Functional Block Diagram

(b) Input/output control words. - Input/output control words specify where (memory locations) to store input data from peripheral equipment or where to extract output data for peripheral equipment. The control words also specify the size of the memory areas assigned to peripheral equipment. Since each memory location stores 24 bits of data and the peripheral equipment can send 1, 2, 3, 6, or 8-bit characters and receive 6 and 8-bit characters, the control words specify the number of peripheral equipment characters stored in or extracted from one memory location.

Table 1-3, page 1-15, lists the memory locations of the input/output control words assigned to each peripheral equipment. All peripheral equipment except the consoles and PCU have four input/output control words, two for input and two for output. When the memory area specified by the first control word is full (input) or emptied (output), the second control word is referenced. The second control word is transferred to the memory location of the first control word, and the memory location of the second control word is cleared. The memory location of the second control word can be loaded with another control word by the computer program. Each console has 100_8 control words for the input and output equipments shown in table 4-13, page 4-102. The PCU has two control words for each of 40 printers or punches. Figure 4-58, page 4-112, shows the format for three types of input/output control words.

Figure 4-58, page 4-112, shows the format for all of the input/output control words except those for the RD-277A and the console-data-input function when the computer is operating in the serial data mode (see paragraph 4-18b(9)(c), page 4-143). The address portion of the control word specifies the memory location in which input characters are to be stored or from which output characters are to be extracted. The word-count portion specifies the number of locations in memory assigned to a peripheral unit. For example, if the word count equals 25_8, the input/output control word specifies 21_{10} memory locations. The character-count portion of the control-word counts the number of characters written into or read from a 24-bit memory location. Each time the character count reaches 10_2, for 8-bit characters, or 11_2, for 6-bit characters, the control word is updated and the character count returned to 00.

Figure 4-58B, page 4-112, shows the format for the RD-277A control words. This control word contains a mode bit. When the mode bit equals zero, four 6-bit characters are stored in each memory location or extracted from each memory location before the control word is updated. When the mode bit equals one, three 8-bit characters are stored in each memory

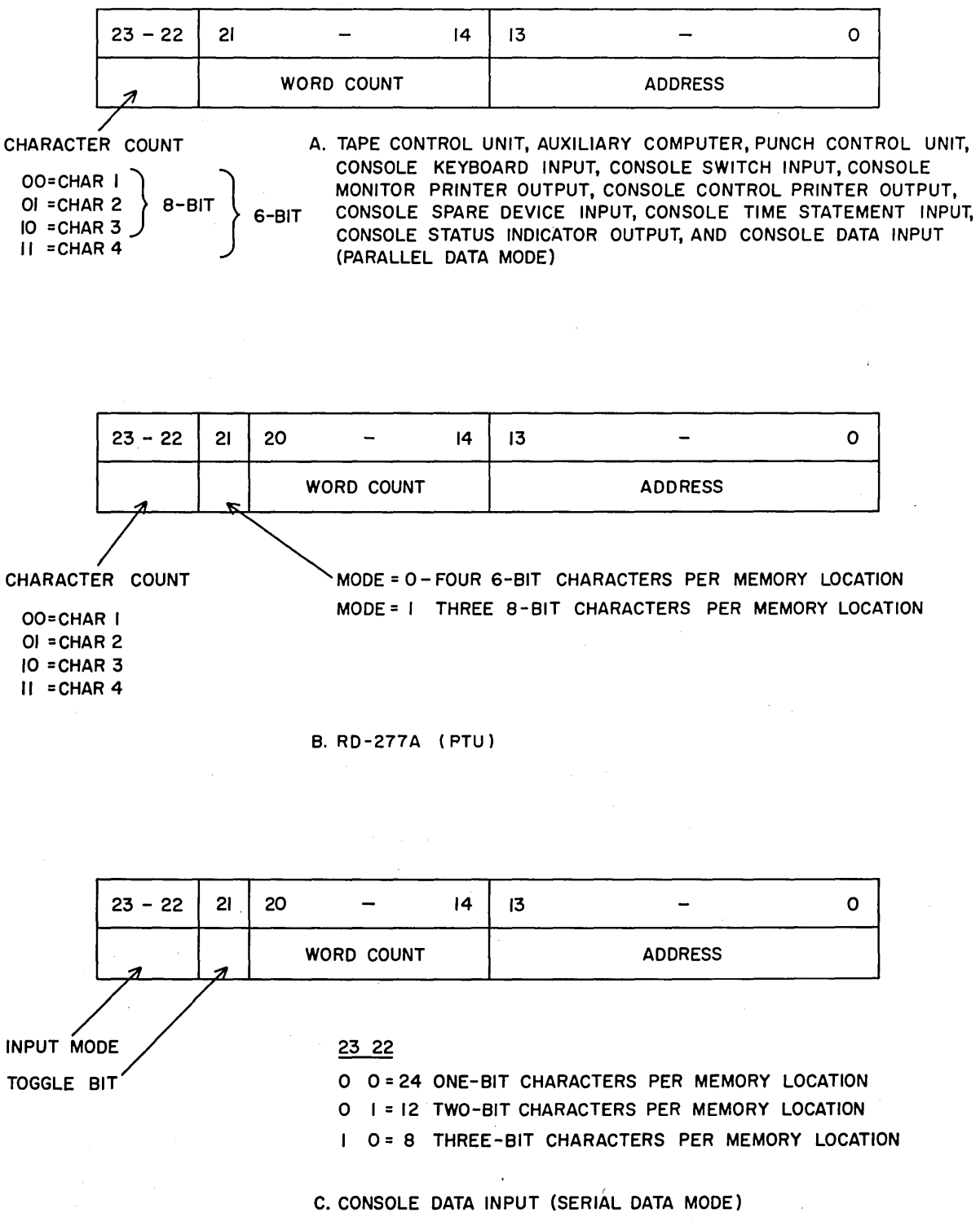


Figure 4-58. Input/Output Control Word Format

location or extracted from each memory location before the control word is updated.

Figure 4-58C, page 4-112, shows the format for the console-data-input control word when the input/output section is accepting console input data in the serial data mode. Bits 22 and 23 of the control word are input mode bits. When the input mode designator equals 00, the input/output section stores 24 one-bit characters of console data input in each memory location. When the input mode designators equal 01 the input/output section stores 12 two-bit characters of console data input in each memory location. When the designators equal 10, the input/output section stores 8 three-bit characters of console data input in each memory location.

(c) Input/output sequences. - The control section generates the input/output sequences. The input/output sequences are RC1, RC2, R/W, and WC. All input data transfers or output data transfers require at least an RC1 and R/W-sequence. Sometimes these data transfers require an RC1, R/W, and WC-sequence. Sometimes they require an RC1, RC2, R/W, and WC-sequence. No WC-sequence is required when the word-count field of CW2 reaches zero. Figure 4-59, page 4-114, shows the input/output sequences, when the different groups of sequences are required, and the general functions performed by each sequence. Tables 4-14 through 4-17, pages 4-115 through 4-122, contain detailed lists of I/O sequence functions. The following paragraphs describe when each group of sequences are used and the functions they perform. Each input data transfer or output data transfer always requires the RC1 and R/W- sequences. The RC1-sequence reads control word #1 from memory, adds one to the character-count portion of the control word, and restores it. The control word is gated to the X-register to provide required enables. The R/W-sequence either writes a character from the peripheral equipment into memory at the address specified by the control word or reads a character for the peripheral equipment from memory at the address specified by the control word. The character count determines in what portion of the memory location the input data is stored or what portion of the memory location is transferred to the peripheral equipment. After the R/W-sequence, the next input/output request is processed; or, if none are present, the computer program resumes and the next instruction is executed.

An input or output data transfer requires an RC1, R/W, and the WC-sequence when the character-count portion of the control word indicates that the memory location specified by the address portion of the control word

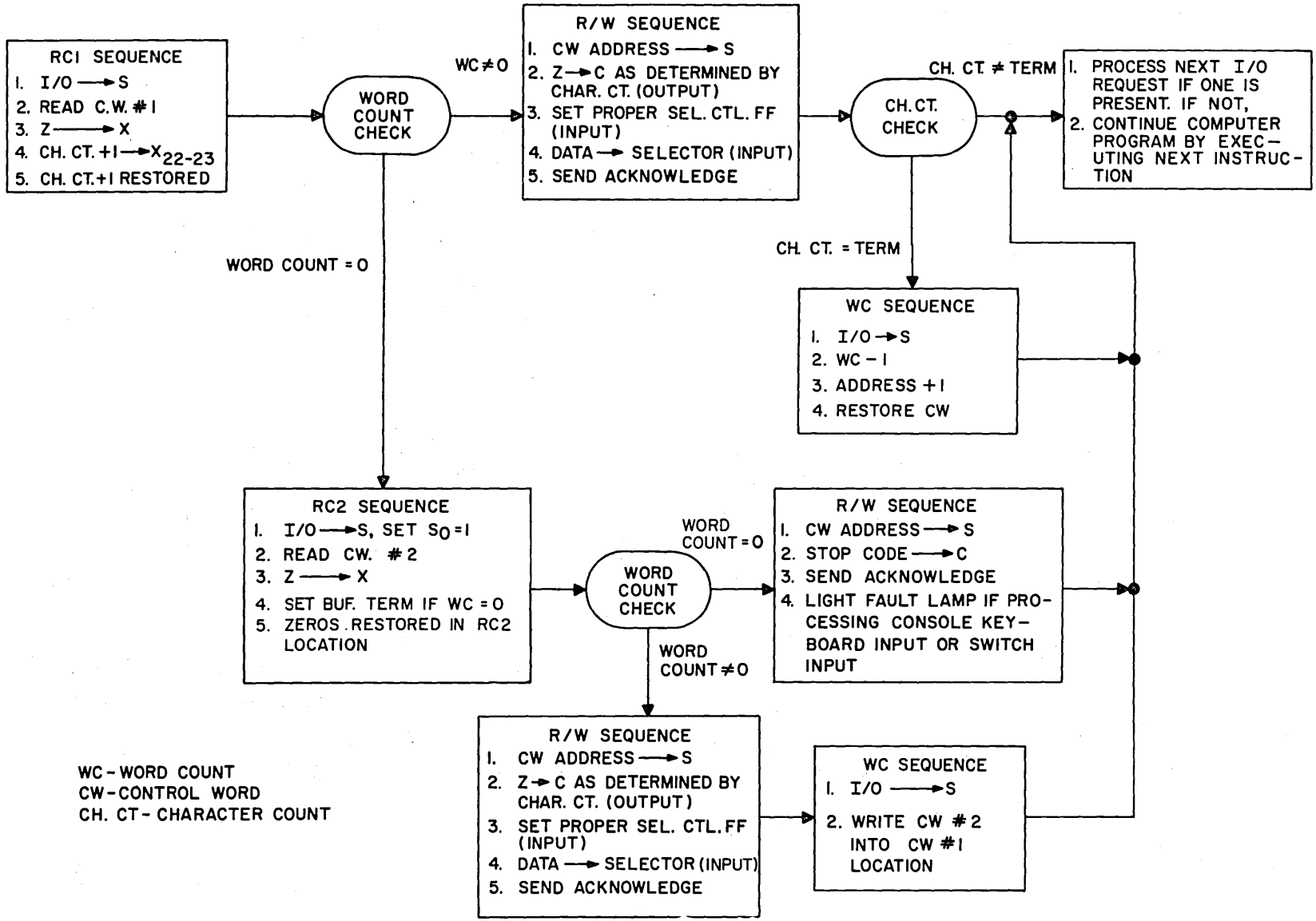


Figure 4-59. Input/Output Sequences

TABLE 4-14. RC1-Sequence

Time	Action	Conditions and Notes
4.3	Set appropriate resync flip-flop. Enable appropriate S-register bits 6, 7, and 8	If scan flip-flop, or request one-shot flip-flop set, and I/O request. If request is from PCU or console.
4.4	Clear scan flip-flop	Cleared every 4.4 time regardless of sequence type.
6.1	Set RC1-sequence enable flip-flop	If I/O request
6.4	Clear S and Z	
	Set console data flip-flop	Only for console serial data input request.
	Clear advance character count flip-flop	Cleared every 6.4 time regardless of sequence type.
1.1	I/O $\longrightarrow$ S	Control word address to S. For consoles and PCU the input address is added to the control word address.
1.2	Set RC1-sequence flip-flop	Set selector bit 21 if console data flip-flop set.
1.4	Set advance character count flip-flop	Disabled on console serial data inputs, interrupt, or if CW rewrite flip-flop is set.
2.2	Strobe (memory to Z)	Read control word 1
2.3	Clear X and D registers	

TABLE 4-14. RC1-Sequence (continued)

Time	Action	Conditions and Notes
3.3	$Z \longrightarrow X$	Control word to X.
	$Z_{23 - 22} + 1 \longrightarrow X_{23 - 22}$ (no increment if $Z_{21} = 1$)	
	Clear console-data-terminate flip-flop	
3.4	Disable set scan flip-flop	
	Enable write	Restore updated control word
4.2	Set console-data-terminate flip-flop	Only on console serial data input and $Z_{21} = 0$.
4.3	Set CSL switch flip-flop	Only on CSL switch input request when character count = 10_2.
4.4	Clear scan flip-flop	
5.4	Clear RC1-sequence enable flip-flop	
6.1	Set R/W-sequence enable flip-flop	If $Z_{14 - 21} \neq 0$.
	Set RC2-sequence enable flip-flop	If $Z_{14 - 21} = 0$ (buffer terminate flip-flop set).
	This sequence is initiated by all I/O requests and serves to read up control word #1. Control word formats are shown in figure 4-58, page 4-112. It is followed by an RC2-sequence if the word count (bits 14 through 21) is 0 or by an R/W-sequence if the word count is not 0.	

TABLE 4-15. RC2-Sequence

Time	Action	Conditions and Notes
6.4	Clear Z-register	
1.1	I/O $\longrightarrow$ S (set S_{00} flip-flop)	Address of control word 2.
1.2	Set RC2-sequence flip-flop	
	Clear RC1-sequence flip-flop	
	Enable all inhibits	
1.4	Set advance character count flip-flop	Disabled on console serial data inputs, interrupt, or if CW rewrite flip-flop is set.
2.2	Strobe (memory to Z)	Read control word 2
3.2	Clear X and D-registers	
3.3	Z $\longrightarrow$ X	Control word #2 to X. Memory location of control word 2 is cleared.
3.4	Disable set scan flip-flop	
	Inhibit write	Control word 2 location remains cleared.
4.2	Set console data terminate flip-flop	Only on console serial data input and $Z_{21} = 0$.
4.4	Set buffer terminate flip-flop	If $(\overline{INT} \cdot Z_{14-20} = 0 \cdot (Z_{21} = 0 +$ PTU REQ + CSL SDI REQ)
	Set 2^7 bit in C-register	$C = 200_8$ if $Z_{14-21} = 0$.

TABLE 4-15. RC2-Sequence (continued)

Time	Action	Conditions and Notes
4.4 (cont.)	Set data overflow flip-flop on next T33	If buffer terminate flip-flop is set and console data input.
	Clear scan flip-flop	
5.2	Set control-word-rewrite flip-flop	If buffer terminate flip-flop is cleared.
5.4	Clear RC2-sequence-enable flip-flop	
6.1	Set R/W-sequence enable flip-flop	
	This sequence is initiated only when the word count of control word #1 is 0 and upon the completion of an RC1-sequence. It serves to read up control word #2 so it can be placed at the address of control word #1.	

TABLE 4-16. R/W-Sequence

Time	Action	Conditions and Notes
6.4	Clear S and Z registers	
1.1	Adder to S	Buffer address.
1.2	Set R/W-sequence flip-flop	
	Clear RC1-sequence flip-flop	Or RC2-sequence flip-flop if following an RC2-sequence.
	Clear acknowledge flip-flops	

TABLE 4-16. R/W-Sequence (continued)

Time	Action	Conditions and Notes
1.3	Set appropriate acknowledge flip-flop	
	Clear appropriate request-one-shot flip-flop	If request is granted
	Enable data input gates	
1.4	Clear 6 bits in flip-flop and 8 bits in flip-flop	Both flip-flops are cleared every 1.4 time regardless of sequence type.
2.2	Strobe (memory to Z)	If console data terminate flip-flop clear or buffer terminate flip-flop set.
	Inhibit strobe	If console data terminate flip-flop set and BT flip-flop clear.
2.4	Set 8 bits in flip-flop (I_{0-7} to selector)*	If input request from RD-277A with X_{21} = 1 or CSL input in 8-bit mode and buffer terminate flip-flop is clear.
	Set 6 bits in flip-flop (I_{0-5} to selector)* *Placement in selector controlled by X_{22-23}.	If input request from RD-277A with X_{21} = 0, TCU, auxiliary computer, or CSL input in 6-bit mode and buffer terminate flip-flop clear.
	Set serial input flip-flop Enable data to selector mode 00 - 1 bit mode 01 - 2 bits mode 10 - 3 bits	Console data serial input only.

TABLE 4-16. R/W-Sequence (continued)

Time	Action	Conditions and Notes
2.4 (cont.)	Set selector bit 01 = 1 and inhibit memory to Z	If console data terminate flip-flop set and BT flip-flop clear.
3.2	Clear C-register	If buffer terminate flip-flop is set or CSL output, or any one of the following output acknowledge flip-flops are set: TCU, auxiliary computer, PCU and RD-277A.
	Clear control word rewrite flip-flop	If last character count is reached.
3.3	Z to C (as determined by character count)	
	$X_{22-23} = 01$ Z_{18-23} to C $X_{22-23} = 10$ Z_{12-17} to C $X_{22-23} = 11$ Z_{6-11} to C $X_{22-23} = 00$ Z_{0-5} to C or	If 6-bit output to TCU tape, auxiliary computer or RD-277A (6-bit mode).
	$X_{23-22} = 01$ Z_{16-23} to C $X_{23-22} = 10$ Z_{8-15} to C $X_{23-22} = 11$ Z_{0-7} to C	If 8-bit output to printer buffer, consoles, or RD-277A (8-bit mode).
	200_8 to C	If BT flip-flop is set.
3.4	Set scan flip-flop	If BT flip-flop is set or none of the conditions listed in time 6.1 exist.
	Enable write	

TABLE 4-16. R/W-Sequence (continued)

Time	Action	Conditions and Notes
4.2	Clear appropriate resync flip-flop	If scan flip-flop is set.
4.3	Set D_{14-23} flip-flops	If control-word-rewrite flip-flop is clear.
	Tally -1 enable	
	Address +1 enable	No forced end around borrow.
	Set appropriate resync flip-flop	If scan flip-flop and request one-shot flip-flop set and I/O request.
4.4	Clear scan flip-flop	
5.4	Clear R/W-sequence-enable flip-flop	
6.1	Set WC-sequence-enable flip-flop	If the buffer terminate flip-flop is cleared and one of the following exist: 1) 6-bit I/O and $X_{23-22} = 00$. 2) 8-bit I/O and $X_{23-22} = 11$. 3) Console data input and a) $Z_7 = 1$ and $X_{23-22} = 10$. b) $Z_{11} = 1$ and $X_{23-22} = 01$. c) $Z_{23} = 1$ and $Z_{23-22} = 00$. 4) Control-word-rewrite flip-flop set (by RC2 sequence).
	Set new sequence-enable flip-flop	If WC-sequence not enabled

TABLE 4-16. R/W-Sequence (continued)

Time	Action	Conditions and Notes
6.3	Set enable acknowledge flip-flop to send acknowledge to appropriate I/O device.	4-microsecond duration
	This sequence is initiated by the completion of an RC1-sequence when the word count is not equal to 0 or upon the completion of an RC2-sequence. It is followed by an I-sequence if the I/O control word does not have to be updated and no new request is waiting, or by a WC-sequence if updating is necessary.	

TABLE 4-17. WC-Sequence

Time	Action	Conditions and Notes
6.4	Clear S and Z registers	
	Clear BT flip-flop	Even if WC-sequence does not exist, BT flip-flop is cleared at T6.4 by the new sequence.
1.1	I/O $\longrightarrow$ S	S = address of control word #1 address incremented,
	Adder $\longrightarrow$ Z	tally decremented.
1.2	Set WC-sequence flip-flop	
	Clear R/W-sequence flip-flop	
	Set selector bit 21	If console-data-terminate flip-flop set and console data input request, or CSL data input request and Z_{21} = 1.

TABLE 4-17. WC-Sequence (continued)

Time	Action	Conditions and Notes
1.4	Set advance character count flip-flop	Disabled on console serial data inputs, interrupt, or CW rewrite flip-flop set.
	Clear serial input flip-flop	
2.4	Inhibit $Z_{23 - 22}$ to selector 23 - 22	If advance character count flip-flop is set.
3.2	Clear control-word rewrite flip-flop	
3.4	Set scan flip-flop	If not shift reload.
	Enable write	Rewrite updated control word (address incremented, word count decremented, and character count reset to 00_2).
4.2	Clear appropriate resync flip-flop	If scan flip-flop is set.
4.3	Set appropriate resync flip-flop	If scan flip-flop is set and I/O request.
5.4	Clear WC-sequence-enable flip-flop	
6.1	Set new sequence-enable flip-flop	I-sequence if no I/O request. RC1-sequence if I/O request.
	This sequence is initiated upon the completion of an R/W-sequence to update the control word or upon the completion of an RC2-sequence to transfer control word 2 to the address of control word 1 and clear memory location that held word 2.	

is full. The RC1 and R/W-sequences perform the same function as previously described. The WC-sequence increments the memory address by one, decrements the word count by one, and restores the updated control word in its memory location. After the WC-sequence, the next input/output request is processed; or, if none are present, the computer program resumes and the next instruction is executed.

An input or output data transfer requires an RC1, RC2, R/W, and WC-sequence when the word-count portion of control word #1 equals zero. This means that the memory area specified by the control word #1 is either full or all data in the memory area has been transferred out to the peripheral equipment. The RC1-sequence performs the same function as described previously. The RC2-sequence follows the RC1-sequence. This sequence reads control word #2 from memory, gates it to the X-register, and writes all zeros in the control-word #2 memory location. Control word #2 remains in the X-register during the WC-sequence. The R/W-sequence performs the same function as described previously. The WC-sequence writes the contents of control word #2 into the memory location for control word #1. Thus control word #2 becomes control word #1. If, during the RC2-sequence, the word count of control word #2 equals zero, the computer does not accept or send data to the requesting peripheral equipment. The following R/W-sequence differs from the normal R/W-sequence. Instead of storing or reading data for the requesting peripheral equipment, the R/W-sequence sends the 200_8 terminate code and, if the request was an input data transfer from a console keyboard, switches, or data generator, lights OVERFLOW indicators.

(d) Input/output timing. - The computer requires a minimum of 8 microseconds and a maximum of 16 microseconds for each input or output data transfer depending upon the status of the I/O control word. If the character-count portion of the control word does not indicate that the memory location specified by control word #1 will be filled or emptied, the time for one input or output operation is 8 microseconds, the time required for an RC1 and R/W-sequence. If the character count portion of the control word does indicate that the memory location specified by control word #1 will be filled or emptied, the control word needs updating and the time required for the input or output operation is 12 microseconds, the time required for an RC1, R/W, and a WC-sequence. If the word-count portion of control word #1 equals zero, a new control word is required. The time required for the input or output operation is 16 microseconds, the time required for an RC1, RC2, R/W, and a WC-sequence. If the word count portion of control word #2 equals zero, the following R/W-sequence sends a stop code 200_8 and terminates the operation. The time required

for the input or output operation is 12 microseconds (the time required for an RC1, RC2, and R/W-Sequence).

Figure 4-60, page 4-126, shows input/output timing for an 8-microsecond data transfer. The scan pulse (approximately 0.17 microseconds) occurs in every computer sequence (at 4.3 time) except when inhibited. If a request is present when a scan occurs, an input or output operation begins. If the request is an input request, the data is available before the request signal. After the scan pulse gates the request into the input/output section, the RC1-sequence begins, followed by the R/W-sequence. If the request is an output request, output data is placed on the output data lines near the middle of the R/W-sequence and remains on the output data lines until the next output data operation. At the middle of the R/W-sequence, the scan occurs again; and, if another request (from a different channel) is present, an RC1-sequence follows the R/W-sequence. Near the end of the R/W-sequence, the acknowledge signal occurs and remains for 4 microseconds. When the peripheral equipment detects the acknowledge signal, it drops the request and input data in preparation for its next input or output operation.

Figure 4-61, page 4-127, shows input/output timing for a 12-microsecond data transfer. This data transfer differs from an 8-microsecond data transfer in two ways.

1) A WC-sequence follows the R/W-sequence to update and restore the I/O control word.

2) The scan does not occur until the middle of the WC-sequence.

Figure 4-62, page 4-128, shows input-output timing for a 16-microsecond data transfer. This data transfer differs from an 8-microsecond data transfer in two ways also.

1) An RC2-sequence follows the RC1-sequence, and a WC-sequence follows the R/W-sequence.

2) The scan does not occur until the middle of the WC-sequence.

(2) Input/output requests (figures 8-69 and 8-70, pages 8-153 and 8-155). - The I/O request logic holds input and output requests from peripheral equipment and presents these requests to the I/O priority circuits (figure 8-71, page 8-157) until they are honored by the priority section. The

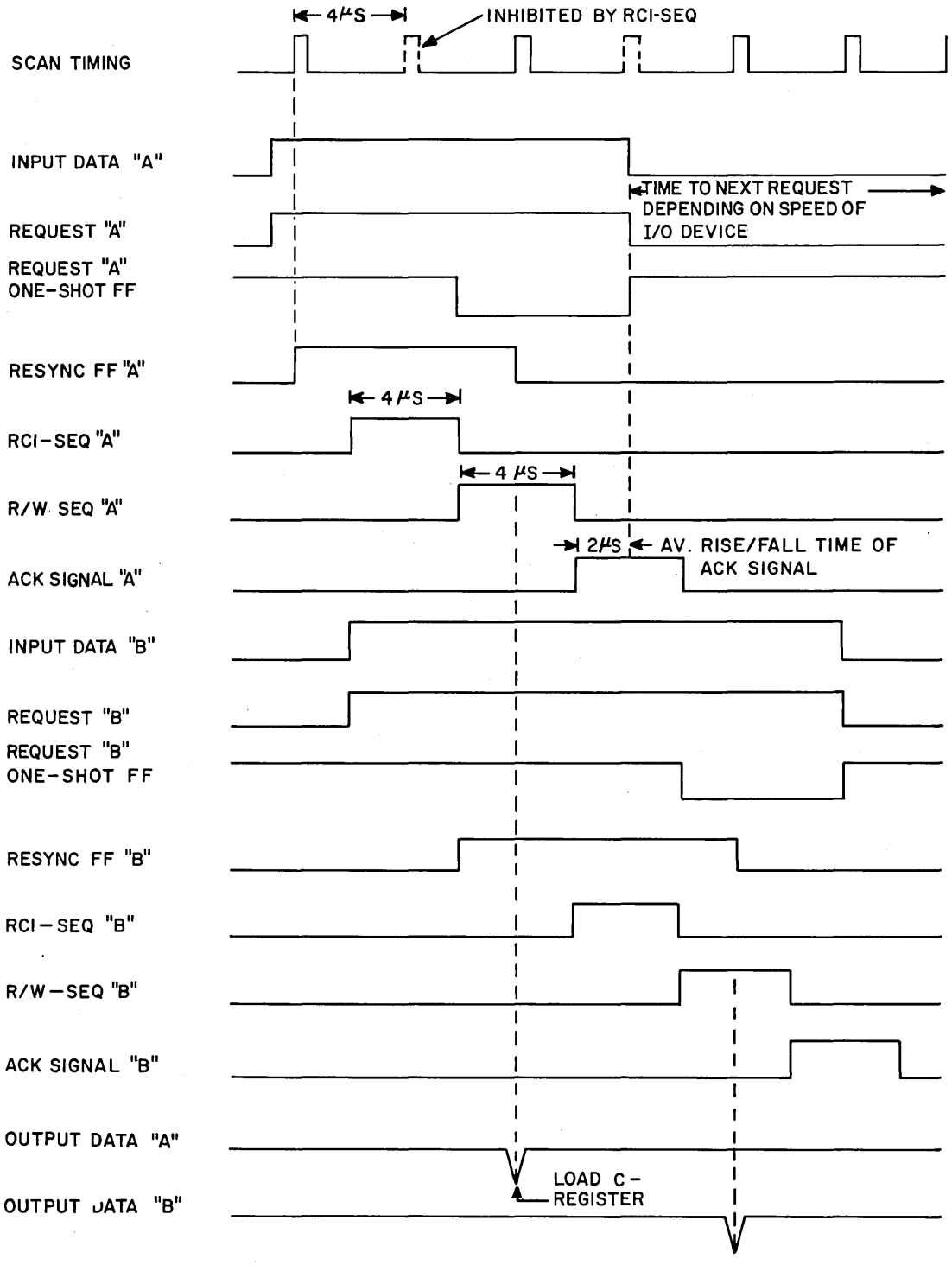


Figure 4-60. 8-Microsecond Data Transfer Cycle

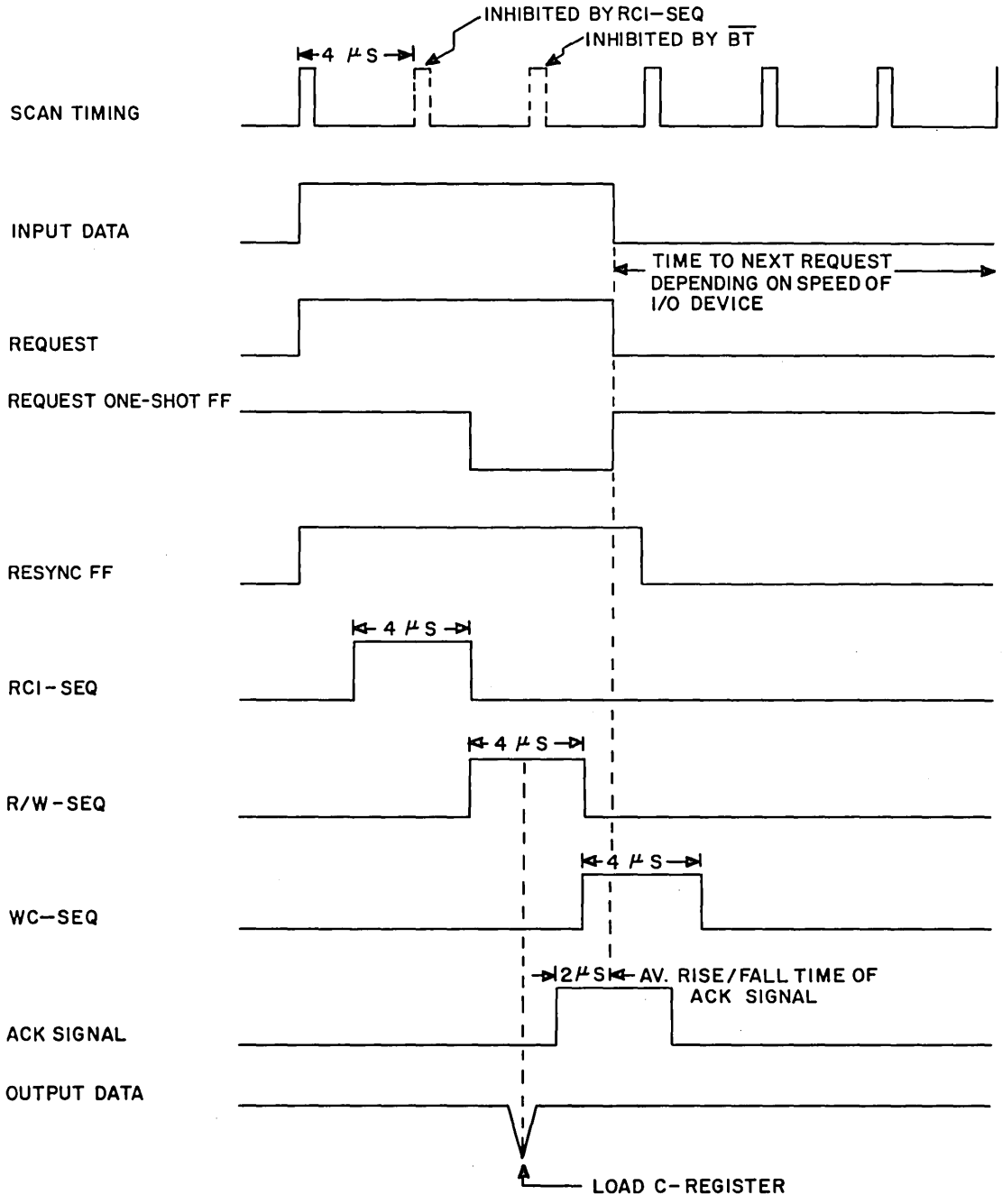


Figure 4-61. 12-Microsecond Data Transfer Cycle

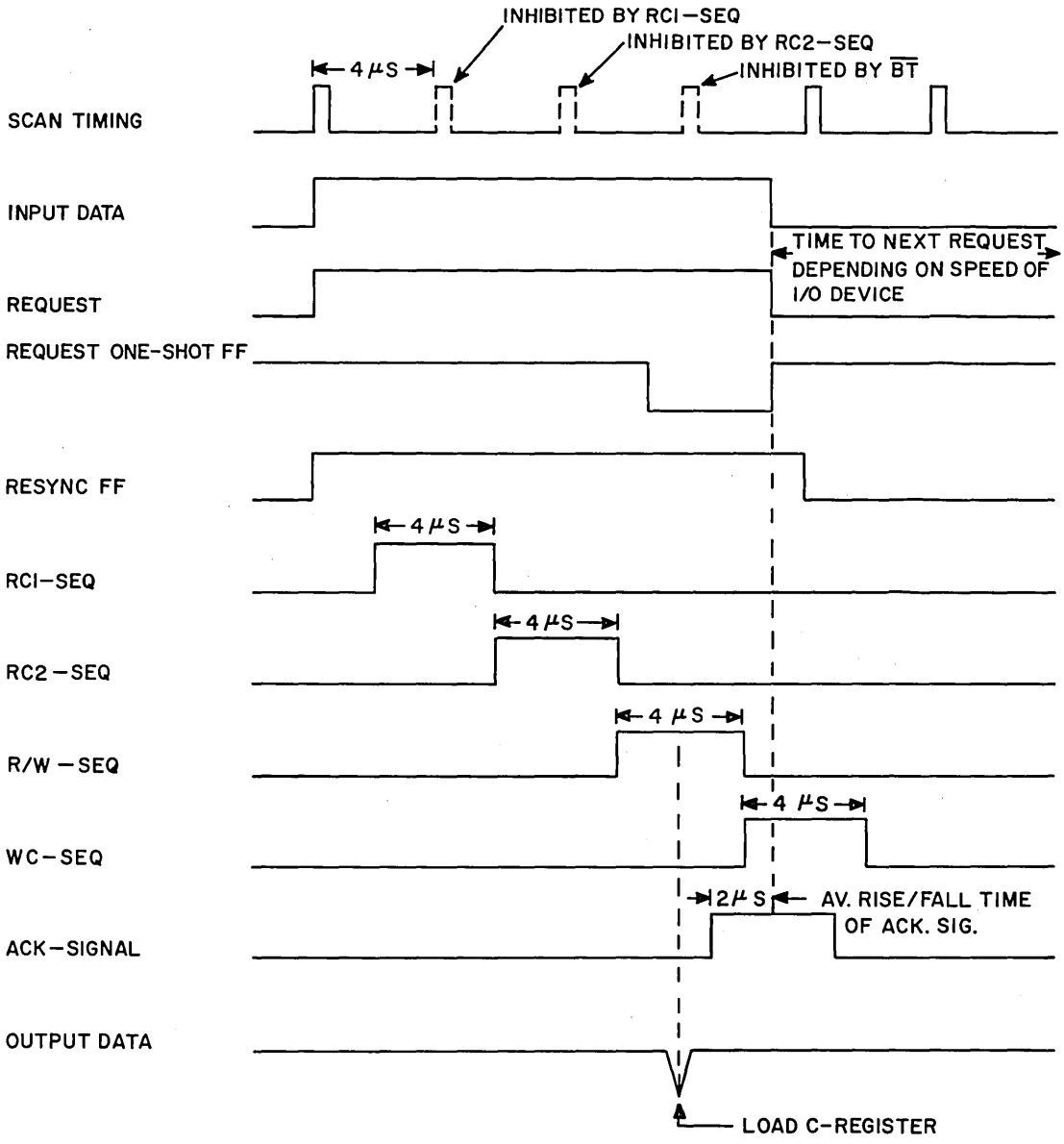


Figure 4-62. 16-Microsecond Data Transfer Cycle

I/O request logic consists of 11 request circuits, one for each request line from the peripheral equipment. Each request circuit consists of a request-one-shot flip-flop and a resync flip-flop. The following paragraphs describe each type of request circuit.

All request circuits shown on figures 8-69 and 8-70, pages 8-153 and 8-155, operate the same. This paragraph describes the TCU output request circuit. When the computer is master cleared or when no TCU-output-request signal is present, the request one-shot flip-flop sets. If the scan flip-flop is set (at time T3.4) when TCU sends an output request signal, the resync flip-flop sets at T4.3. Outputs from the resync flip-flop indicate to the I/O priority and other I/O circuits that TCU is requesting an output character. The request one-shot flip-flop remains set until the I/O section honors the request (no interrupt request present) at time 1.3 of the R/W sequence, or time 1.3 of the $\overline{WC/RCI_N}$ interrupt sequence. The resync flip-flop clears at time 4.2. The request-one-shot flip-flop remains clear until the TCU output request signal drops. This ensures that each TCU output request signal is recognized only once no matter how long it remains. When the TCU output request signal drops, the request-one-shot flip-flop sets and the request circuit is ready for the next TCU output request signal.

There are two differences between the operation of the RD-277A (PTU) input request circuit and the TCU output request circuit.

1) The computer program must execute a 07 (EXF) instruction specifying a paper tape input before the PTU input request circuit accepts the request signals.

2) While the computer executes an external function instruction specifying a paper tape input, the PTU input request circuit is disabled.

A comparison between the operation of the PTU output request circuit and the TCU output request circuit is similar since the PTU input and output request circuits operate in the same manner.

1) The computer program must execute a 07 (EXF) instruction specifying a paper tape output before the PTU output request circuit accepts PTU output request signals.

2) While the computer executes an external function instruction for the RD-277A, the PTU output request circuit is disabled.

The auxiliary-computer-output and auxiliary-computer-input request circuit operations differ from that of the other request circuits. This paragraph describes the auxiliary-computer output request circuit. Assume that the request circuit is in the initial state (both flip-flops clear). The auxiliary-computer-request-one-shot flip-flop sets when an auxiliary-computer-output-request signal is present and the computer is conditioned for intercomputer operation. At time 4.3 of the scan cycle, the resync flip-flop sets. Outputs from the resync flip-flop indicate to I/O priority and other input/output circuits that the auxiliary computer wants a character from the computer. The request circuit remains in this state until the input/output section honors the request. Then at time 1.3 of the R/W-sequence, when the character is read from memory, the request-one-shot flip-flop clears, and at time 4.2, the resync flip-flop clears. The request-one-shot flip-flop sets again as soon as the next auxiliary-computer output-request signal occurs.

(3) Input/output priority (figure 8-71, page 8-157). - The I/O priority logic monitors request circuit outputs, and determines which request is honored first if more than one are present. The I/O priority logic also helps generate the addresses of I/O control words. The priority of the input/output system is as follows.

1) Time base interrupt

2) TCU output

3) TCU input

4) Console 0

5) Console 1

6) Console 2

7) Console 3

8) RD-277A (PTU) input

9) RD-277A (PTU) output

10) PCU

11) Auxiliary computer output

12) Auxiliary computer input

In addition to indicating which input or output operation has been selected, outputs from the I/O priority logic perform the following functions.

1) A group of outputs enables the appropriate input data gates to gate data into the computer during an input request.

2) Another group of outputs (if a console or PCU request is honored) enables the appropriate address input amplifiers to gate an address into the computer.

3) An output to the appropriate request circuit clears it.

4) An output to the acknowledge circuits sets the proper input or output acknowledge flip-flop to generate the peripheral equipment acknowledge signal.

5) Outputs to the address input amplifiers and S-register help generate the I/O control word address.

(4) Address input amplifiers (figures 8-72 and 8-73, pages 8-159 and 8-161). - The address-input-amplifier circuits gate the addresses from the consoles and PCU to the address circuits to generate control word addresses.

With each request the consoles send a 5-bit address to identify the origin of the request. The PCU sends a 6-bit address with each output request to specify which punch wants an output character. When I/O priority honors a request from a console or the PCU, it generates an enable signal that gates the appropriate address into the input/output section. These addresses help generate the address of the I/O control word. Table 1-3, page 1-15, lists the assigned control word memory addresses that are generated by the I/O priority outputs and the outputs from the address input amplifiers.

Address-input-amplifier circuits 51I01 through 51I06 and 24V08 encode the output from the address input amplifiers and some of the I/O priority outputs into a control word address. This address goes to the S-register to specify part of the control word address associated with the input or output operation being processed. The address-input-amplifier circuits also gate in the serial/parallel control signal from the consoles and route this signal on to the console I/O translation logic (figure 8-77, page 8-169). Outputs

from the address input amplifiers also go to the console I/O translation logic described in paragraph 4-18b(9)(b), page 4-143).

(5) Data input amplifiers (figures 8-74 through 8-76, pages 8-163 through 8-167). - The data input amplifiers gate data from the peripheral equipment into the input/output section. The peripheral equipments sending input data are consoles, TCU, and RD-277A. The consoles send 1, 2, 3, 6, or 8-bit characters to the computer. The RD-277A sends 6 or 8-bit characters, as required by the computer program. The TCU sends 6-bit characters. Characters enter the input/output section via the data input amplifiers at time 1.3 of the R/W-sequence. The origin of the character that enters depends upon which input request I/O priority honors. For example, if priority honors an input request from console 3, the data input amplifiers for console 3 are enabled and the character enters the input/output section. After a character enters the input/output section, it is stored in memory.

Each memory location stores 24 bits of data. Thus, each memory location can store 3 eight-bit input characters, 4 six-bit input characters, 8 three-bit characters, 12 two-bit characters, or 24 one-bit characters.

Figure 4-63, page 4-133, shows how 8-bit input characters enter memory. During time 1.3 of the R/W sequence, an 8-bit character enters the input/output section via the data input amplifiers. The character-count portion of the I/O control word (in the X register, loaded by the previous RC1-sequence) determines which bits of the selector the input character enters. If no previous characters have been stored in the memory location, the input character is transferred to bits 2^{16} through 2^{23} of the selector. If one character has already been stored in the memory location, the input character is transferred to bits 2^{8} through 2^{15} of the selector; and if two characters have already been stored in memory location, the input characters enter bits 2^{0} through 2^{7} of the selector. During the R/W-sequence the contents of the selector are returned to memory. When the memory location contains three 8-bit characters, the I/O control word is updated, and a new memory location is referenced for the next input character.

Figure 4-64, page 4-134, shows how 6-bit input characters enter memory. The same procedure is used but the character counts and character placement in the word are different.

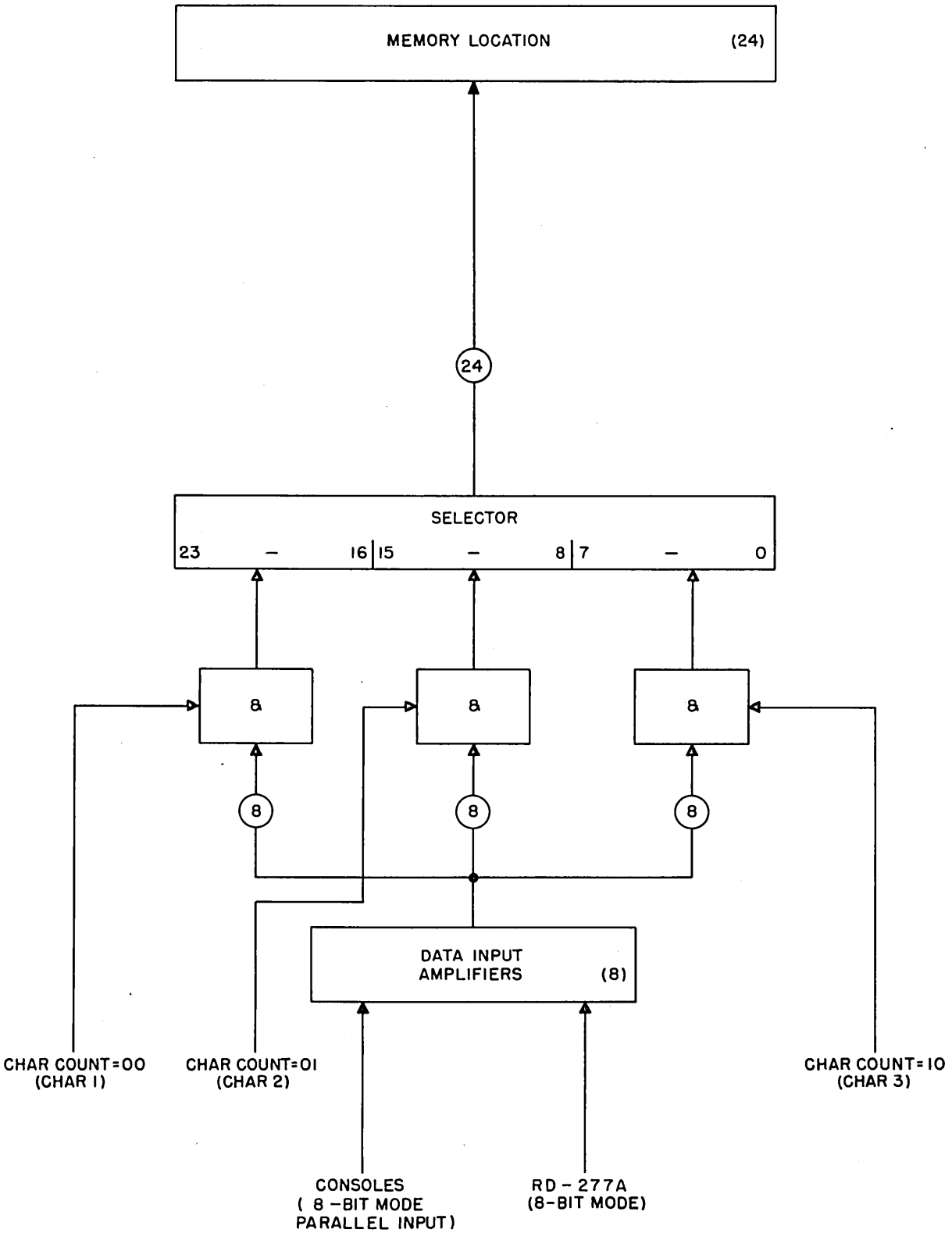


Figure 4-63. Input Data Path, Consoles and RD-277A

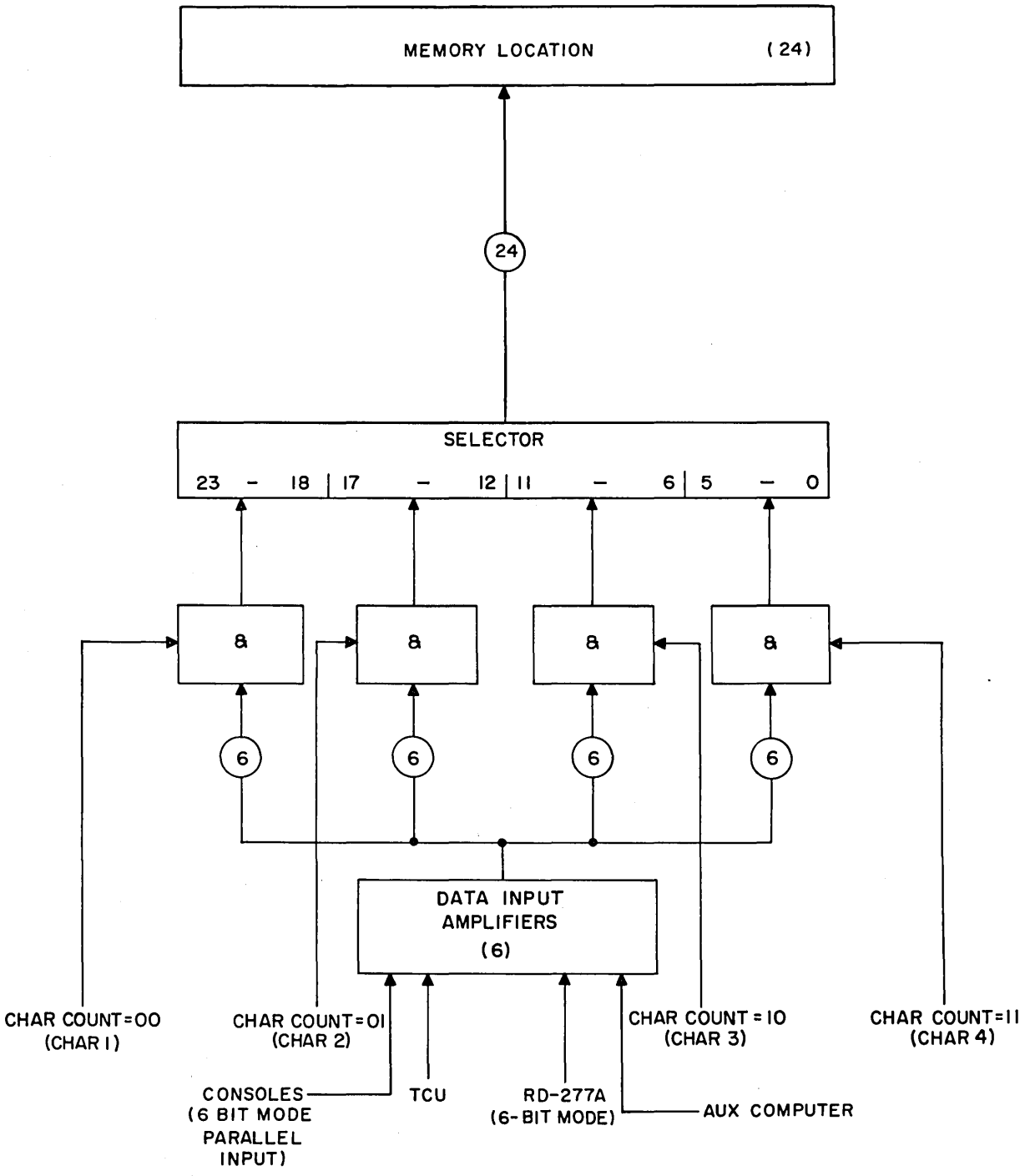


Figure 4-64. Input Data Path, Consoles, TCU, RD-277A, and Auxiliary Computer

(6) C-register (figures 8-82 through 8-84, pages 8-179 through 8-183). - The C-register is an 8-bit output register shared by all peripheral equipment. It temporarily stores characters transferred from computer memory to the peripheral equipment. The C-register has inputs from the Z-register, the buffer-terminate detector (figure 8-87, page 8-189), and the parity circuits (figures 8-66 and 8-67, pages 8-147 and 8-149). The inputs from the Z-register consist of two groups of inputs. One group of inputs transfers three 8-bit characters per memory location to the peripheral equipment. The other group transfers four 6-bit characters per memory location to the peripheral equipment. An input from the buffer-terminate detector generates a terminate code of 200_8 when all characters in the memory area assigned to the peripheral equipment requesting data have been transferred. The parity input from the parity check circuits adds odd parity to all 6-bit characters transferred to the peripheral equipment.

The C-register enable logic (figure 8-82, page 8-179) generates the signals that clear the C-register and load it with the proper part of the data in the Z-register. The C-register clears at time 3.2 of an R/W or R-sequence of the 07 (EXF) instruction. A data character is loaded into the C-register at time 3.3 of the R/W-sequence. An external function character is loaded into the C-register at time 3.3 of the R-sequence. The character-count portion of the control word determines which character in a memory location is transferred to the C-register. The C-register-enable logic monitors the character count and the peripheral equipment requesting data and generates the enable signals to gate the appropriate character into the C-register.

Figures 4-65 and 4-66, pages 4-136 and 4-137, show the data path of 6 and 8-bit characters transferred from memory to the peripheral equipment. Figure 4-65, page 4-136, shows that when the character count portion of the I/O control word equals 00, bits 16 through 23 of the memory location specified by the I/O control word transfer to the peripheral equipment requesting the character. When the character count equals 10, the last character of the specified memory location (bits 0 through 7) transfers to the peripheral equipment. The I/O control word is then updated. The character count returns to 00, the word count is decremented by one, and the address is incremented by one. When the computer executes a 07 (EXF) instruction, the C-register-enable logic simulates a character count of 10, and bits 0 through 7 of the instruction are sent to the specified peripheral equipment as a control character.

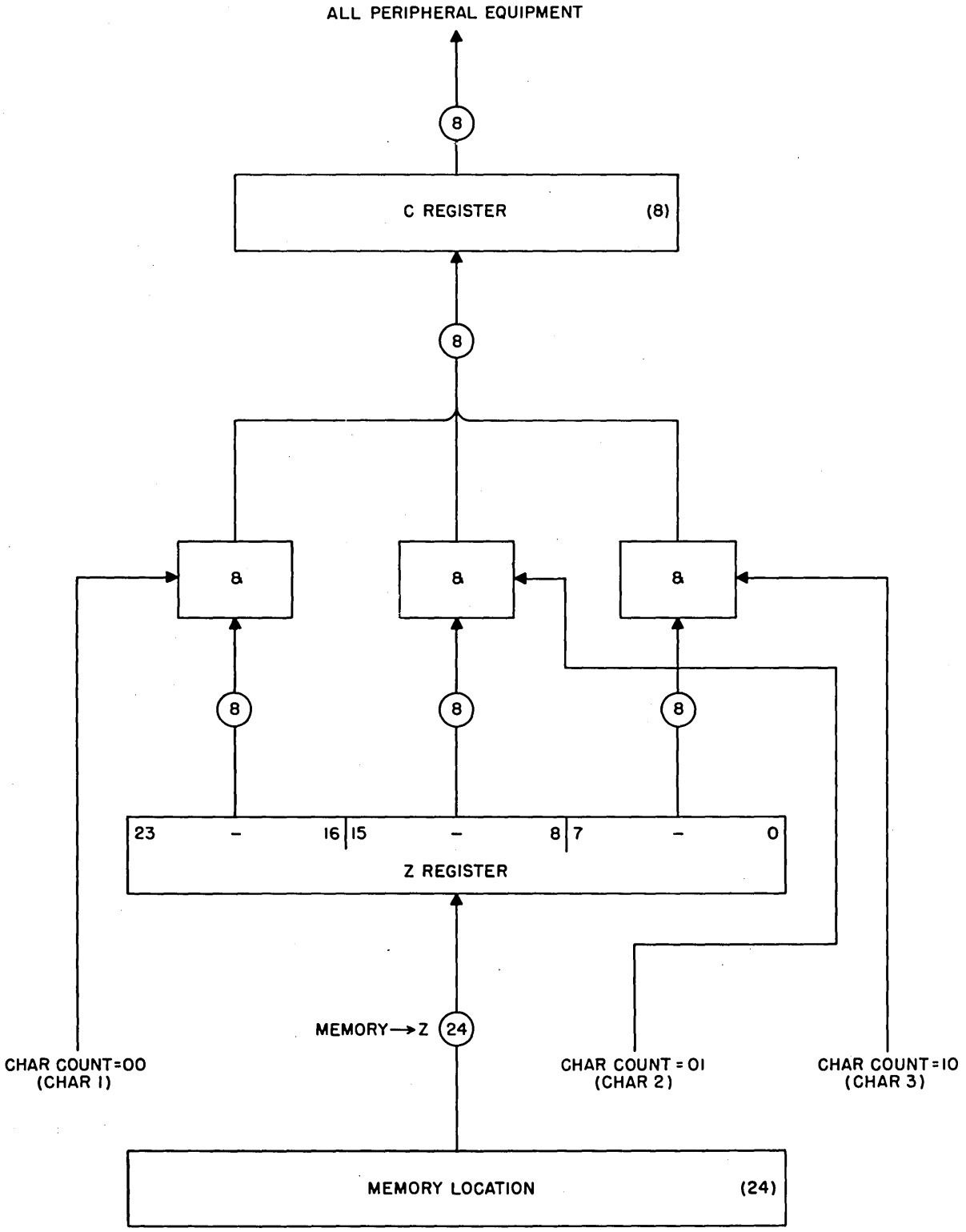


Figure 4-65. Output Data Path, Console, PCU, RD-277A (8-Bit Mode), Auxiliary Computer (EF), and TCU (EF)

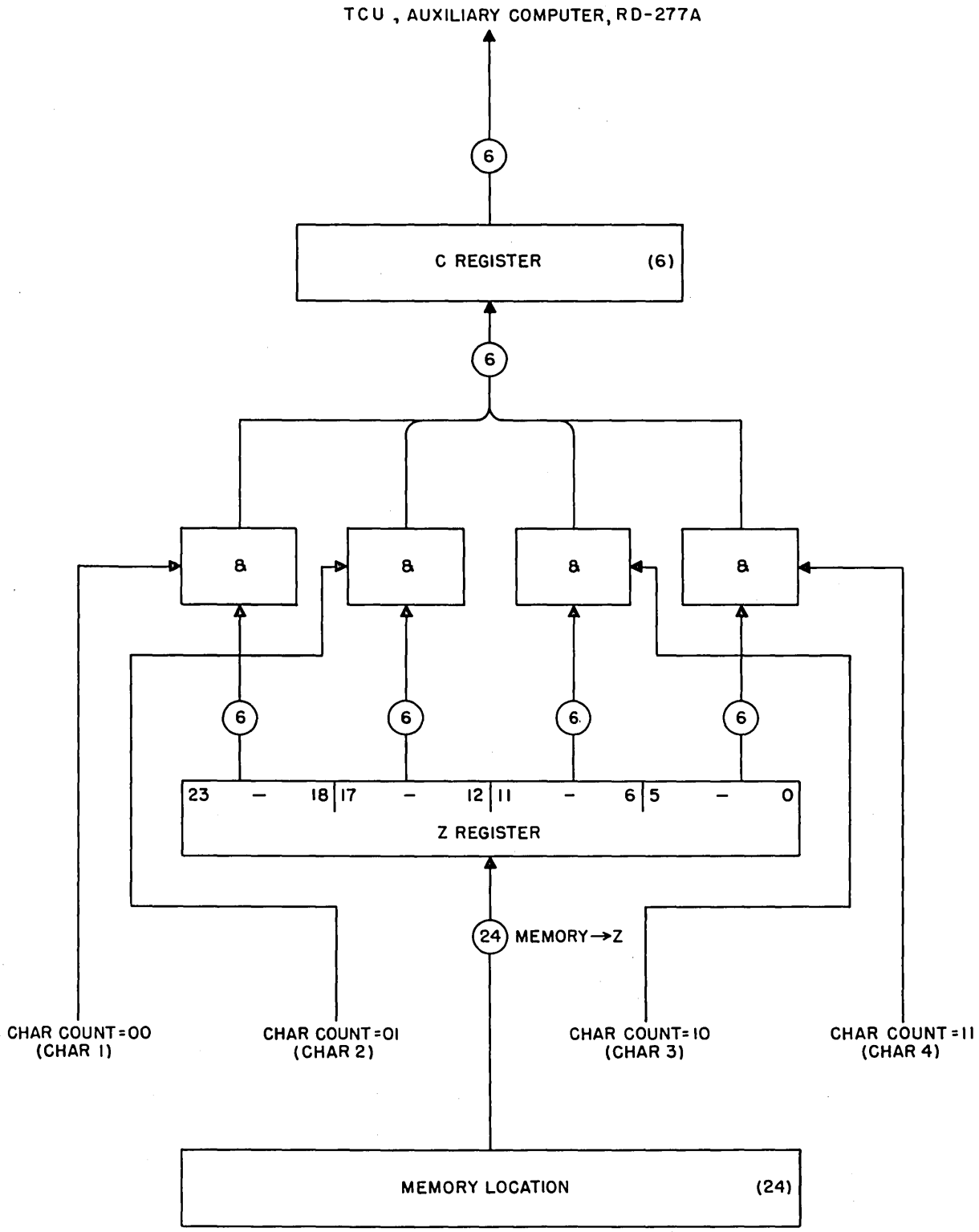


Figure 4-66. Output Data Path, TCU, RD-277A, and Auxiliary Computer (6-Bit Mode)

Figure 4-66, page 4-137, shows how 6-bit characters transfer from the memory location specified by the I/O control word to the TCU, auxiliary computer, and RD-277A when it is operating in the 6-bit mode. The first character transferred consists of bits 18 through 23. The last character transferred consists of bits 0 through 5.

(7) Acknowledge circuits. - The acknowledge circuits generate input and output acknowledge signals for the peripheral equipment. When the input/output section honors an input request, it sends an input acknowledge signal that indicates to the peripheral equipment that the computer has accepted the input character. When the input/output section honors an output request, it sends an output acknowledge signal indicating to the peripheral equipment that the computer has placed an output character on the output data lines. The acknowledge circuits consist of acknowledge flip-flops and acknowledge enable circuits.

(a) Acknowledge enable circuits (figure 8-86, page 8-187). - The acknowledge-enable circuits generate the signals that clear and set the acknowledge flip-flops and gate the acknowledge signals to the peripheral equipment. When the acknowledge signal is in response to a data request, an acknowledge flip-flop clears at time 1.2 (R/W-sequence) and sets at time 1.3 (R/W-sequence). The acknowledge signal does not go to the peripheral equipment until time 6.3 of the R/W-sequence. The acknowledge signal remains until time 6.3 of the next sequence (approximately 4 microseconds). However, the acknowledge flip-flop remains set until time 1.2 of the next R/W-sequence or R-sequence of a 07 (EXF) instruction. The acknowledge signal accompanies an external function character in an R-sequence. All flip-flops acknowledge clear at time 1.2.

(b) Acknowledge flip-flops (figures 8-85 and 8-86, pages 8-185 and 8-187). - There is one acknowledge flip-flop for each of the acknowledge signals generated by the input/output section. The conditions for generating acknowledge signals differ for the different peripheral equipment. The following paragraphs describe the conditions necessary to generate each acknowledge signal.

The TCU output acknowledge signal occurs for two different conditions. It occurs each time the input/output section honors a TCU output request. It also occurs when the computer executes the external function instruction with a peripheral unit code of 000012. A TCU output acknowledge signal accompanies each data and external function character sent to the TCU. The TCU input acknowledge signal occurs each time the input/output section honors a TCU input request.

The console acknowledge signal occurs when the input/output section honors a console request. If the request is for output, the acknowledge signal accompanies the character sent to the console. If the request is for input, only the acknowledge signal goes to the console.

The PTU input acknowledge signal occurs when the input/output section honors a PTU input request. The PTU output acknowledge signal occurs each time the input/output section honors a PTU output request. The PTU output acknowledge signal accompanies each data character sent to the RD-277A.

The auxiliary-computer input acknowledge signal occurs and is sent to the auxiliary computer for two different conditions. It occurs each time the input/output section honors an auxiliary-computer input request. It also occurs when the computer executes the 07 (EXF) instruction with a peripheral unit code of 00110_2. The auxiliary-computer output acknowledge signal occurs for two different conditions. It occurs each time the input/output section honors an auxiliary-computer output request. It also occurs when the computer executes the 07 (EXF) instruction with a peripheral unit code of 00100_2.

The PCU output acknowledge signal occurs for two different conditions. It occurs each time the input/output section honors a PCU output request. It also occurs when the computer executes the 07 (EXF) instruction with a peripheral unit code of 00011_2. The PCU output acknowledge signal accompanies each data character and external function character sent to PCU.

(8) Time base interrupt. - Two interrupt control words (figure 4-67, page 4-140) must be loaded into memory prior to executing the time base interrupt instruction. The control word loaded into memory location 42 contains the address of a subroutine (jump address) in bits 0 through 13 and a word count (tally) in bits 14 through 23. The value of the tally determines the length of the interrupt: all bits at zero result in 1 millisecond; all bits at one (1024_{10} decrements) result in 1 second. The control word at location 43 is loaded with the address of the interrupted instruction. At the completion of the jump instruction, address 43 must be referenced to return to the interrupt instruction.

The time base interrupt operation uses the RC1, $RC1_N$, and WC-sequences. The interrupt operation flow diagram is shown in figure 4-68, page 4-140. The RC1 and WC-sequences are the same as for the other I/O operations

23 - 14	13 - 0
TALLY	JUMP ADDRESS

A. CONTROL WORD AT MEMORY LOCATION 42

23 - 19	18 - 14	13 - 0
f =14(TRU)	BLANK	RETURN ADDRESS

B. CONTROL WORD AT MEMORY LOCATION 43

Figure 4-67. Time-Base-Interrupt Control Word Formats

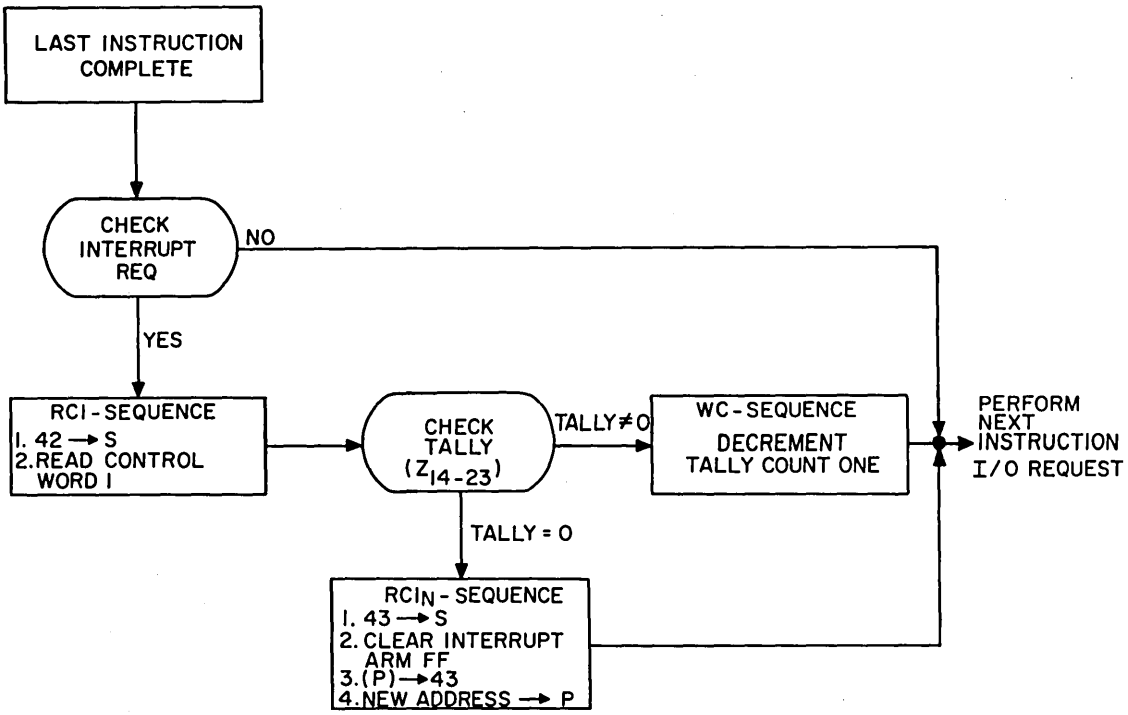


Figure 4-68. Interrupt Operation Flow Diagram

and are shown in tables 4-14 and 4-17, pages 4-115 and 4-122. The $RC1_N$-sequence, used only for time base interrupt, is shown in table 4-18.

TABLE 4-18. $RC1_N$-Sequence

Time	Action	Conditions and Notes
6.4	Clear S- and Z-registers	
1.1	$43 \longrightarrow S$	
1.2	Clear X-register and interrupt arm flip-flop	Disable future interrupt until enabled by programmer
1.3	$P \longrightarrow X$	
2.1	$X_{0-13} \longrightarrow Z$	Store next instruction word address of interrupted program in location 43. Upper half of 43 should contain TRU function code
2.2	Strobe upper and clear P	
2.3	$D_{0-13} \longrightarrow P$	Address of first instruction for new program
3.2	Clear D	
5.4	Clear $RC1_N$-sequence flip-flop	
6.1	Set I-sequence enable flip-flop	Or RC1-sequence if I/O request is present
	This sequence is used only during an interrupt operation when bits 14 through 23 in memory location 42 (interrupt control word 1) equal zero. The sequence clears the interrupt arm flip-flop, stores the present contents of the P-register into the 14 low-order bits of memory location 43, and loads a new address (from bits 0 through 13 of memory location 42) into the P-register.	

The time base interrupt logic (figures 8-69 and 8-88, pages 8-153 and 8-191), when armed, generates requests to the I/O system at a 1-KHz rate. The interrupt request-one-shot flip-flop sets when the interrupt arm flip-flop is set and the oscillator output is low. It remains set until:

1) The program executes a disarm code, which clears the interrupt arm flip-flop,

2) Word count equals zero during the $RC1_N$-sequence,

3) Approximately 1/2 millisecond later if the resync flip-flop is set, and at time 1.3 of the R/W-sequence or the WC or $RC1_N$ interrupt-sequences.

The resync flip-flop sets approximately 1/2-millisecond after the interrupt one-shot flip-flop is set if the scan flip-flop is set (time 3.4 of the scan cycle). Outputs from the resync flip-flop indicate to the I/O priority and other I/O circuits that an interrupt is underway and appropriate operations are to be followed. At time 4.2, the resync flip-flop clears. The request one-shot flip-flop remains clear until the interrupt arm flip-flop is set again by the program. The cycle time for the interrupt is thus approximately 1 millisecond.

(9) Miscellaneous input/output circuits. - The following input/output circuits perform special functions not common to all input/output operations.

(a) Buffer terminate (figure 8-87, page 8-189). - The buffer terminate circuit monitors the memory areas assigned to the peripheral equipment. When an input memory area has been filled or all the data in an output memory area has been transferred to the peripheral unit, the buffer-terminate circuit indicates a terminate condition. The buffer-terminate circuit also monitors the memory area specified by the RCA control words (shift instruction, RCA mode). When the contents of the specified memory area have been shifted, the buffer-terminate circuit sends a signal to the shift control logic to stop the shift operation.

The buffer-terminate flip-flop sets at time 4.4 of the RC2-sequence when the word-count portion of the second I/O control word or RCA control word equals zero and no interrupt is granted. The buffer-terminate flip-flop remains set until time 6.4 of the W-sequence. When set, the buffer-terminate flip-flop indicates the terminate condition.

(b) Console I/O translation (figure 8-77, page 8-169). - The console I/O translation logic consists of a priority network and a translator. The priority network operates when I/O priority (figure 8-71, page 8-157) grants priority to a console. The console priority logic then determines which console is serviced if more than one are requesting. Outputs from the console priority network enable the appropriate input data and address gates.

The console translator translates the 5-bit address that accompanies each console request. From this address, the translator determines whether the request is for input or output and which equipment in the console is requesting to send data to or receive data from the computer. The console translator also monitors the serial/parallel line from the consoles (figure 8-73, page 8-161) to determine the type of input data the console is sending. If it is serial data, the computer accepts the console input data one, two, or three bits at a time, depending upon the mode portion of the I/O control word. If it is parallel data the computer accepts the console input data six or eight bits at a time, depending upon the position of the console bit selector switch (figure 8-60, page 8-135).

(c) Console data terminate logic (figure 8-78, page 8-171). - The terminate logic generates control bits for the control section so that the control section can count the number of console-data-input transfers and update the I/O control words associated with console data input.

Before any console data input has been entered into a memory location, bit 21 of the I/O control word equals zero. This indicates that no console data input has been transferred into the memory location specified by the address portion of the I/O control word. When the first console data input occurs, the terminate logic generates a signal that sets bit 21 of I/O control word to one. For the first console data input transfer in each memory location the terminate logic sets bit 1 of the memory location where the console input data is being stored to one. As each console data input occurs, the contents of the memory location are shifted as shown in figure A-4, page A-9. The control section continuously monitors bit 7, 11, or 23 of the memory location where console data input is being stored. If the mode-designator portion of the I/O control word indicates that the computer is accepting one bit of console data input at a time, the control section monitors bit 23 of the memory location. When the control bit inserted in bit position 1 of the memory location reaches bit position 23, the control section knows that the 24th console data input is occurring. The I/O control word is then updated, and bit 21 of the I/O control word cleared to zero. If the mode designator position of the I/O control word indicates that

the computer is accepting two bits of console data input at a time, the control section monitors bit 11 of the memory location. When the control bit inserted in bit position 1 of the memory location reaches bit position 11, the control section knows that the 12th console data input transfer is occurring. The I/O control word is then updated, and bit 21 of the I/O control word cleared to zero. If the mode designator portion of the I/O control indicates that the computer is accepting three bits of console data input at a time, the control section monitors bit 7 of the memory location. When the control bit inserted in bit position 1 of the memory location reaches bit position 7, the control section knows that eighth console data input transfer is occurring. The I/O control word is then updated and bit 21 cleared to zero.

(d) RD-277A enable circuits (figure 8-88, page 8-191). - The RD-277A I/O enable circuits generate control signals that accompany PTU external function characters to the RD-277A. These signals are: external function, PTU lockout, and input active. Control signals and external function codes go to the RD-277A each time the computer program executes the external function instruction and this instruction references the RD-277A The RD-277A I/O enable circuits consist of four flip-flops: external function, lockout, output, and input. Figure 4-69, page 4-145, shows these flip-flops and associated circuits. During a 07 (EXF) instruction when the RD-277A is referenced, the external function code (bits 0 through 10 of the instruction) goes to the C-register and the RD-277A I/O enable circuits during the R-sequence of the instruction. Bits 0 through 7 of the Z-register are gated to the C-register at time 3.3 of the R-sequence. Bits 7 through 10 are gated to the RD-277A I/O enable flip-flops at time 5.1 of the R-sequence. The outputs of the C-register and three of the RD-277A I/O enable flip-flops go to the RD-277A.

The external function flip-flop sets at time 5.1 of the R-sequence of the 07 (EXF) instruction when the RD-277A is referenced and bit 7 of the instruction equals one. When the flip-flop sets, one output prevents input and output requests from the RD-277A from being honored while the 07 (EXF) instruction for the RD-277A is executed. The other output, combined with the acknowledge enable signal, generates the PTU external function signal for approximately 4 microseconds.

The lockout flip-flop sets at time 5.1 of the R-sequence of the 07 (EXF) instruction when the RD-277A is referenced and bit 8 of the instruction equals one. The flip-flop remains set until time 4.2 of the next sequence. While the flip-flop is set, the reader lockout signal is present.

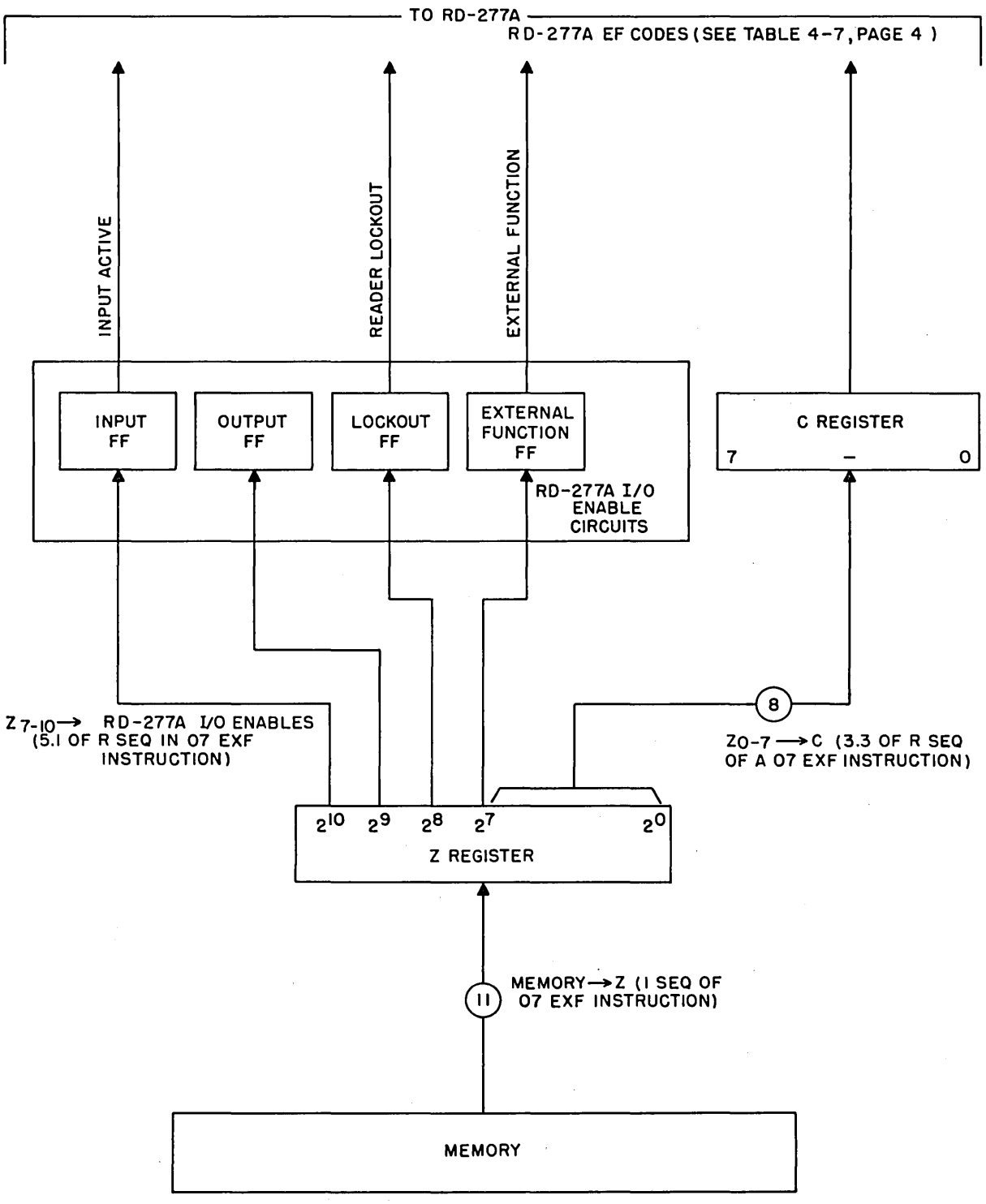


Figure 4-69. RD-277A I/O Enable Circuit and Associated Circuits

The output flip-flop sets at time 5.1 of the R-sequence of a 07 (EXF) instruction when the RD-277A is referenced and bit 9 of the instruction equals one. The flip-flop remains set until the RD-277A requests an output character and all characters in the memory area for paper tape output have been transferred. While the output flip-flop is set, the input/output section accepts output requests from the RD-277A.

The input flip-flop sets at time 5.1 of the R-sequence of a 07 (EXF) instruction when the RD-277A is referenced and bit 10 of the instruction equals one. The flip-flop remains set until the RD-277A sends an input request to the computer and the memory area for RD-277A input is full. While the input flip-flop is set, the input/output section accepts input characters from the RD-277A. Also, an input active signal is sent to the RD-277A. This signal indicates to the RD-277A that the computer memory area is not full and the computer will accept input characters.

c. Description of Operation.

(1) External function transfers. - The computer sends external function characters to the TCU, RD-277A, auxiliary computer, and PCU to instruct them to perform one of the functions listed in tables 4-7 through 4-9, pages 4-21 through 4-24. To send the character, the computer executes a 07 (EXF) instruction which contains a peripheral unit code and a function code. The peripheral unit code specifies which peripheral equipment will receive the function code. The function code specifies the operation to be performed by the peripheral equipment. In the case of the PCU, a function code could specify which punch is to be selected.

The 07 (EXF) instruction requires an I and R-sequence. The instruction is read from memory during the I-sequence. During the R-sequence the peripheral unit code enters the C-register. Near the end of the R-sequence, the appropriate acknowledge flip-flop sets, and an acknowledge signal and function code are sent to the peripheral equipment.

(2) Peripheral equipment data transfers. - The computer sends data to all of the peripheral equipment and accepts data from all peripheral equipment except the PCU.

(a) Output to TCU. - The TCU initiates the output data transfer operation after the computer instructs it to accept data. The TCU sends an output request signal to the computer. During the following scan cycle, the output request signal enters the input/output request logic and sets the

TCU-output-request flip-flop. When input/output priority honors the request, the output data transfer begins. An RC-sequence reads the I/O control word for TCU output at memory location 00056. During the R/W-sequence the contents of the memory location specified by the I/O control word are read. One character from this memory location enters the C-register. At the end of the R/W-sequence the TCU-output-acknowledge flip-flop sets. The character and an acknowledge signal go to the TCU. The TCU detects the acknowledge signal, accepts the character, and drops its output request. Four microseconds later it issues another request signal to the computer. This process continues until all data specified by the I/O control words in addresses 00056 and 00057 has been transferred. When all of the data has been transferred, the computer responds to succeeding output request signals by sending a buffer terminate character of 200_8 to the tape control unit. This terminate character is sent to the TCU until the TCU stops requesting data or until the I/O control words are reloaded.

(b) Output to RD-277A. - The RD-277A initiates the output data transfer operation after the computer instructs it to request data. The RD-277A sends an output request signal to the computer. During the following scan cycle, the output request signal enters the input/output request logic and sets the PTU-output-resync flip-flop. When input/output priority honors the request, the output data transfer begins. The RC-sequence reads the I/O control word from paper tape output at memory location 00052. During the R/W-sequence the contents of the memory location specified by the I/O control word are read. One character of this memory location enters the C-register and the character and an acknowledge signal go to the RD-277A. The RD-277A detects the acknowledge signal, accepts the character, drops the output request, and 4 microseconds later sends another output request signal to the computer. This sequence continues until all data specified by the I/O control words in addresses 00052 and 00053 has been transferred. When all of the data has been transferred, a buffer terminate occurs and the RD-277A acknowledge and output request logic are disabled. The computer does not accept any more RD-277A output request signals until after another 07 (EXF) instruction.

(c) Output to PCU. - The PCU controls a group of punches. The computer enables the punches by executing the 07 (EXF) instruction (one instruction enables one punch). The PCU generates a 6-bit address and a PCU request signal for the computer. The address specifies which punch will receive the data. During the following scan cycle, the request enters the input/output request logic and sets the PCU resync flip-flop. When input/output priority honors the request, the output data transfer

begins. The RC-sequence reads the I/O control word from memory. The address accompanying the request signal from the PCU and the request signal determine the address of the I/O control word (see table 1-3, page 1-15). During the R/W-sequence the contents of the memory location specified by the I/O control word are read. One 8-bit character from this memory location enters the C-register. The character and an acknowledge signal go to the PCU. The PCU detects the PCU acknowledge signal and accepts the character. The PCU then scans the punch addresses for other enabled punches and, when one occurs, it generates another address and another PCU request signal for the computer. This sequence continues until all punches are disabled. The computer disables a punch by responding to a PCU request signal with character 240_8. The PCU then stops requesting data for that punch. The computer must execute another 07 (EXF) instruction to enable the punch again. If all of the data specified by the I/O control words have been transferred to a punch and that punch continues to request data, the computer responds to the request with a buffer terminate (no print) character of $2XX_8$.

(d) Output to console. - The console initiates an output data transfer by sending a request signal and an address to the computer. The address specifies the address of the I/O control word associated with the output equipment in the console. See table 1-3, page 1-15, for console I/O control word addresses. During the following scan cycle, the request enters the input/output request logic and sets the appropriate console resync flip-flop. When input/output priority honors the request, the data transfer begins. The RC-sequence reads the appropriate I/O control word from memory. During the R/W-sequence the contents of the memory location specified by the I/O control word are read. One character of this memory location enters the C-register. The character and acknowledge signal go to the console. The console detects the acknowledge signal, accepts the character, drops its request and generates another request signal. Some console output request signals are generated throughout the console operation. If the console generates a request, and the I/O control words for that request indicate that all of the data has been transferred, the computer responds to the request (and succeeding requests) with a buffer terminate character of 200_8 until the console stops requesting or until the I/O control words are reloaded.

(e) Input from TCU. - The TCU initiates the input data transfer operation after the computer instructs it to send data. The TCU sends an input request signal and an input character to the computer. During the following scan cycle, the input request signal enters the input/output request logic and sets the TCU input-resync flip-flop. When input/output priority

honors the request, the input data transfer begins and the character enters the data input amplifiers. The RC-sequence reads the I/O control word for TCU input at memory location 00054. During the R/W-sequence the input character is stored in memory at the location specified by the I/O control word. At the end of the R/W-sequence the TCU-input-acknowledge flip-flop sets, and the acknowledge signal goes to the TCU. The TCU detects the acknowledge signal, removes the input request signal and input character, and generates another input request signal and input character. This sequence continues until the memory area specified by the I/O control words for TCU input is full. When the memory area is full, the computer responds to input request signals with an acknowledge signal and a buffer terminate character of 200_8 until the TCU stops requesting or until the I/O control words are reloaded.

(f) Input from RD-277A. - The RD-277A initiates the input data transfer operation after the computer instructs it to send data. The RD-277A sends an input request signal and an input character to the computer. During the following scan cycle, the input request signal enters the input/output request logic and sets the PTU-input-resync flip-flop. When input/output priority honors the request, the input character enters the data input amplifiers and the input data transfer begins. The RC-sequence reads the I/O control word for PTU input at memory location 00050. During the R/W-sequence, the input character is stored in memory at the location specified by the I/O control word. At the end of the R/W-sequence, the PTU-input-acknowledge flip-flops set, and the acknowledge signal goes to the RD-277A. The RD-277A detects the acknowledge signal, removes the input request signal and input character, and generates another input request signal and character. This sequence continues until the memory area specified by the I/O control words is full. When the memory area is full, the computer disables the last acknowledge signal and disables the PTU-input-resync flip-flop. This prevents the computer from honoring any more input request signals from the RD-277A until the I/O control words are reloaded.

(g) Input from console. - The console initiates an input data transfer by sending a request signal, an input character, and an address to the computer. The address specifies the address of the I/O control words associated with input equipment in the console. See table 1-3, page 1-15, for console I/O control word addresses. During the following scan cycle, the request signal enters the input/output request logic and sets the appropriate console flip-flop. When input/output priority honors the request, the input character enters the data input amplifiers and the input data transfer

begins. The RC-sequence reads the appropriate control word from memory. During the R/W-sequence the input character is stored in memory at the location specified by the I/O control word. At the end of the R/W-sequence, the appropriate console-acknowledge flip-flop sets, and the acknowledge signal goes to the console. The console detects the acknowledge signal; removes the input character and request signal; and generates another character, address, and request signal. This sequence continues as long as the console has data for the computer. If the memory area from a particular type of input data is full, the computer continuously responds to the request with a buffer terminate character of 200_8 and an acknowledge signal.

(3) Intercomputer operation (figures 8-80 and 8-89, pages 8-175 and 8-193). - The computer can send data to and receive data from another CP-818A/U computer, referred to as the auxiliary computer. The computers have equal priority, thus, for this intercomputer description, the two computers are called computer A and computer B. Either computer can establish communication with the other.

Each computer has two intercomputer cable connectors, labeled J5 and J10, mounted on the top of the cabinet. Only one intercomputer cable connects the two computers. If the cable connects to J5 of computer A, it must connect to J10 of computer B. Figure 4-70, page 4-151, shows how the intercomputer cable must be connected.

CAUTION. - If the cable is not connected as shown in figure 4-70, page 4-151, printed circuit cards are damaged.

Figure 4-71, page 4-151, shows the data and control lines between the two computers. With reference to figure 4-71, page 4-151, note the following.

1) The output acknowledge signal that accompanies an output data character or external function character enters the input request circuit of the other computer.

2) The input acknowledge signal that informs the auxiliary computer that the computer has accepted an input character enters the output request circuit of the other computer.

3) Bits 6 and 7 of the C-register are ones when a computer sends an external function to the other computer. This

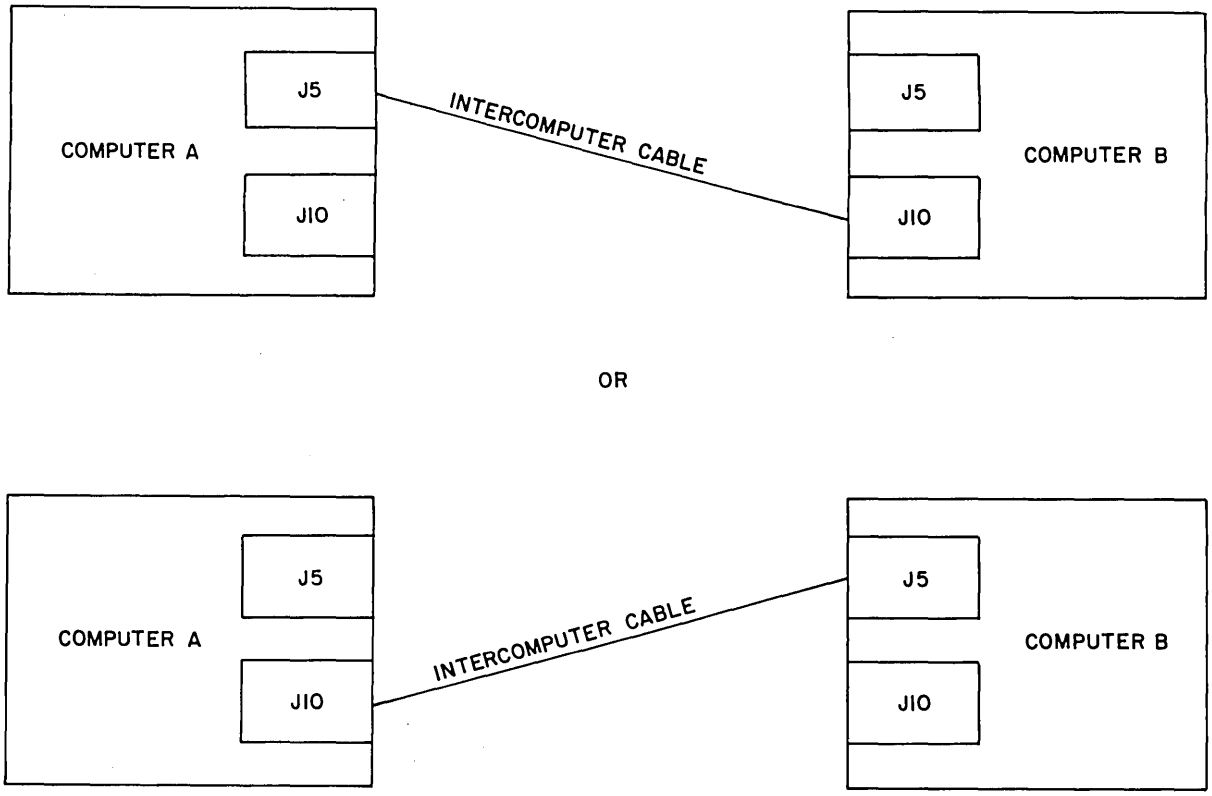


Figure 4-70. Intercomputer Cabling

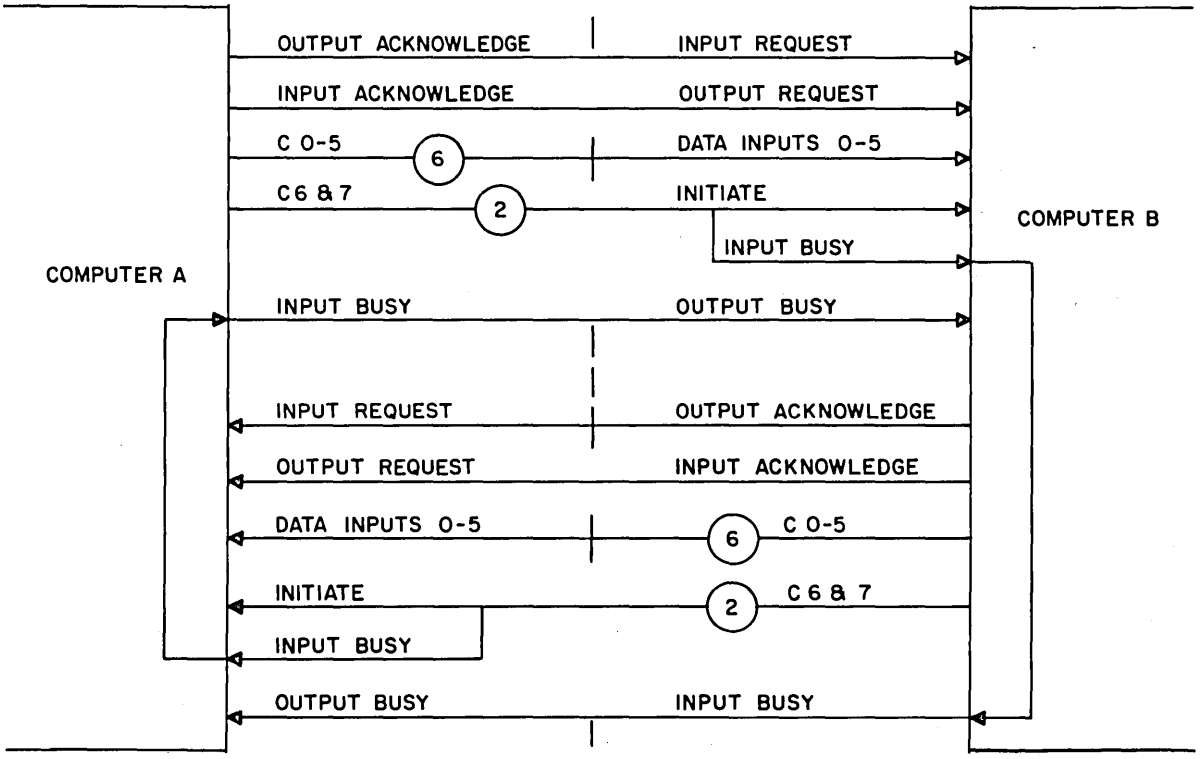


Figure 4-71. Intercomputer Interface

sets the initiate and input-busy status flip-flops in the other computer.

4) When a computer sends an external function to the other computer and the input-busy status flip-flop sets, an output from the input-busy flip-flop activates the output-busy status line in the computer that sent the external function.

The following sequence of events occurs during intercomputer communication. Assume that computer A initiates the data transfer operation. Since the computers are identical, the same sequence of events occurs, when computer B initiates the data transfer operation.

1) Computer A executes a 07 (EXF) instruction that specifies auxiliary-computer output (computer B) and contains an external function code of 300_8. The instruction also generates an external function (output acknowledge) signal. This external function signal and the external function code are sent to computer B.

2) Bits 6 and 7 of the external function code from computer A set the initiate and input-busy status flip-flops in computer B. An output from the input-busy status flip-flop activates the output-busy status line to computer A.

Note: - When bits 6 and/or 7 of the character transferred to computer B are set, computer B recognizes the character as an external function, and the character does not enter the intercomputer register (figure 8-89, page 8-193) of computer B. Computer B does not acknowledge the external function character.

3) Computer B has its initiate and input-busy status flip-flops set, and computer A has its output-busy status line active. The intercomputer operation remains in this state until the computer B program senses, via a 02 (TRF) instruction that computer A wants to send data.

4) In computer B the 02 (TRF) instruction senses the initiate and input-busy status flip-flops. When computer B executes the 02 (TRF) instruction and senses the initiate status flip-flop is set, computer B knows that computer A

wants to send data. Computer B responds by executing the 07 (EXF) instruction. This instruction specifies auxiliary-computer input (computer A) and contains a function code of 100_8.

5) When computer B executes external function 100_8, this instruction clears the initiate status flip-flop in computer B and generates an external function (input acknowledge) signal for computer A. With the initiate status flip-flop cleared and the input-busy status flip-flop set, computer B's program knows that intercomputer communication has been established with computer A.

6) Computer A receives the external function (input acknowledge) signal from computer B as an auxiliary-computer output request signal. Computer A recognizes bits 6 and/or 7, when set, as an external function code from computer B and does not enable the input gates on its intercomputer register and does not acknowledge the external function from computer B.

7) Since the output-busy status line in computer A is active, computer A accepts the input acknowledge signal from computer B as an auxiliary-computer output request signal.

8) When I/O priority in computer A honors the auxiliary-computer output request signal, computer A sends 6-bit character and an output acknowledge signal to computer B.

9) Computer B gates the 6-bit data character from computer A into the intercomputer register.

10) The character is then stored in memory and computer B returns an input acknowledge signal to computer A requesting the next character. The input acknowledge signal is interpreted by computer A as an auxiliary-computer output request signal.

11) Events 7 through 10 repeat until one of two conditions occurs. First, if computer A transfers all of its specified data to computer B, events 12, 13, and 14 occur. Secondly,

if computer B fills its memory area assigned to auxiliary computer input, events 15 and 16 occur.

12) Computer A generates a buffer terminate code of 200_8 and sends this code and an output acknowledge signal to computer B.

13) Computer B does not accept the terminate code into the intercomputer register, but the terminate code clears the input-busy status flip-flop. The program in computer B senses, via a 02 (TRF) instruction, the input-busy status flip-flop and the word count of the I/O control word from auxiliary computer input and determines that computer A terminated the intercomputer operation.

14) When the input-busy status flip-flop in computer B clears, the output-busy status line in computer A is inactive. The program in computer A can sense the output-busy status line and the word count of the I/O control word from auxiliary computer output and determine that computer A terminated the intercomputer operation.

15) The buffer-terminate flip-flop in computer B sets and the input-busy status flip-flop clears. This clears the output-busy status line in computer A.

16) The computer A program can sense its output-busy status line and the word-count portion of the I/O control word from auxiliary computer output and determine that computer B terminated the intercomputer operation. Conversely, the computer B program can sense the input-busy status flip-flop and the word-count portion of the I/O control word for auxiliary computer input and determine that computer B terminated the intercomputer operation.

4-19. MEMORY SECTION (see figure A-7, page A-15).

a. Main Memory. - The main memory is a random-access, bit-oriented, destructive-readout, magnetic core memory. All memory circuits are contained in the two lower chassis, A3A2(6) and A4A2(8) of the computer. Except for the bootstrap modules, the chassis are identical and

interchangeable. All memory logic schematics (figures 8-92 through 8-99, pages 8-199 through 8-213) represent both chassis. Chassis A3A2(6) (lower left) contains the circuits for bits 0 through 11 and the lower parity bit. Chassis A4A2(8) (lower right) contains the circuits for bits 12 through 23 and the upper parity bit. Each chassis contains four identical plug-in core stacks (A20-A23) that contain 4096 13-bit storage locations.

The core stacks are sealed, non-repairable packages and must be replaced if a malfunction is traced to a stack. Table 4-19 lists the address range and bits associated with each stack. The random-access feature allows words to be read from memory in any order. Thus, the addresses placed in the S-register do not have to be sequential. The bit-oriented feature causes the word to be read from memory in a parallel mode. The destructive-readout feature clears the memory location to zero when its contents are read out. Therefore, the word must be written back into memory (restored) if it is to be retained.

(1) Magnetic core characteristics. - A magnetic core is a bi-stable device capable of storing a one or a zero depending on the polarity of its residual magnetization. The cores used in main memory are made of ferrite material. The characteristics of these cores are such that a current of approximately 500 milliamperes for a period of 1.2 micro-seconds is required to switch them from one stable state to the other. The coincident current method is employed to address the cores. Four wires pass through each core, as shown in figure 4-72, page 4-156: an X-axis drive wire, a Y-axis drive wire, an inhibit wire parallel to the Y-drive wire, and a sense wire.

TABLE 4-19. Memory Stack Select Codes

S	Bits		A3A2(6) Stack Bits 0-11	A4A2(8) Stack Bits 12-23	Address Range
	13	12			
0XXXX	0	0	A20	A20	00000-07777
1XXXX	0	1	A21	A21	10000-17777
2XXXX	1	0	A22	A22	20000-27777
3XXXX	1	1	A23	A23	30000-37777

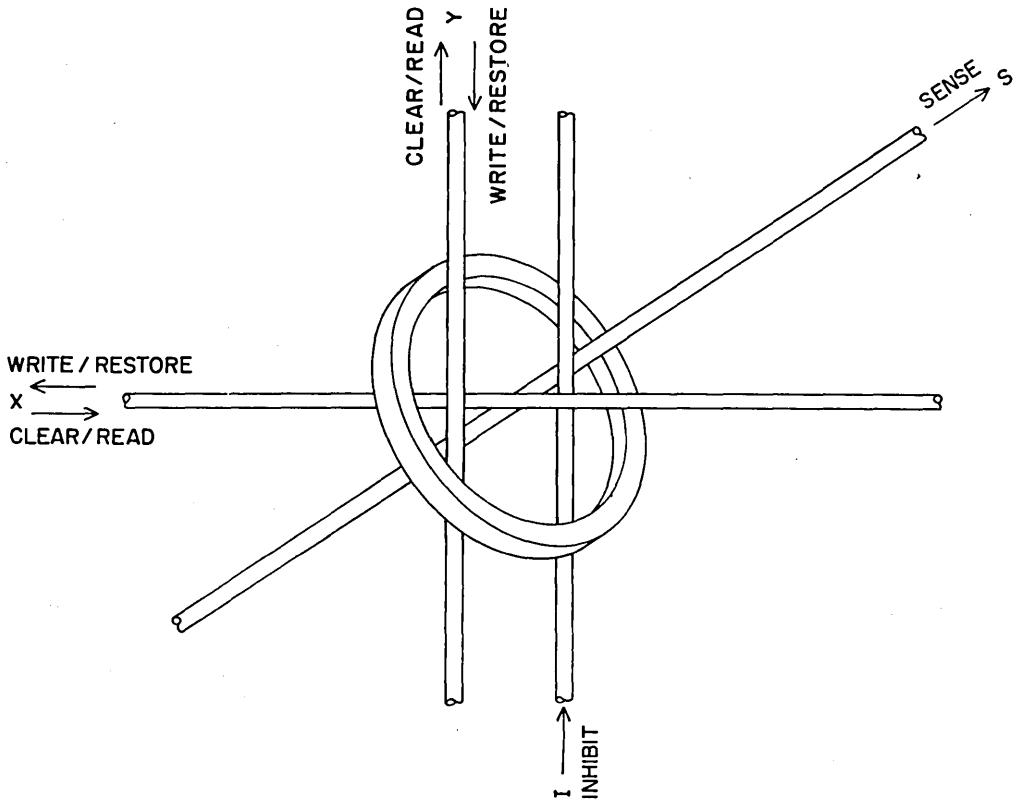


Figure 4-72. Typical Magnetic Core

The magnetization characteristics of ferrite cores are shown in figures 4-73 through 4-76, pages 4-157 through 4-158. Table 4-20, page 4-159, summarizes core operations. These figures are diagrams of a hysteresis loop, plotting magnetic flux as a function of the magnetizing field induced by the currents in the X and Y-drive wires. Ferrite cores tend to resist the effect of a magnetizing force; and, if this force is not sufficient to cause the polarity of their magnetization to reverse, they tend to return to their original state when the magnetizing force is removed. If the magnetizing force is sufficient to switch them, they change rapidly to the opposite polarity of magnetization.

The hysteresis loop shown in figure 4-73, page 4-157, assumes that the core is originally in the one state of magnetization. If the magnetizing force on the X and Y-wires is great enough, it will drive the core to the zero state, thus causing a change of flux within the core. A change of flux induces a voltage in the wires passing through the core.

The induce voltage on the sense wire is sampled to see if the core was in the one state. If it was, an output of approximately 50 millivolts should be induced in the sense line as the core switches. If, on the other hand, the core was originally in the zero state, as shown in figure 4-74, page 4-157,

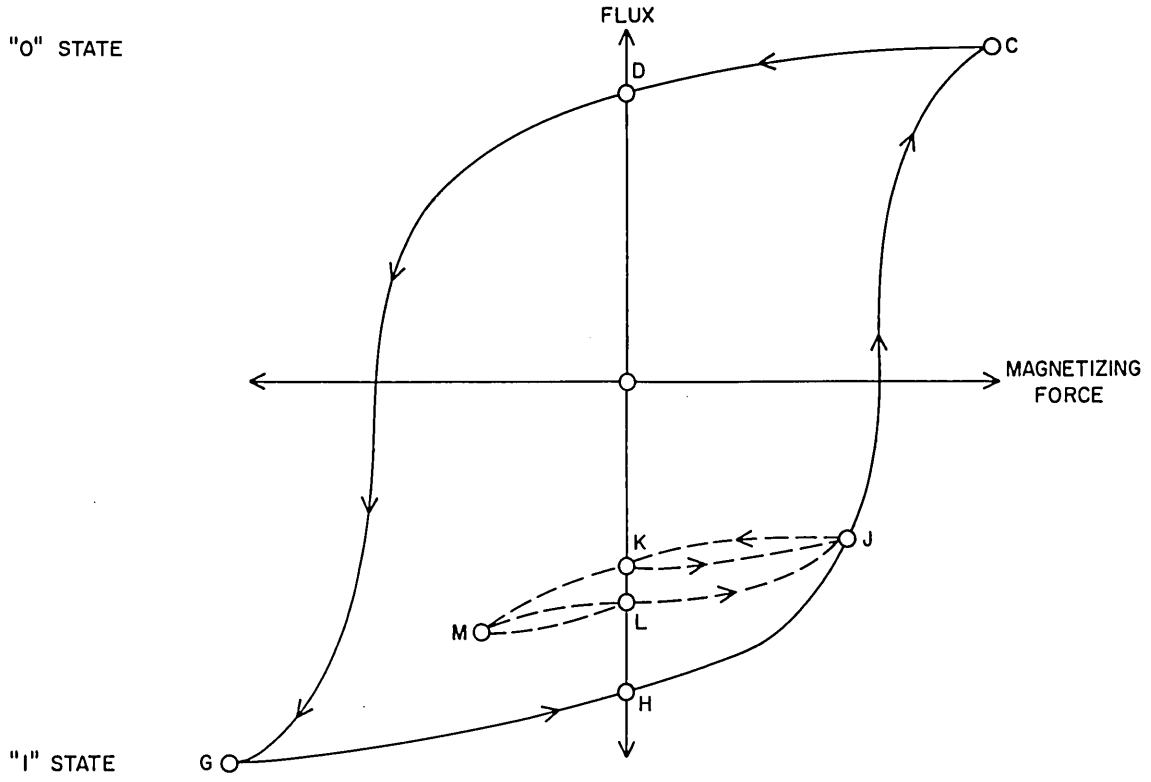


Figure 4-73. Reading and Restoring a Core in the One State

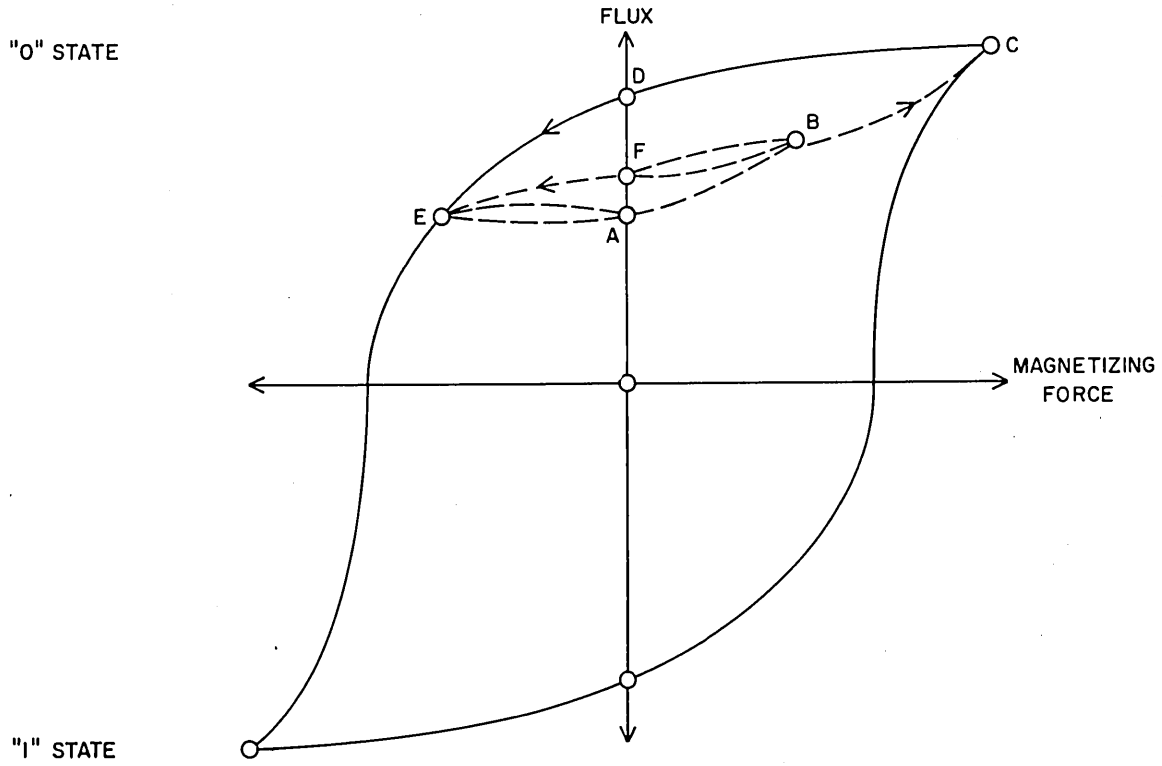


Figure 4-74. Reading and Restoring a Core in the Zero State

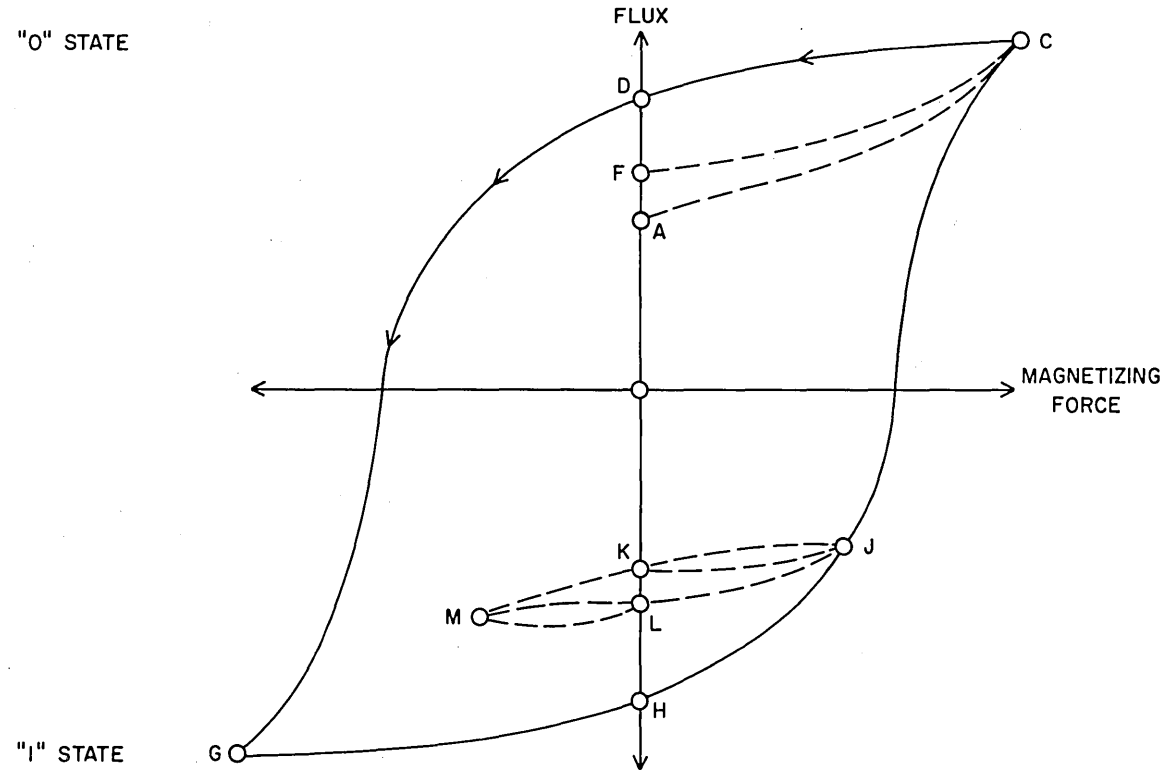


Figure 4-75. Writing a One into a Core that was in the Zero State

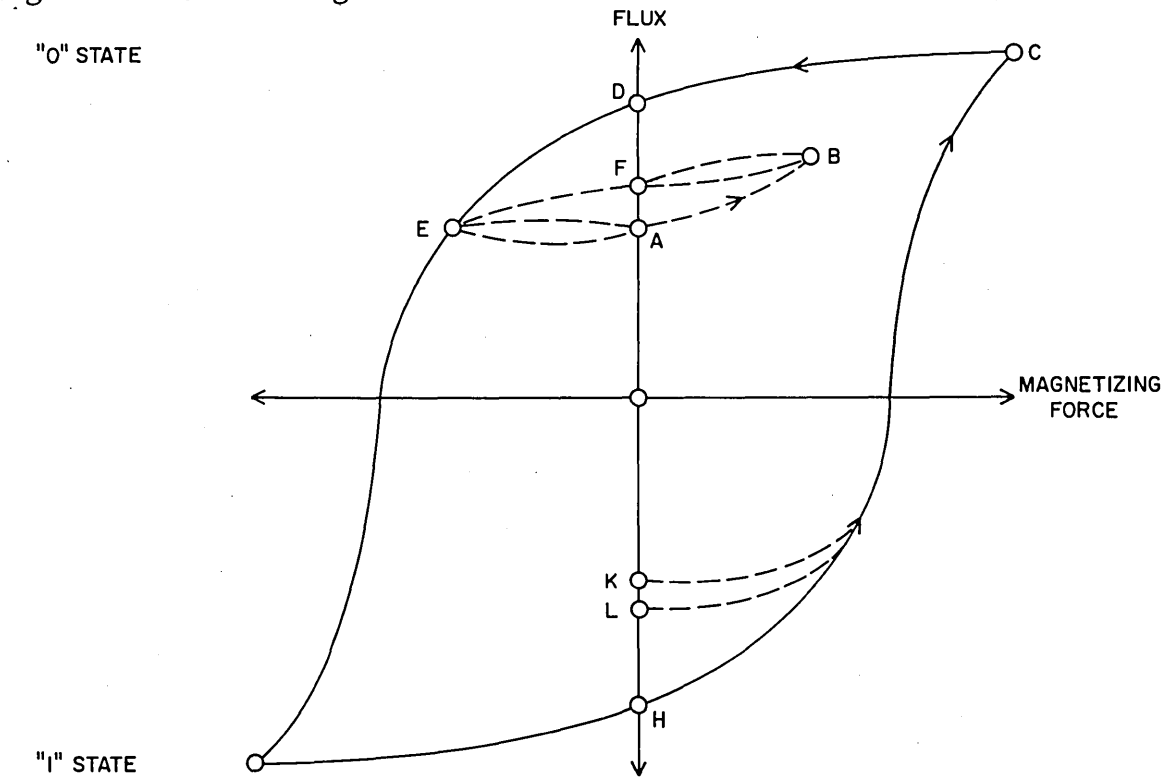


Figure 4-76. Writing a Zero into a Core that was in the One State

TABLE 4-20. Core Operation

Operation	Core State		Figure	Description
	Initial	Final		
Read-Restore Cycle				
Read	One	Zero	4-73, page 4-157	Clear/read pulses on X and Y-wires drive core state from H, L, or K to C; and a one output (about 50 millivolts) is produced on sense wire. When pulses terminate, core settles back to D.
	Zero	Zero	4-74, page 4-157	Clear/read pulses on X and Y-wires drive core state from A or F to C. No appreciable change in flux; no output observed or sense wire. When pulses terminate, core settles back to D.
Restore	Zero	One	4-73, page 4-157	Write/restore pulses on X and Y-wires drive core state from D to G. No inhibit pulse is applied. When pulses terminate, core settles back to H. Succeeding half-currents (on X, Y, or inhibit wires) shift core state from H to I to K and then around minor hysteresis loops from K to M to L, L to J to K, K to J to K, or L to M to L.
	Zero	Zero	4-74, page 4-157	Inhibit pulse on inhibit wire cancels effect of restore pulse on Y-wire; thus, half-amplitude pulse on X-wire shifts core state from D to E to A. Succeeding half-currents (on X, Y, or inhibit wires) shift core around minor loops from A to B to F, F to E to A, F to B to F, or A to E to A.

TABLE 4-20. Core Operation (continued)

Operation	Core State		Figure	Description
	Initial	Final		
Clear-Write Cycle				
Clear	Zero	Zero	4-75, page 4-158	Clear/read pulses on X and Y-wires drive core state from A or F to C. Output induced on sense wire is negligible; sensing circuitry is not activated. When pulses terminate, core settles back to D.
	One	Zero	4-76, page 4-158	Clear/read pulses on X and Y-wires drive core state from K, L, or H to C. Induced output on sense wire is ignored since core state prior to write operation is not important. When pulses terminate, core settles back to D.
Write	Zero	One	4-75, page 4-158	Write/restore pulses on X and Y-wires drive core state from D to G. No inhibit pulse is generated. When pulses terminate, core settles back to H. Succeeding half-currents (on X, Y, or inhibit wires) drive core from H to J to K, then around minor loops from K to M to L, L to J to K, K to J to K, or L to M to L.
	Zero	Zero	4-76, page 4-158	Inhibit pulse on inhibit wire cancels effect of write/restore pulse on Y-wire; thus, half-amplitude pulse on X-wire shifts core state from D to E. When pulses terminate, core settles back to A. Succeeding half-currents (on X, Y, or inhibit wires) shift core around minor loops from A to B to F, F to E to A, F to B to F, or A to E to A.

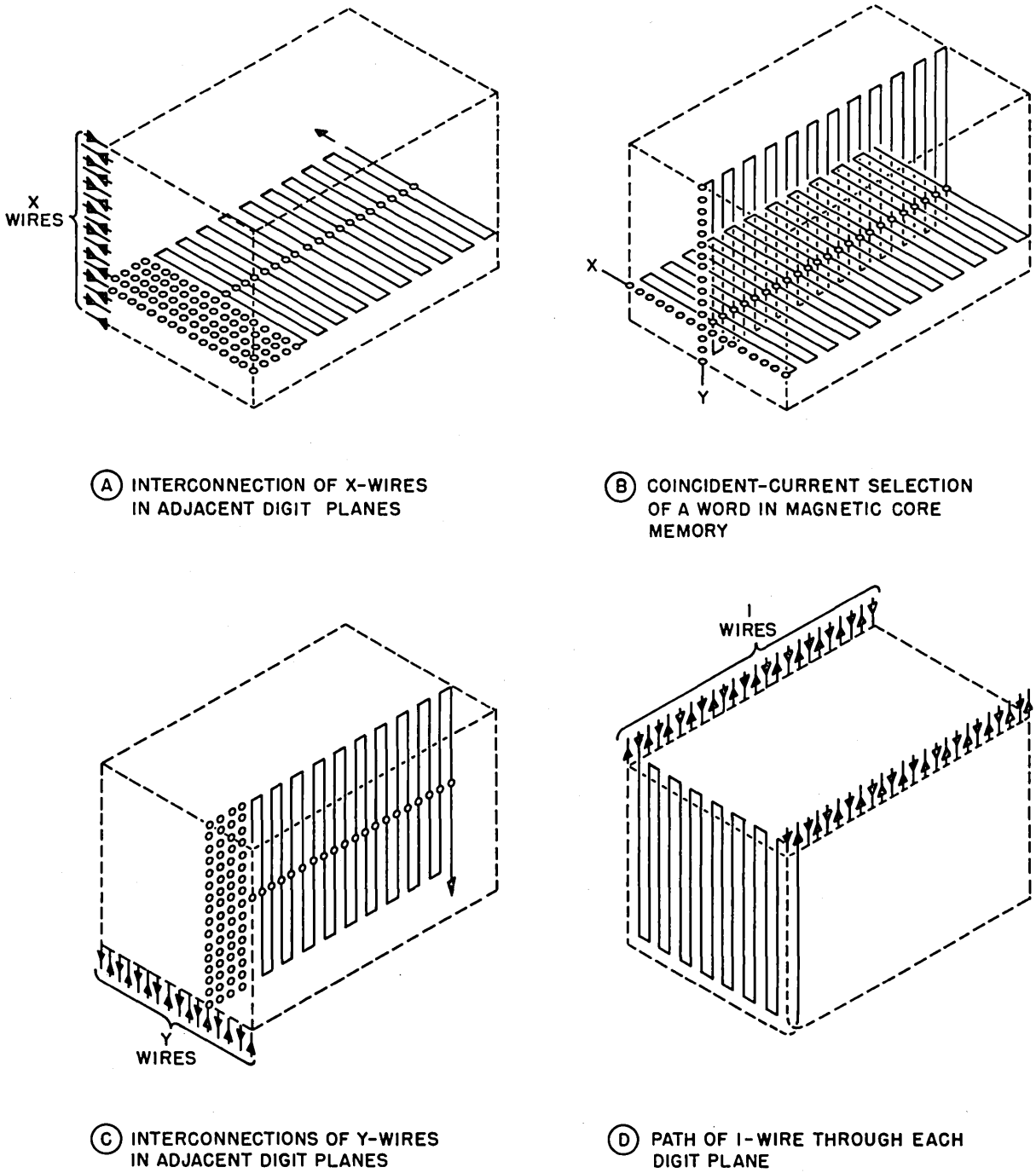
the magnetizing force produces only a small change in the state of the core and no appreciable flux change occurs. Therefore, no output is observed on the sense wire. Because the state of the core is determined by clearing it (switching it to the zero state), the current pulse producing this action is called the clear/read pulse.

The core will always be in the zero state after it has been read (destructive readout). To restore the core to a one condition, a write current opposite in polarity to the clear/read pulse is applied on the X and Y-wires. If a zero is to be stored, another current opposite in polarity to the write pulse on the Y-wire is simultaneously applied to the inhibit wire. This pulse reduces the effect of the X and Y-pulses sufficiently to prevent the core from being driven to the one state, and it remains in the zero state. The pulses associated with the write function are called write/restore pulses and are equal in amplitude, but opposite in polarity from the clear/read pulses.

When reading from cores, the process is called a read-restore cycle. The clear/read pulses switch all cores to the zero state, and the output from the sense lines is stored in a flip-flop register. The write/restore pulses then, controlled by the inhibit pulses, write the information back into the cores by switching the required cores back to the one state. When writing into cores, the process is called a clear-write cycle. The clear/read pulses switch the cores to the zero state, but the output from the sense lines is ignored. The write/restore pulses then, controlled by the inhibit pulses, write the information from a flip-flop register into the cores. See figures 4-75 and 4-76, page 4-158, for hysteresis loops involved in writing.

(2) Core memory addressing. - A coincident-current core storage system stores information in parallel form, using one magnetic core for each binary digit. The cores which store the corresponding bit of all words are contained on a single digit plane. Each digit plane of the memory contains 4096 magnetic cores and their control wires are arranged in a 64 x 64 array. The cores are held in position by the wires, which are soldered to a square printed-circuit frame. The complete core stack assembly consists of 13 such planes.

Each word in the memory is identified by an address consisting of the X and Y-coordinates corresponding to its position. The X and Y-wires thread through the cores of the memory assembly in a three-dimensional pattern similar to that illustrated in figure 4-77, page 4-162. The cores in each horizontal plane throughout the entire core assembly are connected in series



(A) INTERCONNECTION OF X-WIRES IN ADJACENT DIGIT PLANES

(B) COINCIDENT-CURRENT SELECTION OF A WORD IN MAGNETIC CORE MEMORY

(C) INTERCONNECTIONS OF Y-WIRES IN ADJACENT DIGIT PLANES

(D) PATH OF I-WIRE THROUGH EACH DIGIT PLANE

Figure 4-77. Core Addressing

by the X-wire; the cores in each vertical plane are connected in series by the Y-wire. The coincidence of currents at each intersection of one X-wire and one Y-wire provides the means for manipulating all cores identified with one word (see figure 4-77, page 4-162). Only those cores at the intersections of a selected pair of X and Y-wires are affected by coincident currents. The other cores along these wires are not affected, since the pulse on a single wire is not sufficient to switch the cores.

The inhibit wires provide the means for writing any desired combination of binary digits into any word address. Since each digit plane stores one digit of the word, a separate inhibit wire must be provided for each plane. The presence or absence of the inhibit current determines whether a zero or a one will be stored in that plane by the coincident X and Y-write pulses. Each inhibit wire threads through all the cores of a plane in series paralleling in the Y-wires, as shown in figure 4-77, page 4-162. The current flow in the inhibit wire is opposite in direction to the write/restore current in the Y-wire.

The sense wires provide the means for reading the words stored in memory. The digits of the word are read in parallel fashion. A separate sense wire is provided for each digit plane, and it follows a diagonal path with respect to the X and Y-wires, connecting all the cores of that plane in series. During a reading operation, the presence or absence of a pulse on the sense wire is an indication of the information stored in that plane at the address specified by the X and Y-coordinates. The path of the S-wire through the core matrix is chosen so the output voltages induced in the sense wire from unselected cores cancel one another, since the sum of these voltages would otherwise approach the amplitude of the desired signal. The sense wire passes back and forth over each X and Y-wire an even number of times so the transients produced in the wire by inductive coupling to the X and Y-wires tend to cancel each other.

b. Main Memory Control. - The main memory control consists of the cycle control circuits and the memory protect circuits.

(1) Cycle control circuits (figure 8-91, page 8-197). - The cycle control circuits generate the read, write, address, and inhibit enables. Main timing pulses set and clear the read, write, and inhibit flip-flops to generate the read, write, and inhibit enables. The read and write flip-flops also generate the address enable which is extended by the two timing pulses (01T31 and 03T53) to 14A00. Figure 4-78, page 4-164, shows the memory cycle timing. The read and the address enables activate the read current diverters causing a word to be read out and clearing the memory location

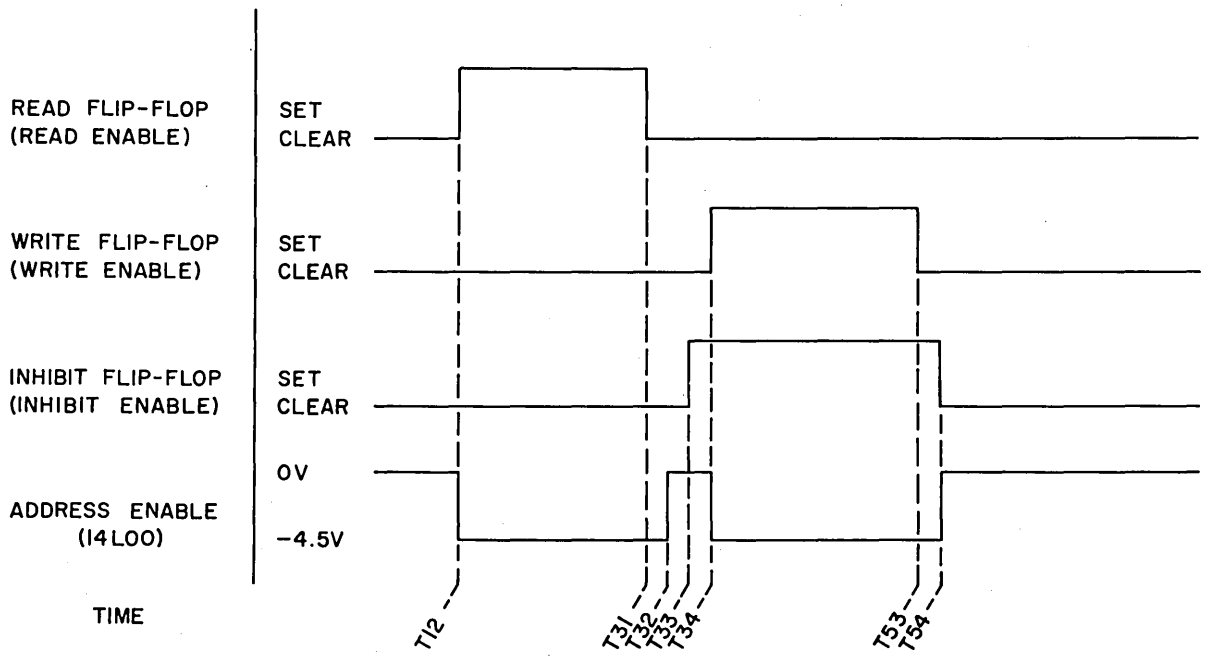


Figure 4-78. Memory Cycle Timing

to all zeros. The read flip-flop, when set, also initiates the read strobe timing circuits that gate the memory word into the Z-register (figure 8-54, page 8-123). The word is gated into Z approximately 1 microsecond after the memory cycle starts. At the completion of the read cycle, the write and address enables activate the write current diverters (19Y00 and 19Y02) and the inhibit enable, via selector circuit, activates the inhibit current diverters. The write currents attempt to write a word of all ones into the memory. The write current is cancelled by the inhibit current in cores that are to contain a zero. Thus the word read from memory is restored during the write cycle. The complete memory cycle of read and restore requires 4 microseconds.

(2) Memory protect circuits (figure 8-91, C2, page 8-197). - The memory protect circuits consist of a -4.5v sensor and a +15v sensor. These sensors act as switches to open the +V regulator supply if the 115 vac, 400-Hz input voltage drops below approximately 100 vac. The sensors enable OR 90J03 forcing the computer into the PHASE STEP mode at the end of the present memory cycle. The computer then master clears.

c. Address Translation. - The address in the S-register goes directly into the stack selection circuits and the X and Y-transformer and diode translator circuits of both memory chassis.

(1) Stack selector (figure 8-92, page 8-199). - The stack selector circuits are enabled by the address enable and translate the contents of bits 12 and 13 of the S-register to select one of the four core stacks in each chassis. Table 4-19, page 4-155, shows the stack selected in each chassis for the combinations of bits 12 and 13 and the address range contained in the stacks. The stack-select outputs enable the inhibit, read, and write switches on the selected core stack.

(2) X and Y-translator circuits. - The X and Y-transformer (16YXX terms) and diode (17YXX terms) translator circuits select one X and one Y-drive line in the selected core stack. S-register bits 6 through 8, for the X-line (figure 8-93, A3, page 8-201) and bits 0 through 2, for the Y-line (figure 8-95, A3, page 8-205), are decoded via the transformer translator circuits to select one of eight groups of eight lines (figures 8-94 and 8-96, pages 8-203 and 8-207). S-register bits 9 through 11, for the X-line (figure 8-93, C3, page 8-201) and bits 3 through 5, for the Y-line (figure 8-95, C3, page 8-205) are decoded, via the diode translator circuits, to select one of eight lines in each of the selected groups (figures 8-94 and 8-96, pages 8-203 and 8-207).

d. Memory Drive Circuits. - There are two types of drive circuits in the main memory, the read/write drive circuits, and inhibit drive circuits.

(1) Read/write drive circuits. - The read/write drive circuits consist of the R/W-current diverters and switches. These circuits control the direction of current flow in the memory drive lines. When the read flip-flop sets, it enables the X and Y-read current diverters (19Y03 and 19Y01) which enable the read switches in the stack selection circuits. The combination of the read diverters and two switches being enabled induces a voltage across the X and Y-transformer assemblies (figures 8-94 and 8-96, pages 8-203 and 8-207) on the core stacks to cause current flow in the selected memory drive line. The write circuits operate in the same manner as the read circuits except they are enabled by the write flip-flop; the voltage induced on the X and Y-transformer assemblies is of the opposite polarity, and the drive-line current flow is in the opposite direction.

(2) Inhibit drive circuits (figures 8-97, and 8-98, pages 8-209 and 8-211). - The inhibit drive circuits consist of the inhibit current diverters, switches, and transformer assemblies. They generate current flow in one inhibit line in each core plane of the selected stack. The inhibit current counteracts the effect of the write current when a core is to remain a zero. The inhibit switches of a selected stack are enabled by the stack-select circuits. The inhibit current diverters are enabled by the selector circuits when a bit is to remain a zero and the inhibit flip-flop sets. When a switch and diverter are enabled, the inhibit current flows from the diverter to the inhibit transformer assembly, through the transformer primary, and on to the switch. Current flow through the transformer primary induces a current on the inhibit line of a core plane and prevents all cores on the plane from switching.

e. Sense Amplifiers (figure 8-99, page 8-213). - A sense line from each of the 13 core planes of all four stacks in each chassis connects to sense amplifiers. The outputs of the amplifiers of corresponding bits in all four stacks connect to an OR circuit. The OR circuit output, a logic low when a logic one is read from the core plane, connects to the corresponding bit in the Z-register and is gated into the register by the read strobe from memory control. Operating the Marginal Check HIGH/NORMAL/LOW switch changes the sense amplifier bias by connecting pin 7 to the +15v supply (for low) or to the -15v supply (for high). In the HIGH position less of the signal is sensed and the amplifier may fail to sense a switching core. In the LOW position more of the signal is sensed and the amplifier may sense background noise as a logic one. Either condition indicates the drive currents are out of adjustment or are not functioning properly.

f. Bootstrap Memory (figure 8-100, page 8-215).

(1) Assembly. - The bootstrap memory is a permanent, prewired memory. It consists of two assemblies, one in each memory chassis. Each assembly contains four printed circuits bolted together and has a capacity of 32 words of 18 bits each. Only 16 words of 13 bits each (12 data bits plus a parity bit) are used. However, the 16 unused words are wired with the same information as the 16 that are used. To use the duplicate information move the wire on pin J2D6 to J2D8 and the wire on pin J2D5 to J2D7. The chassis-bit-position assignment is the same as used in main memory, bits 0 through 11 and lower parity bit in chassis A3A2(6) and bits 12 through 23 and upper parity in chassis A4A2(8). Figure A-8, page A-17, shows a schematic of the assembly. Card locations 2D, 3D, and 5D shown in the figure indicate the position of the assemblies in each chassis. The memory elements are 18 toroid coils mounted over

holes in the cards, with a hole next to each coil and a word line for each word. The coil and associated hole represent one bit of all words. If a bit is a one, the word line threads through the coil; if the bit is a zero, the word line threads through the hole. For the five bits shown wired as zeros in figure A-8, page A-17, all 32 word lines are threaded through the first five holes.

(2) Control. - The prewired bootstrap memory contains two 8-word automatic-program-loading routines. One routine loads from paper tape and the other from magnetic tape. The 16 words are assigned addresses 00060_8 to 00077_8. Figure 4-79, page 4-168, shows a block diagram of the bootstrap memory and figure 4-80, page 4-168, the functional operation of the bootstrap memory. When the S-register contains an address in the bootstrap range, a word group driver, a word line driver, the bootstrap enable, and bootstrap-to-Z-gate are enabled. S-register bits 4-13 generate the bootstrap enable to disable main memory control and the bootstrap-to-Z-gate to enable the input gates at the Z-register. Bit 3 of the S-register enables one of the two group drivers and bits 0 through 2 are translated to enable one of eight line drivers. With a group and line driver enabled, current flows in a specific word line, and the word is read out and gated into the Z-register. Once the word is in the Z-register, it is treated as if it came from main memory.

4-20. POWER SECTION (figure 8-101 through 8-103, pages 8-217 through 8-221). - The power section controls the ac power and provides dc voltage.

a. Control and AC Distribution. - The power control circuits are in the power supply (PS1) and on the hood control panel. Figure A-9, page A-19, shows the simplified power control circuits. Placing the POWER ON/OFF switch to ON initiates the following power-on sequence.

1) POWER ON/OFF switch contacts 1-2 close to energize power sequencing relay PS1K1 (ØA and ØB).

2) Relay PS1K1 contacts close to energize the +15v indicator supply, the memory blowers, the cabinet blowers, and heater voltage for relays A2K1 and A2K2 (ØA and ØB).

3) Approximately 30 seconds after PS1K1 energizes, if +15v indicator voltage is up, thermal time delay relay A2K2 contact closes, allowing A2K3 to energize if airflow sensor relay A2K1 has been activated by cabinet airflow.

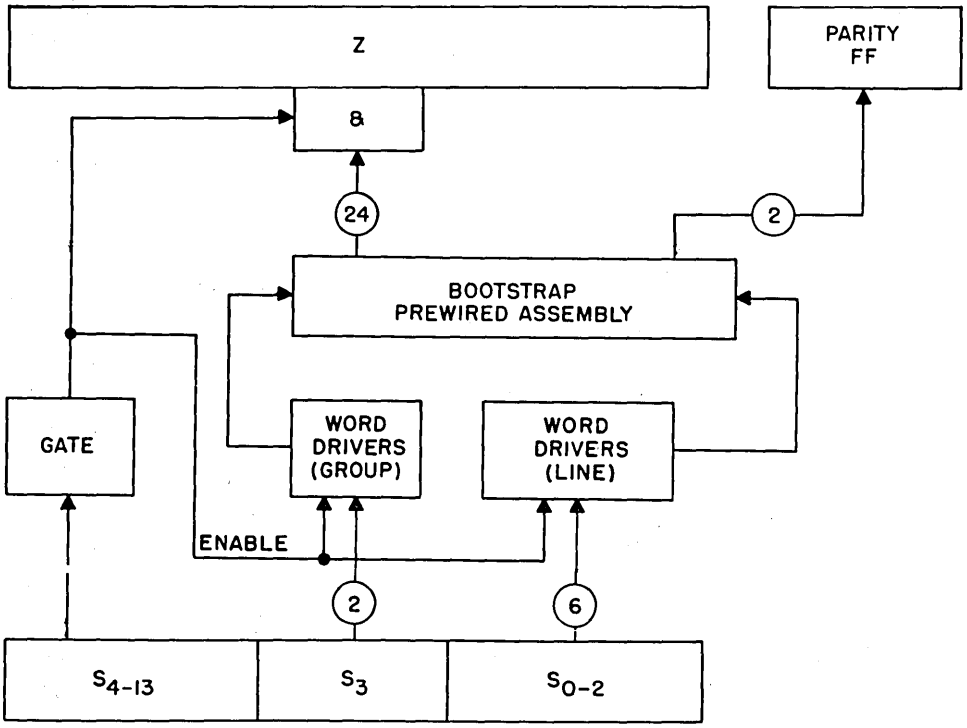


Figure 4-79. Bootstrap Block Diagram

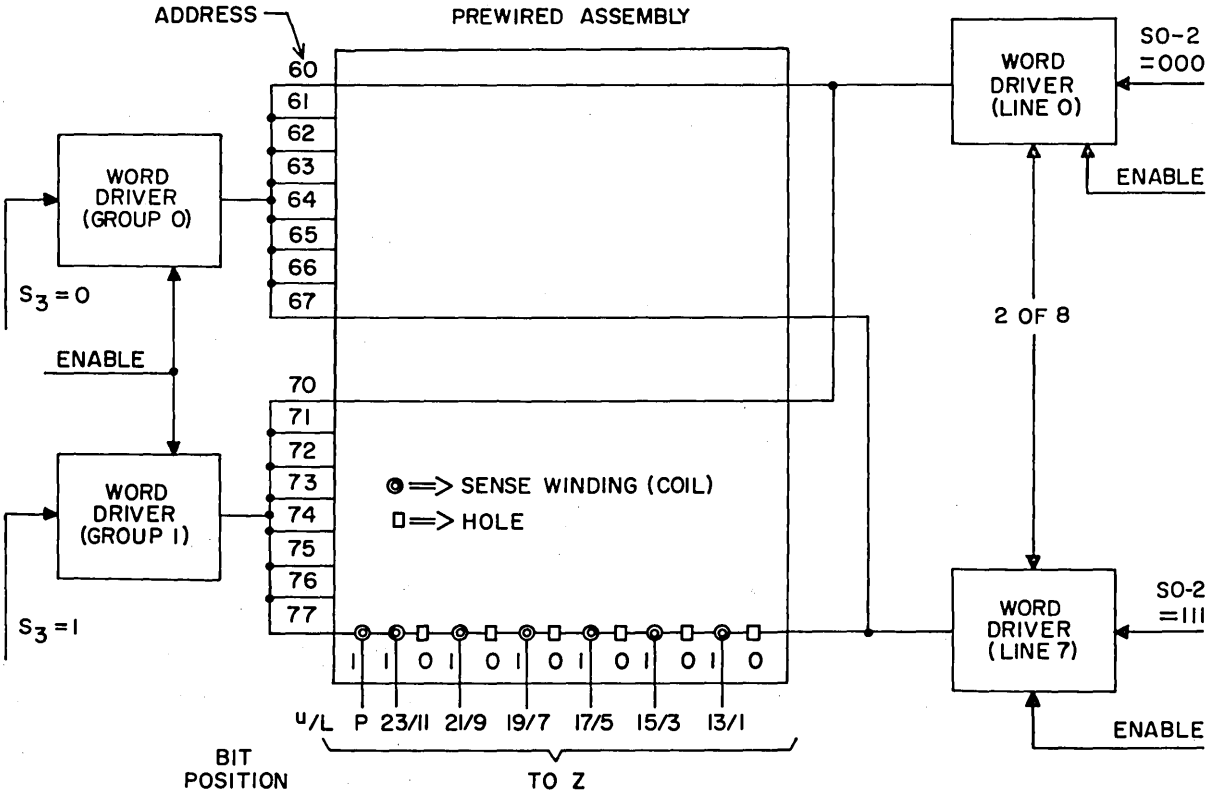


Figure 4-80. Bootstrap Operation

4) Relay A2K3 contacts 2-5 close to energize PS1K2 if the power supply interlock and 60°C (140°F) thermostats are closed.

5) Relay PS1K2 contacts close to energize the -15v, +15v, and -4.5v dc supplies.

The AIR FLOW BYPASS switch when operated bypasses contacts 2-5 of relay A2K3 to energize relay PS1K2 without the 30-second delay or sufficient airflow. Table 4-21, page 4-170, lists all relays and contact functions.

b. DC Supplies and Distribution (figure 8-103, page 8-221). - The dc voltage supplies are mounted in the power supply PS1. When power sequencing relay PS1K1 energizes, the +15v indicator supply (T2) is energized. The +15v indicator supply connects to all indicators in the hood control panel, and both logic panels. Energizing the +15v indicator supply before energizing the logic voltages causes all indicators to light until the logic voltages are available. Energizing power sequencing to relay PS1K2 energizes the dc logic voltage supplies (-4.5, -15, and +15). The logic voltage and ground distribution networkds and test points are shown in figure 8-103, page 8-221. The fuses protecting each voltage supply are listed in table 5-3, page 5-10.

c. Fault Indicator Control Circuits (figure 8-101, page 8-217). - The fault indicator control circuits consist of three flip-flops, driver circuits, indicators, and the fault horn.

(1) Airflow fault circuits. - The airflows fault circuits are activated when the airflow is insufficient to hold relay A2K1 contact closed. When relay A2K1 contact opens, relay A2K3 de-energizes. Contact A2-A3 of A2K3 closes to light the AIR FLOW FAULT indicator, and contact A2-A1 opens applying a logic low to AND gate 1 of 94V01 which has been conditioned by flip-flop 9XV52. When 94V01 is enabled, the horn sounds until the airflow fault drops or the FAULT DISC HORN/HORN CLEAR switch is placed to HORN CLEAR to clear flip-flop 9XV52. Flip-flop 9XV52 is set again when the airflow fault drops.

(2) Overtemperature fault circuits. - The overtemperature fault circuits are activated when either of the 46°C (115°F) thermostats close. In the quiescent state the overtemperature flip-flop 9XV51 is held set by a constant enable, and AND gate 2 of 94V01 is conditioned. When internal cabinet temperature exceeds 46°C (115°F), one or both of the thermostats

TABLE 4-21. Power Relay Contact Functions

Relay	Location	Contact	State	Function
K1	PS1			Power sequencing.
		A1-A2	NO.	ØA to blowers and +15v indicator supply.
		B1-B2	NO.	ØB to blowers, +15v indicator supply and heaters on A2K1 and A2K2.
		C1-C2	NO.	ØC to blowers, +15v indicator supply, and PS1K2 coil.
		D1-D2	NO.	Holding path.
K2	PS1			Power sequencing.
		A1-A2	NO.	ØA to dc supplies.
		B1-B2	NO.	ØB to dc supplies and time meter.
		C1-C2	NO.	ØC to dc supplies.
		D1-D2	NO.	Holding path.
K1	A2			Airflow sensor.
		3-8	NC	Opens if no air flow.
K2	A2			30-second time delay (approximately).
		5-7	NO.	Closes approximately 30 seconds after heater voltage applied.
K3	A2			Power sequencing.
		B1-B2	NO.	Energize PS1K1.
		A2-A1	NO.	Holding path.
		A2-A3	NC	AIR FLOW FAULT indicator.

will close applying a logic high to 93V02 which enables 94V01 to sound the horn and 93V03 to light the OVERTEMP indicator. This condition remains until the FAULT DISC HORN/HORN CLEAR switch is placed to HORN CLEAR to clear flip-flop 9XV51 or until the cabinet temperature drops to disable 94V01 and 93V03. If the switch is used, flip-flop 9XV51 clears and the horn is silenced, but the indicator remains lighted. In this condition the horn will not sound until another fault occurs. When the overtemperature fault drops, the horn is silenced (if the FAULT DISC HORN/HORN CLEAR switch was not used), the OVER TEMP indicator goes out, and the constant set enable is applied to flip-flop 9XV51.

(3) Logic fault circuits. - The logic fault circuits are activated when a logic fault (see paragraph 4-16i, page 4-82) occurs. In the quiescent state the fault flip-flop 9XV50 receives a constant set enable to condition AND gate 4 of 94V01. When the fault occurs the fault flip-flop enables 91V04 and 91V03 to light the FAULT indicator and activate the horn. This condition remains until the FAULT DISC HORN/HORN CLEAR switch is placed to HORN CLEAR which clears flip-flop 9XV05 and silences the horn. If the switch has been placed in the DISC HORN position prior to the fault, the horn will not sound when the fault occurs. When the logic fault condition drops, the constant set enable is placed on 9XV50, AND gate 4 of 94V01 is disabled to silence the horn, and 91V04 is disabled to extinguish the FAULT indicator.

IV - INSTRUCTION TIMING

4-21. INSTRUCTION TIMING CHARTS. - The instruction timing charts list the sequences required to execute the instruction and the functions performed during each clock phase of each sequence.

These timing charts are good reference data for maintenance personnel already familiar with the operation of the computer. Table 4-22, page 4-172, is an index to the instruction timing charts for the complete repertoire of instructions. The charts are subdivided according to function code and mnemonic notation.

TABLE 4-22. Index of Timing Charts

Mnemonic	Function Code (and 06 - Sub-Order)	Table	Page
HLT, HLD	00, 11, 37	4-23	4-174
LGN	01	4-24	4-175
TRF	02	4-25	4-176
TSR	03	4-26	4-177
TRX	04	4-27	4-178
TAX	05	4-28	4-179
SCN, SAN, SXN, SLN (SHL) I, R, W-Sequences Shift-Sequences	06-0 Mode = 1 + $\overline{(RCA)}$	4-29	4-180
SCD, SAD, SXD, SLD (SHL) I, R, W-Sequences Shift-Sequences	06-0 Mode = 0 · (RCA)	4-30	4-183
DIV I, M, R, W-Sequences Shift-Sequence	06-1	4-31	4-187
SCA	06-2	4-32	4-189
SCL I, R, W-Sequences Shift-Sequence	06-3	4-33	4-191
SCR, SAR, SXR, SLR (SHR) I, R, W-Sequences Shift-Sequences	06-4	4-34	4-193
MUL I, R, W-Sequences Shift-Sequence	06-5	4-35	4-196
SUD I, R, W-Sequences Shift-Sequence	06-6	4-36	4-198

TABLE 4-22. Index of Timing Charts (continued)

Mnemonic	Function Code (and 06 - Sub-Order)	Table	Page
Reload-Sequences (RC1, RC2, WC)		4-37	4-201
R/W-Sequence		4-38	4-202
EXF	07	4-39	4-204
CLR	10	4-40	4-205
STR	12	4-41	4-208
RPA	13	4-42	4-207
TRU	14	4-43	4-208
TRA	15	4-44	4-209
TRD	16	4-45	4-210
SWC	17	4-46	4-211
EXC	20	4-47	4-213
ADC	21	4-48	4-215
ADO	22	4-49	4-216
AID	23	4-50	4-218
RCA	24	4-51	4-220
ERC	25	4-52	4-222
STX, SRC	26	4-53	4-224
LDX, LRC	27	4-54	4-226
CLA	30	4-55	4-228
ADD	31	4-56	4-229
SUB	32	4-57	4-230
COM	33	4-58	4-231
LGA	34	4-59	4-233
LGM	35	4-60	4-235
ADB	36	4-61	4-236
Interrupt-Sequences		4-62	4-237

TABLE 4-23. f = 00, 11, 37, Instruction Timing Chart

HLT, HLD	
Time	I-Sequence
6.4	Clr: S, Z
1.1	P $\longrightarrow$ S
1.2	Clr: X, D Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D
2.2	Strobe Memory Clr: P
2.3	Adder $\longrightarrow$ P
3.2	Clr: X, D, F, M
3.3	$Z_{0 - 13} \longrightarrow$ X, $Z_{14 - 18} \longrightarrow$ M, Note: $Z_{0 - 18}$ Not Used $Z_{19 - 23} \longrightarrow$ F, Clr: K_0
4.4	Set: Halt FF
5.2	Clr: Run FF
5.4	Clr: I-Seq
6.1	Set: NI or I/O-Seq

TABLE 4-24. f = 01, Instruction Timing Chart

LGN	
Time	I-Sequence
6.4	Clr: S, Z
1.1	P → S
1.2	Clr: X, D Initiate Memory
1.3	P → X, +1 → D
2.2	Strobe Memory Clr: P
2.3	Adder → P
3.2	Clr: X, D, F, M
3.3	$Z_{0-13} \rightarrow X$, $Z_{14-18} \rightarrow M$ Note: Z_{0-18} Not Used $Z_{19-23} \rightarrow F$, Clr: K_0
4.1	$\overline{A} \rightarrow D$
4.2	Initiate Arithmetic Timing Chain
5.2	Clr: X (1)
5.4	Clr: I-Seq Clr: A (1)
6.1	Set: NI or I/O-Seq X ⊕ D → A (1)

(1) Enabled by Arithmetic Timing Chain

TABLE 4-25. f = 02, Instruction Timing Chart

TRF	
Time	I-Sequence
6.4	Clr: S, Z
1.1	P $\longrightarrow$ S
1.2	Clr: X, D Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D
2.2	Clr: P Strobe Memory
2.3	Adder $\longrightarrow$ P
3.2	Clr: X, D, F, M
3.3	$Z_{0 - 13} \longrightarrow$ X, $Z_{14 - 18} \longrightarrow$ M, $Z_{19 - 23} \longrightarrow$ F Clr: K_0
5.4	Clr: I-Seq
6.1	Set: NI or I/O-Seq
6.2	If Jump FF Clr, Clr: P If RS/S type FF, Clr: Sensed Status FF (1)
6.3	If Jump FF, Clr: Adder $\longrightarrow$ P

(1) FF may be cleared as late as time 6.4, depending on waveform of T11.

TABLE 4-26. f = 03, Instruction Timing Chart

TSR		
Time	I-Sequence	W-Sequence
6.4	Clr: S, Z	Clr: S, Z
1.1	P $\longrightarrow$ S	M $\longrightarrow$ S
1.2	Clr: X, D Initiate Memory	Clr: X Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D	P $\longrightarrow$ X
2.1		$X_{0 - 13} \longrightarrow Z$
2.2	Strobe Memory Clr: P	Strobe Memory Upper Clr: P
2.3	Adder $\longrightarrow$ P	D $\longrightarrow$ P
3.2	Clr: X, D, F, M	
3.3	$Z_{0 - 13} \longrightarrow X$, $Z_{14 - 18} \longrightarrow M$ $Z_{19 - 23} \longrightarrow F$, Clr: K_0	
5.1	X $\longrightarrow$ D	
5.4	Clr: I-Seq	Clr: W-Seq
6.1	Set: W-Seq	Set: NI or I/O-Seq

TABLE 4-27. f = 04, Instruction Timing Chart

TRX			
Time	I Sequence	R-Sequence	W-Sequence
6.4	Clr: S, Z	Clr: S, Z	Clr: S, Z
1.1	P $\longrightarrow$ S	M $\longrightarrow$ S	M $\longrightarrow$ S, Adder $\longrightarrow$ Z
1.2	Clr: X, D Initiate Memory	Initiate Memory	Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D		
2.1		X $\longrightarrow$ D	
2.2	Strobe Memory Clr: P	Strobe Memory	
2.3	Adder $\longrightarrow$ P		
3.2	Clr: X, D, F, M	Clr: X If $Z_{14 - 23} \neq 0$, Clr: P	
3.3	$Z_{0 - 13} \longrightarrow$X, $Z_{14 - 18} \longrightarrow$M, $Z_{19 - 23} \longrightarrow$F, Clr: K_0	If $Z_{14 - 23} \neq 0$, D $\longrightarrow$ P, Z $\longrightarrow$ X	
4.2		Clr: D	
4.3		Set: $D_{14 - 23}$, Force Borrow Enable FF (1)	
5.4	Clr: I-Seq	Clr: R-Seq	Clr: W-Seq
6.1	Set: R-Seq	If $Z_{14 - 23} \neq 0$, Set: W-Seq If $Z_{14 - 23} = 0$, Set: NI or I/O-Seq	Set: NI or I/O-Seq

(1) Forced End Around Borrow

TABLE 4-28. f = 05, Instruction Timing Chart

TAX			
Time	I-Sequence	R-Sequence	W-Sequence
6-4	Clr: S, Z	Clr: S, Z	Clr: S, Z
1.1	P $\longrightarrow$ S	M $\longrightarrow$ S	M $\longrightarrow$ S, Adder $\longrightarrow$ Z
1.2	Clr: X, D Initiate Memory	Initiate Memory	Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D		
2.1		X $\longrightarrow$ D	
2.2	Strobe Memory Clr: P	Strobe Memory	
2.3	Adder $\longrightarrow$ P		
3.2	Clr: X, D, F, M	Clr: X If $Z_{14-23} \neq 0$, Clr: P	
3.3	$Z_{0-13} \longrightarrow$X $Z_{14-18} \longrightarrow$M, $Z_{19-23} \longrightarrow$M, Clr: K_0	If $Z_{14-23} \neq 0$: D $\longrightarrow$ P, Z $\longrightarrow$ X	
4.2		Clr: D	
4.3		Set: D_{14-23}, Force Borrow Enable FF (1)	
5.4	Clr: I-Seq	Clr: R-Seq	Clr: W-Seq
6.1	Set: R-Seq	If $Z_{14-23} \neq 0$, Set: W-Seq If $Z_{14-23} = 0$, Set: NI or I/O-Seq	Set: NI or I/O-Seq
6.2		If M = 37, Clr: B	
6.3		If M = 37, Adder $\longrightarrow$ B (2)	

(1) No Forced End Around Borrow
(2) B is incremented by 1

TABLE 4-29. f = 06-0, Mode = 1 + ($\overline{RCA}$), Instruction Timing Chart

SCN, SAN, SXN, SLN			
Time	I-Sequence	R-Sequence	W-Sequence
6.4	Clr: S, Z	Clr: S, Z	Clr: S
1.1	P ⟶ S	M ⟶ S	M ⟶ S
1.2	Clr: X, D Initiate Memory	Initiate Memory	Initiate Memory
1.3	P ⟶ X, +1 ⟶ D		
2.2	Strobe Memory Clr: P	Strobe Memory	
2.3	Adder ⟶ P		
3.2	Clr: X, D, F, M	Clr: X (d)	
3.3	Z_{0-13} ⟶ X Z_{14-18} ⟶ M, Z_{19-23} ⟶ F, Clr: K_0	Z ⟶ X (d)	
4.4	Z_{0-4} ⟶ K_0, Clr: Type, Mode, CAT FF's		
5.1	Enable: Type, Mode, CAT FF's		
5.4	Clr: I-Seq If Type 0X · K_0 = 0, Set: SHF CTL FF 1	Clr: R-Seq If $K_0 \neq 0$, Set: SHF CTL FF 1	Clr: W-Seq
6.1	If Type 1X: Set: R-Seq If Type 0X · K_0 = 0, Set: NI or I/O-Seq, Clr: K_1	If K_0 = 0, Set: NI or I/O-Seq Clr: K_1	Set: NI or I/O- Seq
6.2	If SHF CTL FF1 Set, Set: SHF CTL FF2 & Begin SHL Shift-Seq	If SHF CTL FF1 Set, Set: SHF CTL FF2 & Begin SHL Shift- Seq	

(d) Don't Care Condition.

TABLE 4-29. f = 06-0, Mode = 1 + ($\overline{RCA}$), Instruction Timing Chart (continued)

SHL Shift-Sequence		
Time	SCN Type 00	Column B
Ø2	Clr: U, A_{24} $(K_0 - 1) \longrightarrow K_1$	Clr: SHF CTL FF2
Ø3	$A_{L1} \longrightarrow U$, $A_{23} \longrightarrow A_{24} \longrightarrow U_{00}$ Clr: K_0	
Ø4	Clr: A $K_1 \longrightarrow K_0$ If $K_1 = 0$, Clr: SHF CTL FF1, Set: NI or I/O-Seq	Begin NI or I/O-Seq (T6.4)
Ø1	$U \longrightarrow A$ Clr: K_1 If NI or I/O-Seq set, go to Column B; if not, repeat this column	
	SAN Type 01	Column B
Ø2	Clr: U, A_{24} $(K_0 - 1) \longrightarrow K_1$	Clr: SHF CTL FF2
Ø3	$A_{L1} \longrightarrow U$, $A_{23} \longrightarrow A_{24}$ Clr: K_0	
Ø4	Clr: A $K_1 \longrightarrow K_0$ If $K_1 = 0$, Clr: SHF CTL FF1, Set: NI or I/O-Seq	Begin NI or I/O-Seq (T6.4)
Ø1	$U \longrightarrow A$ Clr: K_1 If NI or I/O-Seq set, go to Column B; if not, repeat this column	
	SXN Type 10	Column B
Ø2	Clr: X $(K_0 - 1) \longrightarrow K_1$	Clr: SHF CTL FF2
Ø3	$Z_{L1} \longrightarrow X$ Clr: K_0	
Ø4	Clr: Z $K_1 \longrightarrow K_0$ If $K_1 = 0$, Clr: SHF CTL FF1, Set: W-Seq	Begin W-Seq (T6.4, page 4-180)
Ø1	$X \longrightarrow Z$ Clr: K_1 If W-Seq set, go to Column B; if not, repeat this column	

TABLE 4-29. f = 06-0, Mode = 1 + (RCA), Instruction Timing Chart (continued)

SHL Shift-Sequence		
Time	SLN Type 11	Column B
Ø2	Clr: X, U, A_{24} $(K_0 - 1) \longrightarrow K_1$	Clr: SHF CTL FF2
Ø3	$A_{L1} \longrightarrow U$, $A_{23} \longrightarrow A_{24}$, $Z_{L1} \longrightarrow X$, $A_{23} \longrightarrow X_{00}$ Clr: K_0	
Ø4	Clr: A, Z $K_1 \longrightarrow K_0$ If $K_1 = 0$, Clr: SHF CTL FF1, Set: W-Seq	Begin W-Seq (T6.4, page 4-180)
Ø1	$U \longrightarrow A$, $X \longrightarrow Z$, Clr: K_1 If W-Seq set, go to Column B; if not, repeat this column	

TABLE 4-30. f = 06-0, Mode = 0 · (RCA), Instruction Timing Chart

SCD, SAD, SXD, SLD		
Time	I-Sequence	
6.4	Clr: S, Z	
1.1	P → S	
1.2	Clr: X, D Initiate Memory	
1.3	P → X, +1 → D	
2.2	Clr: P Strobe Memory	
2.3	Adder → P	
3.2	Clr: X, D, F, M	
3.3	$Z_{0-13} \rightarrow X$, $Z_{14-18} \rightarrow M$, $Z_{19-23} \rightarrow F$, Clr: K_0	
4.4	$Z_{0-4} \rightarrow K_0$, Clr: Type, Mode, CAT FF's	
5.1	Enable: Type, Mode, CAT FF's	
	If $RC_0 = 0$:	If $RC_0 \neq 0$:
5.3	If Type 0X, Set: REL REQ FF	
5.4	Clr: I-Seq	Clr: I-Seq If Type 0X · $K_0 \neq 0$, Set: SHF CTL FF1
	If Type 1X, Set: R-Seq (page 4-184)	
6.1	If Type 0X, Set: RC1-Seq (table 4-37, page 4-201)	If Type 0X · $K_0 = 0$, Set: NI or I/O-Seq. Clr: K_1
6.2		If SHF CTL FF1 Set, Set: SHF CTL FF2; Begin Shift- Seq (page 4-185)

TABLE 4-30. f = 06-0, Mode = 0 · (RCA), Instruction Timing Chart (continued)

SCD, SAD, SXD, SLD			
Time	R-Sequence		W-Sequence
6.4	Clr: S, Z		Clr: S, BT FF
1.1	M → S		M → S
1.2	Initiate Memory		Initiate Memory
2.2	Strobe Memory		
3.2	Clr: X		
3.3	Z → X		
	If $RC_0 = 0$:	If $RC_0 \neq 0$:	
4.2	Initiate Arithmetic Timing Chain		
5.1	$\overline{X}$ → D (1)		
5.2	Clr: X (1)		
5.3	A → X (1) Set: REL REQ FF		
5.4	Clr: R-Seq Clr: A (1)	Clr: R-Seq If $K_0 \neq 0$, Set: SHF CTL FF1	Clr: W-Seq
6.1	Set: RC1-Seq (table 4-37, page 4-201) $\overline{D}$ → A (1)	If $K_0 = 0$, Set: NI or I/O-Seq Clr: K_1, RC_1	Set: NI or I/O-Seq
6.2		If SHF CTL FF1 Set, Set SHF CTL FF2, Begin Shift-Seq (page 4-185)	

1 Enabled by Arithmetic Timing Chain

TABLE 4-30. f = 06-0, Mode = 0 · (RCA), Instruction Timing Chart (continued)

SHL Shift-Sequences		
Time	SCD Type 00	Column B
ø2	Clr: U, A_{24} (K_0 - 1) → K_1, (RC_0 - 1) → RC_1	Clr: SHF CTL FF2 Clr: X, D (1)
ø3	A $_{L1}$ → U, A_{23} → A_{24} → U_{00} Clr: K_0, RC_0	Z → X (1)
ø4	Clr: A K_1 → K_0, RC_1 → RC_0 If K_1 = 0 · RC_1 ≠ 0: (2) Clr SHF CTL FF1, Set: NI or I/O-Seq If RC_1 = 0, (2) Clr: SHF CTL FF1, Initiate Arithmetic Timing Chain; Set: Reload REQ FF and RC1-Seq	Begin NI or I/O-Seq (T6.4) or RC1-Seq (T6.4, table 4-37, page 4-201) Clr: A (1)
ø1	U → A Clr: K_1, RC_1, Reload FF If NI, I/O, or RC1-Seq set, go to Column B. If not, repeat this column.	X ⊕ D → A (1)
	SAD Type 01	Column B
ø2	Clr: U, A_{24} (K_0 - 1) → K_1 (RC_0 - 1) → RC_1	Clr: SHF CTL FF2 Clr: X, D (1)
ø3	A $_{L1}$ → U, A_{23} → A_{24} Clr: K_0, RC_0	Z → X (1)
ø4	Clr: A K_1 → K_0, RC_1 → RC_0 If K_1 = 0 · RC_1 ≠ 0, (2) Clr: SHF CTL FF1, Set: NI or I/O-Seq; If RC_1 = 0, (2) Clr: SHF CTL FF1, Initiate Arithmetic Timing Chain, Set: Reload REQ FF, RC1-Seq	Begin NI or I/O-Seq (T6.4) or RC1-Seq (T6.4, table 4-37, page 4-201) Clr: A (1)
ø1	U → A Clr: K_1, RC_1, Reload FF If NI, I/O, or RC1-Seq set, go to Column B. If not, repeat this column.	X ⊕ D → A (1)

1 Enabled By Arithmetic Timing Chain.

2 If RC_1 = 0 · K_1 = 0 at same time, reload operation (table 4-37, page 4-201) will occur first; and then NI or I/O-Seq will be set, completing shift instruction.

TABLE 4-30. f = 06-0, Mode = 0 · (RCA), Instruction Timing Chart (continued)

SHL Shift-Sequence		
Time	SXD Type 10	Column B
Ø2	Clr: X (K_0 - 1) → K_1, (RC_0 - 1) → RC_1	Clr: SHF CTL FF2 Clr: X, D (1)
Ø3	Z $_{L1}$ → X, Clr: K_0, RC_0	Z → X (1)
Ø4	Clr: Z K_1 → K_0, RC_1 → RC_0 If K_1 = 0 · $RC_1 \neq 0$, (2) Clr: SHF CTL FF1, Set: W-Seq; If RC_1 = 0, (2) Clr: SHF CTL FF1, Initiate Arithmetic Timing Chain, Set: Reload REQ FF and RC1-Seq.	(T6.4) Begin W-Seq (page 4-184) or RC1-Seq (table 4-37, page 4-201). Clr: A (1)
Ø1	X → Z Clr: K_1, RC_1, Reload FF If RC1 or W-Seq set, go to Column B. If not, repeat this column.	X ⊕ D → A (1)
	SLD Type 11	Column B
Ø2	Clr: X, U, A_{24} (K_0 - 1) → K_1, (RC_0 - 1) → RC_1	Clr: SHF CTL FF2 Clr: X, D (1)
Ø3	A $_{L1}$ → U, Z $_{L1}$ → X, A_{23} → A_{24} → X_{00} Clr: K_0, RC_0	Z → X (1)
Ø4	Clr: Z, A K_1 → K_0, RC_1 → RC_0 If K_1 = 0 · $RC_1 \neq 0$, (2) Clr: SHF CTL FF1, Set: W-Seq; If RC_1 = 0, (2) Clr: SHF CTL FF1, Initiate Arithmetic Timing Chain, Set Reload REQ FF and RC1-Seq	(T6.4) Begin W-Seq (page 4-184) or RC1-Seq (table 4-37, page 4-201) Clr: A 1
Ø1	U → A, X → Z Clr: K_1, RC_1, Reload FF If RC1 or W-Seq set, go to Column B. If not, repeat this column.	X ⊕ D → A (1)

(1) Enable By Arithmetic Timing Chain.
(2) If RC_1 = 0 · K_1 = 0 at same time, reload operation (table 4-37, page 4-201) will occur first; and then W-Seq (page 4-184) will be set, completing shift instruction.

TABLE 4-31. f = 06-1, Instruction Timing Chart

DIV		
Time	I-Sequence	M-Sequence
6.4	Clr: S, Z	Clr: X, Z
1.1	P $\longrightarrow$ S	M $\longrightarrow$ S, Adder $\longrightarrow$ Z
1.2	Clr: X, D Initiate Memory	Clr: M Initiate Memory Clr: X, D, d
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D	$Z_{9-13} \longrightarrow$ M, $Z_{0-13} \longrightarrow$ X (d)
1.4		Clr: Z
2.2	Clr: P Strobe Memory	Strobe Memory
2.3	Adder $\longrightarrow$ P	
3.2	Clr: X, D, F, M	Clr: X Initiate Arithmetic Timing Chain
3.3	$Z_{0-13} \longrightarrow$ X, $Z_{14-18} \longrightarrow$ M $Z_{19-23} \longrightarrow$ F, Clr: K_0	Z $\longrightarrow$ X
4.1		$\overline{X} \longrightarrow$ D (1)
4.2		Clr: X (1)
4.3		A $\longrightarrow$ X (1)
4.4	$Z_{0-4} \longrightarrow K_0$ Clr: Type, Mode, CAT FF's	
5.1	Enable: CAT FF's	
5.4	Clr: I-Seq	Clr: M-Seq
6.1	If M $\neq$ 0 + 37, Set: M-Seq If M = 0 + 37, Set: R-Seq	Set: R-Seq

(1) Enabled by Arithmetic Timing Chain
(d) Don't-Care Condition

TABLE 4-31. f = 06-1, Instruction Timing Chart (continued)

DIV		
Time	R-Sequence	W-Sequence
6.4	Clr: S, Z	Clr: S
1.1	M $\longrightarrow$ S	M $\longrightarrow$ S
1.2	Initiate Memory	Initiate Memory
2.2	Strobe Memory	
3.2	Clr: X (d)	
3.3	Z $\longrightarrow$ X	
5.4	Clr: R-Seq, If $K_0 \neq 0$, Set: SHF CTL FF1	Clr: W-Seq
6.1	If $K_0 = 0$, Set: NI or I/O-Seq Clr: K_1	Set: NI or I/O-Seq
6.2	If SHF CTL FF1 Set, Set: SHF CTL FF2, Begin DIV Shifting-Seq	
	DIV Shifting Sequences	Column B
Ø2	Clr: X, U $(K_{0-1}) \longrightarrow K_1$	Clr: SHF CTL FF2
Ø3	A $_{L1} \longrightarrow$ U, Z $_{L1} \longrightarrow$ X, $A_{23} \longrightarrow X_{00}$ Clr: K_0 Set: SHF CYC FF1	
Ø4	Clr: Z, A $K_1 \longrightarrow K_0$	Begin W-Seq (6.4)
Ø1	U $\longrightarrow$ A (1) Set: SHF CYC FF2	
Ø2		
Ø3	Clr: SHF CYC FF1	
Ø4	Clr: A (1) If $K_1 = 0$, Clr: SHF CTL FF1, Set: W-Seq	
Ø1	U $\longrightarrow$ A, Clr: K_1 Clr: SHF CYC FF2 If X $\geq \overline{D}$: Adder $\longrightarrow$ Z, +1 $\longrightarrow A_{00}$ If X < $\overline{D}$: X $\longrightarrow$ Z, 0 $\longrightarrow A_{00}$ If W-Seq is set, go to Column B; if not, repeat this column	

(d) Don't-Care Condition
(1) May or may not occur due to race condition; has no effect on final result.

TABLE 4-32. f = 06-2, Instruction Timing Chart

SCA		
Time	I-Sequence	
6.4	Clr: S, Z	
1.1	P $\longrightarrow$ S	
1.2	Clr: X, D Initiate Memory	
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D	
2.2	Strobe Memory Clr: P	
2.3	Adder $\longrightarrow$P	
3.2	Clr: X, D, F, M	
3.3	$Z_{0-13} \longrightarrow$X, $Z_{14-18} \longrightarrow$M, $Z_{19-23} \longrightarrow$F, Clr: K_0	
4.4	$Z_{0-4} \longrightarrow K_0$ Clr: Type, Mode, CAT FF's	
5.1	Enable: CAT FF's	
	If $A_{22} = A_{23}$:	If $A_{22} \neq A_{23}$:
5.4	Clr: I-Seq If $K_0 \neq 0$, Set: SHF CTL FF1	Clr: I-Seq
6.1	If $K_0 = 0$, Set: NI or I/O-Seq Clr: K_1	Set: NI or I/O-Seq
6.2	If SHF CTL FF1 Set, Set: SHF CTL FF2, Begin Shift Seq	

TABLE 4-32. f = 06-2, Instruction Timing Chart (continued)

SCA		
Time	Shift-Sequence	Column B
Ø2	Clr: X ⓓ , U (K_0 - 1)⟶K_1, (RC_0 - 1) ⟶RC_1	Clr: SHF CTL FF2
Ø3	A_{L1} ⟶U, A_{23} ⟶U_{00}, Z_{L1}⟶X (Lower) ⓓ Clr: K_0, RC_0	
Ø4	Clr: A, Z ⓓ K_1⟶K_0, RC_1 ⟶RC_0 If K_1 = 0, Clr: SHF CTL FF1, Set: NI or I/O-Seq	Begin NI or I/O-Seq (T6.4)
Ø1	U ⟶A, X⟶Z ⓓ Clr: K_1, RC_1 If $U_{22} \neq U_{23}$, Clr: SHF CTL FF1, Set: NI or I/O-Seq, go to Column B	

ⓓ Don't-Care Condition

TABLE 4-33. f = 06-3, Instruction Timing Chart

SCL				
Time	I-Sequence	R-Sequence	W-Sequence	
6.4	Clr: S, Z	Clr: S, Z	Clr: S	
1.1	P ⟶ S	M ⟶ S	M ⟶ S	
1.2	Clr: X, D Initiate Memory	Initiate Memory	Initiate Memory	
1.3	P ⟶ X, +1 ⟶ D			
2.2	Strobe Memory Clr: P	Strobe Memory		
2.3	Adder ⟶ P			
3.2	Clr: X, D, F, M	Clr: X (d)		
3.3	$Z_{0-13} \rightarrow X$, $Z_{14-18} \rightarrow M$, $Z_{19-23} \rightarrow F$, Clr: K_0	Z ⟶ X (d)		
4.4	$Z_{0-4} \rightarrow K_0$ Clr: Type, Mode, CAT FF's			
5.1	Enable: CAT FF's			
		If $Z_{21} = Z_{22}$:	If $Z_{21} \neq Z_{22}$:	
5.4	Clr: I-Seq	Clr: R-Seq If $K_0 \neq 0$, Set: SHF CTL FF1	Clr: R-Seq	Clr: W-Seq
6.1	Set: R-Seq	Clr: K_1 If $K_0 = 0$, Set: NI or I/O-Seq	Set: W-Seq	Set: NI or I/O-Seq
6.2		If SHF CTL FF1 Set, Set: SHF CTL FF2, Begin Shifting-Seq		

(d) Don't-Care Condition

TABLE 4-33. f = 06-3, Instruction Timing Chart (continued)

SCL		
Time	SCL Shifting Sequence	Column B
Ø2	Clr: X, U $(K_0 - 1) \rightarrow K_1$, $(RC_0 - 1) \rightarrow RC_1$	Clr: SHF CTL FF2
Ø3	$A_{L1} \rightarrow U$, A_{23} X_{00}, $Z_{L1} \rightarrow X$, $Z_{23} \rightarrow U_{00}$ If $Z_{20} \neq Z_{21}$: Set: BITS DIFF FF Clr: K_0, RC_0	Clr: BITS DIFF FF
Ø4	Clr: A, Z $K_1 \rightarrow K_0$, $RC_1 \rightarrow RC_0$ If $K_1 = 0$, Clr: SHF CTL FF1, Set: W-Seq If BITS DIFF FF Set, Set: W-Seq	(T6.4) Begin W-Seq
Ø1	$U \rightarrow A$, $X \rightarrow Z$ Clr: K_1, RC_1 If BITS DIFF FF Set, Clr: SHF CTL FF1 If W-Seq is set, go to Column B; if not repeat this column	

TABLE 4-34. f = 06-4, Instruction Timing Chart

SCR, SAR, SXR, SLR			
Time	I-Sequence	R-Sequence	W-Sequence
6.4	Clr: S, Z	Clr: S, Z	Clr: S
1.1	P $\longrightarrow$ S	M $\longrightarrow$ S	M $\longrightarrow$ S
1.2	Clr: X, D Initiate Memory	Initiate Memory	Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D		
2.2	Strobe Memory Clr: P	Strobe Memory	
2.3	Adder $\longrightarrow$ P		
3.2	Clr: X, D, F, M	Clr: X	
3.3	$Z_{0-13} \rightarrow X$, $Z_{14-18} \rightarrow M$, $Z_{19-23} \rightarrow F$, Clr: K_0	Z $\longrightarrow$ X	
4.4	$Z_{0-4} \longrightarrow K_0$ Clr: Type, Mode, CAT FF's		
5.1	Enable: Type, Mode, CAT FF's		
5.4	Clr: I-Seq If Type 0X · $K_0 \neq 0$, Set: SHF CTL FF1	Clr: R-Seq If $K_0 \neq 0$, Set: SHF CTL FF1	Clr: W-Seq
6.1	Clr: K_1 If Type 0X · $K_0 = 0$, Set: NI or I/O-Seq If Type 1X, Set: R-Seq	Clr: K_1 If $K_0 = 0$: Set: NI or I/O-Seq	Set: NI or I/O-Seq
6.2	If SHF CTL FF1 Set, Set: SHF CTL FF2, Begin Shift-Seq	If SHF CTL FF1 Set, Set: SHF CTL FF2, Begin Shift-Seq	

TABLE 4-34. f = 06-4, Instruction Timing Chart (continued)

SHR Shift-Sequences		
Time	SCR Type 00	Column B
Ø2	Clr: U, A_{24} (K_{0-1}) → K_1	Clr: SHF CTL FF2
Ø3	A_{R1} → U, A_{00} → A_{24} → U_{23} Clr: K_0	
Ø4	Clr: A K_1 → K_0 If K_1 = 0, Clr: SHF CTL FF1, Set: NI or I/O-Seq	Begin NI or I/O-Seq (T6.4)
Ø1	U → A Clr: K_1 If NI or I/O-Seq set, go go Column B; if not, repeat this column	
	SAR Type 01	Column B
Ø2	Clr: U (K_{0-1}) → K_1	Clr: SHF CTL FF2
Ø3	A_{R1} → U Clr: K_0	
Ø4	Clr: A K_1 → K_0 If K_1 = 0, Clr: SHF CTL FF1, Set: NI or I/O-Seq	Begin NI or I/O-Seq (T6.4)
Ø1	U → A Clr: K_1 If NI or I/O-Seq set, go to Column B; if not, repeat this column	
	SXR Type 10	Column B
Ø2	Clr: X, A_{24} (K_{0-1}) → K1	Clr: SHF CTL FF2
Ø3	Z_{R1} → X, Z_{00} → A_{24} Clr: K_0	
Ø4	Clr: Z K_1 → K_0 If K_1 = K_0, Clr: SHF CTL FF1, Set : W-Seq	Begin W-Seq (T6.4)
Ø1	X → Z Clr: K_1 If W-Seq set, go to Column B, if not, repeat this column	

TABLE 4-34. f = 06-4, Instruction Timing Chart (continued)

SHR Shift-Sequences		
Time	SLR Type 11	Column B
Ø2	Clr: X, U, A_{24} (K_{0-1}) $\longrightarrow K_1$	Clr: SHF CTL FF2
Ø3	$A_{R1} \longrightarrow U$, $Z_{R1} \longrightarrow X$, $Z_{00} \longrightarrow A_{24} \longrightarrow U_{23}$ Clr: K_0	
Ø4	Clr: A, Z $K_1 \longrightarrow K_0$ If $K_1 = 0$, Clr: SHF CTL FF1, Set: W-Seq	Begin W-Seq (T6.4)
Ø1	$U \longrightarrow A$, $X \longrightarrow Z$, Clr: K_1 If W-Seq set, go to Column B; if not, repeat this column	

TABLE 4-35. f = 06-5, Instruction Timing Chart

MUL			
Time	I-Sequence	R-Sequence	W-Sequence
6.4	Clr: S, Z	Clr: S, Z	Clr: S
1.1	P $\longrightarrow$ S	M $\longrightarrow$ S	M $\longrightarrow$ S
1.2	Clr: X, D Initiate Memory	Initiate Memory	Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D		
2.2	Strobe Memory Clr: P	Strobe Memory	
2.3	Adder $\longrightarrow$ P		
3.2	Clr: X, D, F, M	Clr: X	
3.3	$Z_{0-13} \longrightarrow X$, $Z_{14-18} \longrightarrow M$, $Z_{19-23} \longrightarrow F$, Clr: K_0	Z $\longrightarrow$ X	
4.1		X $\longrightarrow$ D	
4.4	$Z_{0-4} \longrightarrow K_0$ Clr: Type, Mode, CAT FF's		
5.1	Enable: CAT FF's		
5.4	Clr: I-Seq	Clr: R-Seq If $K_0 \neq 0$, Set: SHF CTL FF1 If $A_{00} = 0$, Clr: Z	Clr: W-Seq
6.1	Set: R-Seq	Clr: K_1 If K_0 =0, Set: NI or I/O-Seq	Set: NI or I/O-Seq
6.2		If SHF CTL FF1 Set, Set: SHF CTL FF2, Begin MUL Shift-Seq	

TABLE 4-35. f = 06-5, Instruction Timing Chart (continued)

MUL		
Time	MUL Shifting Sequence	Column B
Ø2	Clr: X, U $(K_0 - 1) \rightarrow K_1$	Clr: SHF CTL FF2
Ø3	A $_{R1} \rightarrow$ U, Z $_{R1} \rightarrow$ X, $Z_{00} \rightarrow U_{23}$ Clr: K_0 Set: SHF CYC FF 1	
Ø4	Clr: Z, A $K_1 \rightarrow K_0$	Begin W-Seq (T6.4) (table 4-31, page 4-188)
Ø1	U $\rightarrow$ A (1) Set: SHF CYC FF2	
Ø2		
Ø3	Clr: SHF CYC FF1	
Ø4	Clr: A (1) If $K_1 = 0$, Clr: SHF CTL FF1, Set: W-Seq	
Ø1	U $\rightarrow$ A Clr: K_1 Clr: SHF CYC FF2 If $U_{00} + K_0 = 0$, X $\rightarrow$ Z If $U_{00} = 1 \cdot K_0 \neq 0$, Adder $\rightarrow$ Z If W-Seq is set, go to Column B; if not, repeat this column.	

(1) May or may not occur, due to race condition; has no effect on final result.

TABLE 4-36. f = 06-6, Instruction Timing Chart

SUD				
Time	I-Sequence	R-Sequence		W-Sequence
6.4	Clr: S, Z	Clr: S, Z		Clr: S, BT FF
1.1	P $\longrightarrow$ S	M $\longrightarrow$ S		M $\longrightarrow$ S
1.2	Clr: X, D Initiate Memory	Initiate Memory		Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D			
2.2	Strobe Memory Clr: P	Strobe Memory		
2.3	Adder $\longrightarrow$ P			
3.2	Clr: X, D, F, M	Clr X		
3.3	$Z_{0-13} \longrightarrow X$, $Z_{14-18} \longrightarrow M$, $Z_{19-23} \longrightarrow F$, Clr: K_0, INIT SUD FF	$Z \longrightarrow X$		
		If $RC_0 = 0$:	If $RC_0 \neq 0$:	
4.2		Initiate Arithmetic Timing Chain		
4.4	$Z_{0-4} \rightarrow K_0$, Clr: Type, Mode, CAT FF's			
5.1	Enable CAT FF's	$\overline{X} \longrightarrow D$ (1)		
5.2		Clr: X (1)		
5.3		A $\longrightarrow$ X (1) Set: REL REQ FF		

(1) Enabled by Arithmetic Timing Chain

TABLE 4-36. f = 06-6, Instruction Timing Chart (continued)

SUD				
Time	I-Sequence	R-Sequence		W-Sequence
		If $RC_0 = 0$:	If $RC_0 \neq 0$:	
5.4	Clr: I-Seq	Clr: R-Seq Clr: A (1)	Clr: R-Seq If $(A_{23} = A_{24}) +$ (INIT SUD FF Clr) $\cdot$ $(A_{23} \neq A_{24})$, Set: SHF CTL FF1	Clr: W-Seq
6.1	Set: R-Seq If $RC_0 = 0$, Set: INIT SUD FF	Set: RC1-Seq $\overline{D} \longrightarrow$ A (1)	Clr: RC_1 If $A_{23} \neq A_{24}$: Set NI or I/O-Seq	Set: NI or I/O-Seq
6.2			If SHF CTL FF1 Set, Set: SHF CTL FF2, Begin Shift-Seq	

(1) Enabled By Arithmetic Timing Chain

TABLE 4-36. f = 06-6, Instruction Timing Chart (continued)

SUD		
Time	SUD Shifting-Sequence	
Ø2	Clr: X, U, A_{24} $(RC_0 - 1) \rightarrow RC_1$ $(K_0 - 1) \rightarrow K_1$ (d)	
Ø3	A $L_1 \rightarrow$ U, $A_{23} \rightarrow A_{24}$, Z $\rightarrow$ X, +1 $\rightarrow$ D Set: SHF CYC FF1 Clr: RC_0 and INIT SUD FF If $A_{22} \neq A_{23}$, Set: BITS DIFF FF	
Ø4	Clr: Z, A $RC_1 \rightarrow RC_0$ $K_1 \rightarrow K_0$ (d)	
Ø1	U $\rightarrow$ A (2) Set: SHF CYC FF2 Clr: Reload FF	
Ø2		
Ø3	Clr: SHF CYC FF1	
Ø4	Clr: A (2) If $RC_1 = 0$, Set: RC1-Seq, Set: REL REQ FF, Clr: SHF CTL FF1, Initiate Arithmetic Timing Chain If BITS DIFF FF Set and $RC_1 \neq 0$, Set: W-Seq	
Ø1	U $\rightarrow$ A, Adder $\rightarrow$ Z Clr: RC_1, SHF CYC FF2 If BITS DIFF FF Set, Clr: SHF CTL FF1 If neither RC1-Seq nor W-Seq was set at Ø4, repeat shift-seq (Ø2)	
	If W-Seq Set:	If RC1-Seq Set:
Ø2	Clr: SHF CTL FF2	Clr: SHF CTL FF2 Clr: X, D (1)
Ø3	Clr: BITS DIFF FF	Clr: BITS DIFF FF Z $\rightarrow$ X (1)
Ø4	Go To W-Seq, Time 6.4 (Page 4-198)	Clr: A (1) RC1-Seq begins at Time 6.4 (table 4-37, page 4-201)
Ø1		X (+) D $\rightarrow$ A (1)

(1) Enabled by Arithmetic Timing Chain
(2) May or may not occur due to race condition. Has no effect on final result.
(d) Don't-Care Condition

TABLE 4-37. Reload Sequences, Instruction Timing Chart

Time	RC1-Sequence	RC2-Sequence	WC-Sequence
6.4	Clr: S, Z 40 → S	Clr: Z	Clr: S, Z 40 → S
1.1		41 → S	Adder → Z
1.2	Initiate Memory	Initiate Memory	Initiate Memory
1.4	Set: Reload FF (1)		
2.2	Strobe Memory Clr: REL REQ FF (2)	Strobe Memory	
3.2	Clr: X, D	Clr: X, D	Clr: D
3.3	Z → X	Z → X	
3.4		Inhibit Write	
4.3	If $Z_{14-20} \neq 0$, Clr: RC_0 Set: D_{14-23}	Clr: RC_0 Set D_{14-23}	
4.4	If $Z_{14-20} \neq 0$, $Z_{21-23} \rightarrow RC\overline{0}\ 2\text{-}4$	If $Z_{14-20} = 0$, Set Buffer TERM FF $Z_{21-23} \rightarrow RC0\ 2\text{-}4$	
5.4	Clr: RC1-Seq	Clr: RC2-Seq	Clr: WC-Seq
6.1	If $Z_{14-20} \neq 0$, Set: WC-Seq If $Z_{14-20} = 0$, Set: RC2-Seq	If Buffer Terminate, Set: R/W-Seq (table 4-38, page 4-202) If Not Buffer Term, Set: WC-Seq	Set: R/W-Seq

(1) FF may set as late as T2.2, depending on T23 waveshape.
(2) FF may set as late as T3.2, depending on Reload FF.

TABLE 4-38. R/W Sequence, Instruction Timing Charts

Time	$\overline{SUD}$ (SCD, SAD, SXD, SLD)		SUD
6.4	Clr: X, Z		
1.1	Adder $\longrightarrow$ S		
1.2	Initiate Memory		
2.2	Strobe Memory If $RC_0 = 0 + BT$, Clr: X		Strobe Memory
2.3	If $RC_0 = 0 + BT$, $\overline{K}_0 \longrightarrow X_0 - 4$, Set: $X_5 - 23$		
3.2	Initiate Arithmetic Timing Chain, Clr: D		
	If $RC_0 \neq 0 \cdot \overline{BT}$, Clr: X		Clr: X
3.3	If $RC_0 \neq 0 \cdot \overline{BT}$, Z $\longrightarrow$ X		Z $\rightarrow$ X
4.1	If $RC_0 \neq 0 \cdot \overline{BT}$, $\overline{X}$ $\longrightarrow$ D (1) If $RC_0 = 0 + BT$, X $\longrightarrow$ D (1)		$\overline{X}$ $\longrightarrow$ D (1)
4.2	Clr: X (1)		
4.3	A $\longrightarrow$ X (1)		
4.4	Clr: A (1)		
5.1	$\overline{D}$ $\longrightarrow$ A (1)		
5.2	Clr: D		
5.4	If $(K_0 = 0) + (RC_0 = 0) + (BT)$, Set: SHF CTL FF1	If $(K_0 \neq 0) \cdot \underline{\quad} (RC_0 \neq 0) \cdot (\overline{BT})$ Set: SHF CTL FF1 Clr: Z, R/W-Seq X $\longrightarrow$ Z	If $(RC_0 \neq 0) \cdot \overline{BT} \cdot$ (INIT SUD FF Set + $A_{23} = A_{24}$), Set: SHF CTL FF1

(1) Enabled by Arithmetic Timing Chain

TABLE 4-38. R/W Sequence, Instruction Timing Chart (continued)

Time	$\overline{\text{SUD}}$ (SCD, SAD, SXD, SLD)		SUD
6.1	If Type 0X, Set: NI or I/O-Seq If Type 1X, Set: W-Seq	Clr: K_1, RC_1	If SHF CTL FF1 Set, Clr: RC_1 If $(RC_0 = 0 + BT) + (A_{23} \neq A_{24}) \cdot$ INIT SUD FF Clr, Set: W-Seq
6.2	If $(RC_0 = 0) + BT$, Clr: RCA FF	If SHF CTL FF1 Set, Set: SHF CTL FF2	
		Begin Shift-Seq this phase (Ø2) (table 4-30, page 4-185,	Begin Shift-Seq this phase (Ø2) (table 4-36, page 4-200)
6.4	Begin NI or I/O-Seq or W-Seq (table 4-30, page 4-184) at time 6.4		If W-Seq Set: Begin W-Seq at time 6.4 (table 4-36, page 4-198)

TABLE 4-39. f = 07, Instruction Timing Chart

EXF		
Time	I-Sequence	R-Sequence
6.4	Clr: S, Z	Clr: Z
1.1	P $\longrightarrow$ S	
1.2	Clr: X, D Initiate Memory	Clr: Acknowledge FF's Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D	
2.2	Strobe Memory Clr: P	Strobe Memory
2.3	Adder $\longrightarrow$ P	
3.2	Clr: X, D, F, M	Clr: X, C Clr: D (d)
3.3	$Z_{0-13} \longrightarrow X$, $Z_{14-18} \longrightarrow M$ $Z_{19-23} \longrightarrow F$, Clr: K_0	Z $\longrightarrow$ X $Z_{0-7} \longrightarrow C$
5.1		If M $\neq$ 7, Set: Appropriate I/O FF's If M = 7, Set/Clr: INTERRUPT ARM FF (2)
5.4	Clr: I-Seq	Clr: R-Seq
6.1	Set: R-Seq	Set: NI or I/O-Seq
6.3		Set: Enable ACK FF(1)

(1) Cleared after 4 μsec; acknowledge signal is sent to I/O device during this 4-μsec period.

(2) If M = 1, Set: TCU Output Acknowledge FF
If M = 2 and Z_7 = 1, Set: External Function FF
If M = 2 and Z_8 = 1, Set: PTU Lockout FF
If M = 2 and Z_9 = 1, Set: PTU Output FF
If M = 2 and Z_{10} = 1, Set PTU Input FF
If M = 3, Set: PCU Output Acknowledge FF
If M = 4, Set: Aux CMPTR Output Acknowledge FF
If M = 6, Set: Aux CMPTR Input Acknowledge FF
If M = 7, C_6 = 1, and C_7 = 1, Set: INT ARM FF
If M = 7, C_5 = 1, C_6 = 0, and C_7 = 1, Clr: INT ARM FF

(d) Don't-Care Condition

TABLE 4-40. f = 10, Instruction Timing Chart

CLR			
Time	I-Sequence	M-Sequence	W-Sequence
6.4	Clr: S, Z	Clr: S, Z	Clr: X, Z
1.1	P ⟶ S (Instruction Address)	M ⟶ S Adder ⟶ Z	Adder ⟶ S
1.2	Clr: X, D Initiate Memory	Clr: X, D Initiate Memory	Initiate Memory
1.3	P ⟶ X, +1 ⟶ D	Z_{0-13} ⟶ X	
1.4		Clr: Z	
2.1		X ⟶ D	
2.2	Strobe Memory Clr: P	Strobe Memory	
2.3	Adder ⟶ P		
3.2	Clr: X, D, F, M	Clr: X	Clr: D ⓓ
3.3	Z_{0-13} ⟶ X, Z_{14-14} ⟶ M, Z_{19-23} ⟶ F, Clr: K_0	Z_{0-13} ⟶ X	
4.1	If Z_M = 37, X_{0-8} ⟶ D		
4.2	If Z_M = 37, Clr: X, M		
4.3	If Z_M = 37, B ⟶ X, Z_{9-13} ⟶ M		
5.4	Clr: I-Seq	Clr: M-Seq	Clr: W-Seq
6.1	If M = 0, Set: W-Seq If M ≠ 0, Set: M-Seq	Set: W-Seq	Set: NI or I/O-Seq

ⓓ Don't-Care Condition

TABLE 4-41. f = 12, Instruction Timing Chart

STR			
Time	I-Sequence	M-Sequence	W-Sequence
6.4	Clr: S, Z	Clr: S, Z	Clr: S, Z
1.1	P $\longrightarrow$ S	M $\longrightarrow$ S, Adder $\longrightarrow$ Z	Adder $\longrightarrow$ S
1.2	Clr: X, D Initiate Memory	Clr: X, D Initiate Memory	Clr: X Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D	$Z_{0-13} \longrightarrow$ X	A $\longrightarrow$ X
1.4		Clr: Z	
2.1		X $\longrightarrow$ D	X $\longrightarrow$ Z
2.2	Strobe Memory Clr: P	Strobe Memory	
2.3	Adder $\longrightarrow$ P		
3.2	Clr: X, D, F, M	Clr: X	Clr: D ⓓ
3.3	$Z_{0-13} \longrightarrow$ X, $Z_{14-18} \longrightarrow$ M, $Z_{19-23} \longrightarrow$ F, Clr: K_0	$Z_{0-13} \longrightarrow$ X	
4.1	If $Z_M = 37$, $X_{0-8} \longrightarrow$ D		
4.2	If $Z_M = 37$, Clr: X, M		
4.3	If $Z_M = 37$, B $\longrightarrow$ X, $Z_{9-13} \longrightarrow$ M		
5.4	Clr: I-Seq	Clr: M-Seq	Clr: W-Seq
6.1	If M = 0, Set: W-Seq If M $\neq$ 0, Set: M-Seq	Set: W-Seq	Set: NI or I/O-Seq

ⓓ Don't-Care Condition

TABLE 4-42. f = 13, Instruction Timing Chart

RPA			
Time	I-Sequence	M-Sequence	W-Sequence
6.4	Clr: S, Z	Clr: S, Z	Clr: S, Z
1.1	P $\longrightarrow$ S	M $\longrightarrow$ S Adder $\longrightarrow$ Z	Adder $\longrightarrow$ S
1.2	Clr: X, D Initiate Memory	Clr: X, D Initiate Memory	Clr: X Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D	$Z_{0-13} \longrightarrow$ X	A $\longrightarrow$ X
1.4		Clr: Z	
2.1		X $\longrightarrow$ D	$X_{0-13} \longrightarrow$ Z
2.2	Strobe Memory Clr: P	Strobe Memory	Strobe Memory (Upper 10)
2.3	Adder $\longrightarrow$ P		
3.2	Clr: X, D, F, M	Clr: X	Clr: D ⓓ
3.3	$Z_{0-13} \longrightarrow$ X, $Z_{14-18} \longrightarrow$ M, $Z_{19-23} \longrightarrow$ F, Clr: K_0	$Z_{0-13} \longrightarrow$ X	
4.1	If $Z_M = 37$, $X_{0-8} \longrightarrow$ D		
4.2	If $Z_M = 37$, Clr: X, M		
4.3	If $Z_M = 37$, B $\longrightarrow$ X, $Z_{9-13} \longrightarrow$ M		
5.4	Clr: I-Seq	Clr: M-Seq	Clr: W-Seq
6.1	If M = 0, Set: W-Seq If M $\neq$ 0, Set: M-Seq	Set: W-Seq	Set: NI or I/O-Seq

ⓓ Don't-Care Condition

TABLE 4-43. f = 14, Instruction Timing Chart

TRU		
Time	I-Sequence	M-Sequence
6.4	Clr: S, Z	Clr: S, Z
1.1	P $\longrightarrow$ S	M $\longrightarrow$ S, Adder $\longrightarrow$ Z
1.2	Clr: X, D Initiate Memory	Clr: X, D Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D	$Z_{0-13} \longrightarrow$ X
1.4		Clr: Z
2.1		X $\longrightarrow$ D
2.2	Strobe Memory Clr: P	Strobe Memory
2.3	Adder $\longrightarrow$ P	
3.2	Clr: X, D, F, M	Clr: X
3.3	$Z_{0-13} \longrightarrow$ X, $Z_{14-18} \longrightarrow$ M, $Z_{19-23} \longrightarrow$ F, Clr: K_0	$Z_{0-13} \longrightarrow$ X
4.1	If $Z_M = 37$, $X_{0-8} \longrightarrow$ D	
4.2	If $Z_M = 37$, Clr: X, M	
4.3	If $Z_M = 37$, B $\longrightarrow$ X, $Z_{9-13} \longrightarrow$ M	
5.4	Clr: I-Seq	Clr: M-Seq
6.1	If M = 0, Set: NI or I/O-Seq If M $\neq$ 0, Set: M-Seq	Set: NI or I/O-Seq
6.2	If M = 0, Clr: P	Clr: P
6.3	If M = 0, Adder $\longrightarrow$ P	Adder $\longrightarrow$ P

TABLE 4-44. f = 15, Instruction Timing Chart

TRA				
Time	I-Sequence		M-Sequence	
6.4	Clr: S, Z, Skip FF ①		Clr: S, Z	
1.1	P → S		M → S, Adder → Z	
1.2	Clr: X, D Initiate Memory		Clr: X, D Initiate Memory	
1.3	P → X, +1 → D		Z_{0-13} → X	
1.4			Clr: Z	
2.1			X → D	
2.2	Strobe Memory Clr: P		Strobe Memory	
2.3	Adder → P			
3.2	Clr: X, D, F, M		Clr: X	
3.3	Z_{0-13} → X, Z_{14-18} → M Z_{19-23} → F, Clr: K_0		Z_{0-13} → X	
4.1	If Z_M = 37, X_{0-8} → D			
4.2	If Z_M = 37, Clr: X, M			
4.3	If Z_M = 37, B → X, Z_{9-13} → M			
4.4	If A_{23} = 1, Set: Skip FF			
	If (A) = 0:	If (A) < 0 (A_{23} = 1):	If (A) > 0 (A_{23} = 0):	
5.2		Clr: X, D		
5.3		P → X, +1 → D		
5.4	Clr: I-Seq	Clr: I-Seq	Clr: I-Seq	Clr: M-Seq
6.1	Set: NI or I/O-Seq	Set: NI or I/O-Seq	If M = 0, Set: NI or I/O-Seq, If M ≠ 0, Set: M-Seq	Set: NI or I/O-Seq
6.2		Clr: P	If M = 0, Clr: P	Clr: P
6.3		Adder → P	If M = 0, Adder → P	Adder → P

① Skip FF cleared every T6.4 regardless of sequence type.

TABLE 4-45. f = 16, Instruction Timing Chart

TRD			
Time	I-Sequence		M-Sequence
6.4	Clr: S, Z		Clr: S, Z
1.1	P $\longrightarrow$ S		M $\longrightarrow$ S, Adder $\longrightarrow$ Z
1.2	Clr: X, D Initiate Memory		Clr: X, D Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D		$Z_{0-13} \longrightarrow X$
1.4			Clr: Z
2.1			X $\longrightarrow$ D
2.2	Strobe Memory Clr: P		Strobe Memory
2.3	Adder $\longrightarrow$ P		
3.2	Clr: X, D, F, M		Clr: X
3.3	$Z_{0-13} \longrightarrow X$, $Z_{14-18} \longrightarrow M$, $Z_{19-23} \longrightarrow F$, Clr: K_0		$Z_{0-13} \longrightarrow X$
4.1	If $Z_M = 37$, $X_{0-8} \longrightarrow D$		
4.2	If $Z_M = 37$, Clr: X, M		
4.3	If $Z_M = 37$, B $\longrightarrow$ X, $Z_{9-13} \longrightarrow M$		
	If $A_{23} = A_{24}$:	If $A_{23} \neq A_{24}$:	
5.4	Clr: I-Seq	Clr: I-Seq	Clr: M-Seq
6.1	Set: NI or I/O-Seq	If M = 0, Set: NI or I/O-Seq If M $\neq$ 0, Set: M-Seq	Set: NI or I/O-Seq
6.2		If M = 0, Clr: P	Clr: P
6.3		If M = 0, Adder $\longrightarrow$ P	Adder $\longrightarrow$ P

TABLE 4-46. f = 17, Instruction Timing Chart

SWC		
Time	I-Sequence	M-Sequence
6.4	Clr: S, Z	Clr: S, Z
1.1	P → S	M → S, Adder → Z
1.2	Clr: X, D Initiate Memory	Clr: X, D, M Initiate Memory
1.3	P → X, +1 → D	Z_{0-13} → X, Z_{9-13} → M ①
1.4		Clr: Z
2.1		X_{0-8} → D
2.2	Strobe Memory Clr: P	Strobe Memory
2.3	Adder → P	
3.2	Clr: X, D, F, M	Clr: X
3.3	Z_{0-13} → X, Z_{14-18} → M, Z_{19-23} → F, Clr: K_0	Z_{0-13} → X
4.1	If Z_M = 0 + 37, X_{0-8} → D	
4.2	If Z_M = 0 + 37, Clr: X, M	
4.3	If Z_M = 0 + 37, Z_{9-13} → M If Z_M = 37, B → X	
5.4	Clr: I-Seq	Clr: M-Seq
6.1	If Z_M = 0 + 37, Set: R-Seq If $Z_M \neq$ 0 + 37, Set: M-Seq	Set: R-Seq

① If M = 0, check bit 14 - 20 which is a word count of 177_8
If M ≠ 0, check bit 14 - 21 which is a word count of 377_8

TABLE 4-46. f = 17, Instruction Timing Chart (continued)

SWC		
Time	R-Sequence	
6.4	Clr: S, Z, Skip FF	
1.1	Adder $\longrightarrow$ S	
1.2	Initiate Memory	
2.2	Strobe Memory	
3.2	Clr: X Clr: D ⓓ	
3.3	Z $\longrightarrow$ X	
	If Z_{WC} ① $\neq$ 0:	If Z_{WC} ① = 0:
4.4		Set: Skip FF
5.2		Clr: X, D
5.3		P $\longrightarrow$ X, +1 $\longrightarrow$ D
5.4	Clr: R-Seq	Clr: R-Seq
6.1	Set: NI or I/O-Seq	Set: NI or I/O-Seq
6.2		Clr: P
6.3		Adder $\longrightarrow$ P

① If M = 0, check bit 14 - 20 which is a word count of 177_8
If M $\neq$ 0, check bit 14 - 20 which is a word count of 377_8
ⓓ Don't-Care Condition

TABLE 4-47. f = 20, Instruction Timing Chart

EXC		
Time	I-Sequence	M-Sequence
6.4	Clr: S, Z	Clr: S, Z
1.1	P → S	M → S, Adder → Z
1.2	Clr: X, D Initiate Memory	Clr: X, D Initiate Memory
1.3	P → X, +1 → D	Z_{0-13} → X
1.4		Clr: Z
2.1		X → D
2.2	Strobe Memory Clr: P	Strobe Memory
2.3	Adder → P	
3.2	Clr: X, D, F, M	Clr: X
3.3	Z_{0-13} → X, Z_{14-18} → M, Z_{19-23} → F, Clr: K_0	Z_{0-13} → X
4.1	If Z_M = 37, X_{0-8} → D	
4.2	If Z_M = 37, Clr: X, M	
4.3	If Z_M = 37, B → X, Z_{9-13} → M	
5.4	Clr: I-Seq	Clr: M-Seq
6.1	If M = 0, Set: R-Seq If M ≠ 0, Set: M-Seq	Set: R-Seq

TABLE 4-47. f = 20, Instruction Timing Chart (continued)

EXC		
Time	R-Sequence	W-Sequence
6.4	Clr: S, Z	Clr: Z
1.1	Adder $\longrightarrow$ S	
1.2	Initiate Memory	Initiate Memory
2.1		X $\longrightarrow$ Z
2.2	Strobe Memory	
3.2	Clr: X, D Initiate Arithmetic Timing Chain	Clr: D (d)
3.3	Z $\longrightarrow$ X	
4.1	$\overline{X}$ $\longrightarrow$ D (1)	
4.2	Clr: X (1)	
4.3	A $\longrightarrow$ X (1)	
4.4	Clr: A (1)	
5.1	$\overline{D}$ $\longrightarrow$ A (1)	
5.4	Clr: R-Seq	Clr: W-Seq
6.1	Set: W-Seq	Set: NI or I/O-Seq

(1) Enabled By Arithmetic Timing Chain
(d) Don't-Care Condition

TABLE 4-48. f = 21, Instruction Timing Chart

ADC			
Time	I-Sequence	R-Sequence	W-Sequence
6.4	Clr: S, Z	Clr: S, Z	Clr: Z
1.1	P $\longrightarrow$ S	Adder $\longrightarrow$ S	Adder $\longrightarrow$ Z
1.2	Clr: X, D Initiate Memory	Initiate Memory	Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D		
2.2	Strobe Memory Clr: P	Strobe Memory	
2.3	Adder $\longrightarrow$ P		
3.2	Clr: X, D, F, M	Clr: X, D	Clr: D (d)
3.3	$Z_{0-13} \longrightarrow$ X, $Z_{14-18} \longrightarrow$ M, $Z_{19-23} \longrightarrow$ F, Clr: K_0	Z $\longrightarrow$ X M $\longrightarrow D_{0-4}$ (1)	
5.4	Clr: I-Seq	Clr: R-Seq	Clr: W-Seq
6.1	Set: R-Seq	Set: W-Seq	Set: NI or I/O-Seq

(1) The Constant C: $0 \leq C \leq 37_8$
(d) Don't-Care Condition

TABLE 4-49. f = 22, Instruction Timing Chart

ADO		
Time	I-Sequence	M-Sequence
6.4	Clr: S, Z	Clr: X, Z
1.1	P $\longrightarrow$ S	M $\longrightarrow$ S, Adder $\longrightarrow$ Z
1.2	Clr: X, D Initiate Memory	Clr: X, D Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D	$Z_{0-13} \longrightarrow X$
1.4		Clr: Z
2.1		X $\longrightarrow$ D
2.2	Strobe Memory Clr: P	Strobe Memory
2.3	Adder $\longrightarrow$ P	
3.2	Clr: X, D, F, M	Clr: X
3.3	$Z_{0-13} \longrightarrow X$, $Z_{14-18} \longrightarrow M$, $Z_{19-23} \longrightarrow F$, Clr: K_0	$Z_{0-13} \longrightarrow X$
4.1	If $Z_M = 37$, $X_{0-8} \longrightarrow D$	
4.2	If $Z_M = 37$, Clr: X, M	
4.3	If $Z_M = 37$, B $\longrightarrow$ X, $Z_{9-13} \longrightarrow M$	
5.4	Clr: I-Seq	Clr: M-Seq
6.1	If M = 0, Set: R-Seq If M $\neq$ 0, Set: R-Seq	Set: R-Seq

TABLE 4-49. f = 22, Instruction Timing Chart (continued)

ADO		
Time	R-Sequence	W-Sequence
6.4	Clr: S, Z	Clr: Z
1.1	Adder ⟶ S	Adder ⟶ Z
1.2	Initiate Memory	Initiate Memory
2.2	Strobe Memory	
3.2	Clr: X, D	Clr: D ⓓ
3.3	Z ⟶ X, +1 ⟶ D	
5.4	Clr: R-Seq	Clr: W-Seq
6.1	Set: W-Seq	Set: NI or I/O-Seq

ⓓ Don't-Care Condition

TABLE 4-50. f = 23, Instruction Timing Chart

AID			
Time	I-Sequence		M-Sequence
6.4	Clr: S, Z		Clr: S, Z
1.1	P $\longrightarrow$ S		M $\longrightarrow$ S, Adder $\longrightarrow$ Z
1.2	Clr: X, D Initiate Memory		Clr: X, D Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D		$Z_{0-13} \longrightarrow X$
1.4			Clr: Z
2.1			X $\longrightarrow$ D
2.2	Strobe Memory Clr: P		Strobe Memory
2.3	Adder $\longrightarrow$ P		
3.2	Clr: X, D, F, M		Clr: X
3.3	$Z_{0-13} \longrightarrow X$, $Z_{14-18} \longrightarrow M$, $Z_{19-23} \longrightarrow F$, Clr: K_0		$Z_{0-13} \longrightarrow X$
4.1	If $Z_M = 37$, $X_{0-8} \longrightarrow D$		
4.2	If $Z_M = 37$, Clr: X, M		
4.3	If $Z_M = 37$, B $\longrightarrow$ X, $Z_{9-13} \longrightarrow M$		
5.4	Clr: I-Seq		Clr: M-Seq
6.1	If $A_{23} \neq A_{24}$	If $A_{23} = A_{24}$	Set: R-Seq
	M = 0, Set: R-Seq M $\neq$ 0, Set: M-Seq	Set: NI or I/O-Seq	

TABLE 4-50. f = 23, Instruction Timing Chart (continued)

AID		
Time	R-Sequence	W-Sequence
6.4	Clr: S, Z	Clr: Z
1.1	Adder → S	Adder → Z
1.2	Initiate Memory	Initiate Memory
2.2	Strobe Memory	
3.2	Clr: X, D	Clr: D ⓓ
3.3	Z → X, +1 → D	
5.4	Clr: R-Seq	Clr: W-Seq
6.1	Set: W-Seq	Set: NI or I/O-Seq

ⓓ Don't-Care Condition

TABLE 4-51. f =24, Instruction Timing Chart

RCA		
Time	I-Sequence	M-Sequence
6.4	Clr: S, Z	Clr: S, Z
1.1	P $\longrightarrow$ S	M $\longrightarrow$ S, Adder $\longrightarrow$ Z
1.2	Clr: X, D Initiate Memory	Clr: X, D Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D	$Z_{0 - 13} \longrightarrow$ X
1.4		Clr: Z
2.1		X $\longrightarrow$ D
2.2	Strobe Memory Clr: P	Strobe Memory
2.3	Adder $\longrightarrow$ P	
3.2	Clr: X, D, F, M	Clr: X
3.3	$Z_{0 - 13} \longrightarrow$ X, $Z_{14 - 18} \longrightarrow$ M, $Z_{19 - 23} \longrightarrow$ F, Clr: K_0	$Z_{0 - 13} \longrightarrow$ X
4.1	If $Z_M = 37$, $X_{0 - 8} \longrightarrow$ D	
4.2	If $Z_M = 37$, Clr: X, M	
4.3	If $Z_M = 37$, B $\longrightarrow$ X, $Z_{9 - 13} \longrightarrow$ M	
5.3	Set: RCA FF	Set: RCA FF
5.4	Clr: I-Seq	Clr: M-Seq
6.1	If M = 0, Set: R-Seq If M $\neq$ 0, Set: M-Seq	Set: R-Seq

TABLE 4-51. f = 24, Instruction Timing Chart (continued)

RCA		
Time	R-Sequence	W-Sequence
6.4	Clr: S, Z	Clr: S 40 → S
1.1	Adder → S	
1.2	Initiate Memory	Initiate Memory
2.2	Strobe Memory	
3.2	Clr: X, D ⓓ	
3.3	Z → X ⓓ	
5.3	Set: RCA FF	Set: RCA FF
5.4	Clr: R-Seq	Clr: W-Seq
6.1	Set: W-Seq	Set: NI or I/O-Seq

ⓓ Don't-Care Condition

TABLE 4-52. f = 25, Instruction Timing Chart

ERC		
Time	I-Sequence	M-Sequence
6.4	Clr: S, Z	Clr: S, Z
1.1	P $\longrightarrow$ S	M $\longrightarrow$ S, Adder $\longrightarrow$ Z
1.2	Clr: X, D Initiate Memory	Clr: X, D Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D	$Z_{0-13} \longrightarrow X$
1.4		Clr: Z
2.1		X $\longrightarrow$ D
2.2	Strobe Memory Clr: P	Strobe Memory
2.3	Adder $\longrightarrow$ P	
3.2	Clr: X, D, F, M	Clr: X
3.3	$Z_{0-13} \longrightarrow X$, $Z_{14-18} \longrightarrow M$, $Z_{19-23} \longrightarrow F$, Clr: K_0	$Z_{0-13} \longrightarrow X$
4.1	If $Z_M = 37$, $X_{0-8} \longrightarrow D$	
4.2	If $Z_M = 37$, Clr: X, M	
4.3	If $Z_M = 37$, B $\longrightarrow$ X, $Z_{9-13} \longrightarrow M$	
5.3	Clr: RCA FF	Clr: RCA FF
5.4	Clr: I-Seq	Clr: M-Seq
6.1	If M = 0, Set: R-Seq If M $\neq$ 0, Set: M-Seq	Set: R-Seq

TABLE 4-52. f = 25, Instruction Timing Chart (continued)

ERC		
Time	R-Sequence	W-Sequence
6.4	Clr: S, Z, 40 → S	Clr: S
1.1		Adder → S
1.2	Initiate Memory	Initiate Memory
2.2	Strobe Memory	
3.2		Clr: D ⓓ
5.3	Clr: RCA FF	Clr: RCA FF
5.4	Clr: R-Seq	Clr: W-Seq
6.1	Set: W-Seq	Set: NI or I/O-Seq

ⓓ Don't-Care Condition

TABLE 4-53. f = 26, Instruction Timing Chart

STX, SRC		
Time	I-Sequence	M-Sequence
6.4	Clr: S, Z	Clr: S, Z
1.1	P $\longrightarrow$ S	M $\longrightarrow$ S, Adder $\longrightarrow$ Z
1.2	Clr: X, D Initiate Memory	Clr: X, D, M Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D	$Z_{0-13} \longrightarrow$ X, $Z_{9-13} \longrightarrow$ M
1.4		Clr: Z
2.1		$X_{0-8} \longrightarrow$ D
2.2	Strobe Memory Clr: P	Strobe Memory
2.3	Adder $\longrightarrow$ P	
3.2	Clr: X, D, F, M	Clr: X
3.3	$Z_{0-13} \longrightarrow$ X, $Z_{14-18} \longrightarrow$ M, $Z_{19-23} \longrightarrow$ F, Clr: K_0	$Z_{0-13} \longrightarrow$ X
4.1	If $Z_M = 0 + 37$, $X_{0-8} \longrightarrow$ D	
4.2	If $Z_M = 0 + 37$, Clr: X, M	
4.3	If $Z_M = 0 + 37$, $Z_{9-13} \longrightarrow$ M If $Z_M = 37$, B $\longrightarrow$ X	
5.4	Clr: I-Seq	Clr: M-Seq
6.1	If $Z_M = 0 + 37$, Set: R-Seq If $Z_M = 0 + 37$, Set: M-Seq	Set: R-Seq

TABLE 4-53. f = 26, Instruction Timing Chart (continued)

STX, SRC		
Time	R-Sequence	W-Sequence
6.4	Clr: S, Z	Clr: S If M = 0, Clr: Z
1.1	M $\longrightarrow$ S	Adder $\longrightarrow$ S If M = 0, $RC_0 \longrightarrow Z_{0-4}$
1.2	Initiate Memory	Initiate Memory
2.2	Strobe Memory	
3.2		Clr: D ⓓ
5.4	Clr: R-Seq	Clr: W-Seq
6.1	Set: W-Seq	Set: NI or I/O-Seq

ⓓ Don't-Care Condition

TABLE 4-54. f = 27, Instruction Timing Chart

LDX, LRC		
Time	I-Sequence	M-Sequence
6.4	Clr: S, Z	Clr: S, Z
1.1	P $\longrightarrow$ S	M $\longrightarrow$ S, Adder $\longrightarrow$ Z
1.2	Clr: X, D Initiate Memory	Clr: X, D, M Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D	$Z_{0-13} \longrightarrow X$, $Z_{9-13} \longrightarrow M$
1.4		Clr: Z
2.1		$X_{0-8} \longrightarrow D$
2.2	Strobe Memory Clr: P	Strobe Memory
2.3	Adder $\longrightarrow$ P	
3.2	Clr: X, D, F, M	Clr: X
3.3	$Z_{0-13} \longrightarrow X$, $Z_{14-18} \longrightarrow M$, $Z_{19-23} \longrightarrow F$, Clr: K_0	$Z_{0-13} \longrightarrow X$
4.1	If $Z_M = 0 + 37$, $X_{0-8} \longrightarrow D$	
4.2	If $Z_M = 0 + 37$, Clr: X, M	
4.3	If $Z_M = 0 + 37$, $Z_{9-13} \longrightarrow M$ If $Z_M = 37$, B $\longrightarrow$ X	
5.4	Clr: I-Seq	Clr: M-Seq
6.1	If $Z_M = 0 + 37$, Set: R-Seq If $Z_M = 0 + 37$, Set: M-Seq	Set: R-Seq

TABLE 4-54. f = 27, Instruction Timing Chart (continued)

LDX, LRC		
Time	R-Sequence	W-Sequence
6.4	Clr: S, Z	Clr: S
1.1	Adder $\longrightarrow$ S	M $\longrightarrow$ S ①
1.2	Initiate Memory	Initiate Memory
2.2	Strobe Memory	
3.2	Clr: X, D	
3.3	$Z_{0-13} \longrightarrow X$	
4.3	If M = 0, Clr: RC_0	
4.4	If M = 0, $Z_{0-4} \longrightarrow RC_0$	
5.4	Clr: R-Seq	Clr: W-Seq
6.1	If M = 0, Set: NI or I/O-Seq If M $\neq$ 0, Set: W-Seq	Set: NI or I/O-Seq
6.2	If M = 37, Clr: B	
6.3	If M = 37, Adder $\longrightarrow$ B	

① If M = 37, IDX 37 and B-register will be loaded
If M = 0, RC_0 will be loaded

TABLE 4-55. f = 30, Instruction Timing Chart

CLA			
Time	I-Sequence	M-Sequence	R-Sequence
6.4	Clr: S, Z	Clr: S, Z	Clr: S, Z
1.1	P $\longrightarrow$ S	M $\longrightarrow$ S Adder $\longrightarrow$ S	Adder $\longrightarrow$ S
1.2	Clr: X, D	Clr: X, D Initiate Memory	Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D	$Z_{0-13} \longrightarrow$ X	
1.4		Clr: Z	
2.1		X $\longrightarrow$ D	
2.2	Strobe Memory Clr: P	Strobe Memory	Strobe Memory
2.3	Adder $\longrightarrow$ P		
3.2	Clr: X, D, F, M	Clr: X	Clr: X, D Initiate Arithmetic Timing Chain
3.3	$Z_{0-13} \rightarrow$ X, $Z_{14-18} \rightarrow$ M, $Z_{19-23} \rightarrow$ F, Clr: K_0	$Z_{0-13} \longrightarrow$ X	Z $\longrightarrow$ X
4.1	If $Z_M = 37$, $X_{0-8} \longrightarrow$ D		X $\longrightarrow$ D (1)
4.2	If $Z_M = 37$, Clr: X, M		Clr: X (1)
4.3	If $Z_M = 37$, B $\longrightarrow$ X, $Z_{9-13} \longrightarrow$ M		A $\longrightarrow$ X (1)
4.4			Clr: A (1)
5.1			D $\longrightarrow$ A (1)
5.4	Clr: I-Seq	Clr: M-Seq	Clr: R-Seq
6.1	If M = 0, Set: R-Seq If M $\neq$ 0, Set: M-Seq	Set: R-Seq	Set: NI or I/O-Seq

(1) Enabled By Arithmetic Timing Chain

TABLE 4-56. f = 31, Instruction Timing Chart

ADD			
Time	I-Sequence	M-Sequence	R-Sequence
6.4	Clr: S, Z	Clr: S, Z	Clr: S, Z
1.1	P → S	M → S, Adder → Z	Adder → S
1.2	Clr: X, D Initiate Memory	Clr: X, D Initiate Memory	Initiate Memory
1.3	P → X, +1 → D	Z_{0-13} → X	
1.4		Clr: Z	
2.1		X → D	
2.2	Strobe Memory Clr: P	Strobe Memory	Strobe Memory
2.3	Adder → P		
3.2	Clr: X, D, M, M	Clr: X	Clr: X, D Initiate Arithmetic Timing Chain
3.3	Z_{0-13} → X, Z_{14-18} → M, Z_{19-23} → F, Clr: K_0	Z_{0-13} → X	Z → X
4.1	If Z_M = 37, X_{0-8} → D		X → D ①
4.2	If Z_M = 37, CLR: X, M		Clr: X ①
4.3	If Z_M = 37, B → X, Z_{9-13} → M		A → X ①
4.4			Clr: A ①
5.4	Clr: I-Seq	Clr: M-Seq	Clr: R-Seq
6.1	If M = 0, Set: R-Seq If M ≠ 0, Set: M-Seq	Set: R-Seq	Set: NI or I/O-Seq Adder → A

① Enabled By Arithmetic Timing Chain

TABLE 4-57. f = 32, Instruction Timing Chart

SUB Time	I-Sequence	M-Sequence	R-Sequence
6.4	Clr: S, Z	Clr: S, Z	Clr: S, Z
1.1	P $\longrightarrow$ S	M $\longrightarrow$ S Adder $\longrightarrow$ Z	Adder $\longrightarrow$ S
1.2	Clr: X, D Initiate Memory	Clr: X, D Initiate Memory	InitiateMemory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D	$Z_{0-13} \longrightarrow$ X	
1.4		Clr: Z	
2.1		X $\longrightarrow$ D	
2.2	Strobe Memory Clr: P	Strobe Memory	Strobe Memory
2.3	Adder $\longrightarrow$ P		
3.2	Clr: X, D, F, M	Clr: X	Clr: X, D Initiate Arithmetic Timing Chain
3.3	$Z_{0-13} \longrightarrow$ X, $Z_{14-18} \longrightarrow$ M, $Z_{19-23} \longrightarrow$ F, Clr: K_0	$Z_{0-13} \longrightarrow$ X	Z $\longrightarrow$ X
4.1	If $Z_M = 37$, $X_{0-8} \longrightarrow$ D		$\overline{X} \longrightarrow$ D ①
4.2	If $Z_M = 37$, Clr: X, M		Clr: X ①
4.3	If $Z_M = 37$, B $\longrightarrow$ X $Z_{9-13} \longrightarrow$ M		A $\longrightarrow$ X ①
4.4			Clr: A 1
5.4	Clr: I-Seq	Clr: M-Seq	Clr: R-Seq
6.1	If M = 0, Set: R-Seq If M $\neq$ 0, Set: M-Seq	Set: R-Seq	Set: NI or I/O-Seq Adder $\longrightarrow$ A

① Enabled By Arithmetic Timing Chain

TABLE 4-58. f = 33, Instruction Timing Chart

COM		
Time	I-Sequence	M-Sequence
6.4	Clr: S, Z	Clr: S, Z
1.1	P $\longrightarrow$S	M $\longrightarrow$ S, Adder $\longrightarrow$ Z
1.2	Clr: X, D Initiate Memory	Clr: X, D Initiate Memory
1.3	P $\longrightarrow$X, +1 $\longrightarrow$ D	$Z_{0 - 13} \longrightarrow X$
1.4		Clr: Z
2.1		X $\longrightarrow$ D
2.2	Strobe Memory Clr: P	Strobe Memory
2.3	Adder $\longrightarrow$ P	
3.2	Clr: X, D, F, M	Clr: X
3.3	$Z_{0 - 13} \longrightarrow X$, $Z_{14 - 18} \longrightarrow M$, $Z_{19 - 23} \longrightarrow F$, Clr: K_0	$Z_{0 - 13} \longrightarrow X$
4.1	If $Z_M = 37$, $X_{0 - 8} \longrightarrow D$	
4.2	If $Z_M = 37$, Clr: X, M	
4.3	If $Z_M = 37$, B $\longrightarrow$X	
	$Z_{9 - 13} \longrightarrow M$	
5.4	Clr: I-Seq	Clr: M-Seq
6.1	If M = 0, Set: R-Seq If M $\neq$ 0, Set: M-Seq	Set: R-Seq

TABLE 4-58. f = 33, Instruction Timing Chart (continued)

COM			
Time	R-Sequence		
6.4	Clr: S, Z, Skip FF, Adder Equal FF ①		
1.1	Adder $\longrightarrow$ S		
1.2	Initiate Memory		
2.2	Strobe Memory		
3.2	Clr: X, D		
3.3	Z $\longrightarrow$ X		
4.1	$\overline{A} \longrightarrow D$		
	If: (A) > (Y) ie, $(\overline{D})$ > (X) (Signs = and EAB) (Signs $\neq$ and $\overline{EAB}$)	If: (A) < (Y) ie, $(\overline{D})$ < (X) (Signs = and $\overline{EAB}$) (Signs $\neq$ and EAB)	If: (A) = (Y) ie, $(\overline{D})$ = (X) (Signs = and $\overline{EAB}$)
4.4		Set: Skip FF	Set: Skip FF, Adder Equal FF
5.2		Clr: X, D	Clr: X, D
5.3		P $\longrightarrow$ X, +1 $\longrightarrow$ D	P $\longrightarrow$ X, +2 $\longrightarrow$ D
5.4	Clr: R-Seq	Clr: R-Seq	Clr: R-Seq
6.1	Set: NI or I/O-Seq	Set: NI or I/O-Seq	Set: NI or I/O-Seq
6.2		Clr: P	Clr: P
6.3		Adder $\longrightarrow$ P	Adder $\longrightarrow$ P

① Skip and Adder Equal FF's cleared every T6.4 regardless of sequence type

TABLE 4-59. f = 34, Instruction Timing Chart

LGA			
Time	I-Sequence	M-Sequence	R-Sequence
6.4	Clr: S, Z	Clr: S, Z	Clr: S, Z
1.1	P $\longrightarrow$ S	M $\longrightarrow$ S Adder $\longrightarrow$ Z	Adder $\longrightarrow$ S
1.2	Clr: X, D Initiate Memory	Clr: X, D Initiate Memory	Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D	$Z_{0-13} \longrightarrow$ X	
1.4		Clr: Z	
2.1		X $\longrightarrow$ D	
2.2	Strobe Memory Clr: P	Strobe Memory	Strobe Memory
2.3	Adder $\longrightarrow$ P		
3.2	Clr: X, D, F, M	Clr: X	Clr: X, D, Initiate Arithmetic Timing Chain
3.3	$Z_{0-13} \longrightarrow$ X, $Z_{14-18} \longrightarrow$ M, $Z_{19-23} \longrightarrow$ F, Clr: K_0	$Z_{0-13} \longrightarrow$ X	Z $\longrightarrow$ X
4.1	If Z_M = 37, $X_{0-8} \longrightarrow$ D		X $\longrightarrow$ D ①
4.2	If Z_M = 37, Clr: X, M		Clr: X ①
4.3	If Z_M = 37, B $\longrightarrow$ X, $Z_{9-13} \longrightarrow$ M		A $\longrightarrow$ X ①
4.4			Clr: A ①
5.1			X $\oplus$ D $\longrightarrow$ A ①
5.4	Clr: I-Seq	Clr: M-Seq	Clr: R-Seq

① Enabled By Arithmetic Timing Chain

TABLE 4-59. f = 34, Instruction Timing Chart (continued)

LGA			
Time	I-Sequence	M-Sequence	R-Sequence
6.1	If M = 0, Set: R-Seq If M ≠ 0, Set: M-Seq	Set: R-Seq	Set: NI or I/O-Seq

TABLE 4-60. f = 35, Instruction Timing Chart

LGM			
Time	I-Sequence	M-Sequence	R-Sequence
6.4	Clr: S, Z	Clr: S, Z	Clr: S,Z
1.1	P $\longrightarrow$ S	M $\longrightarrow$ S Adder $\longrightarrow$ Z	Adder $\longrightarrow$ S
1.2	Clr: X, D Initiate Memory	Clr: X, D Initiate Memory	Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D	$Z_{0-13} \longrightarrow$ X	
1.4		Clr: Z	
2.1		X $\longrightarrow$ D	
2.2	Strobe Memory Clr: P	Strobe Memory	Strobe Memory
2.3	Adder $\longrightarrow$ P		
3.2	Clr: X, D, F, M	Clr: X	Clr: X, D Initiate Arithmetic Timing Chain
3.3	$Z_{0-13} \longrightarrow$ X, $Z_{14-18} \longrightarrow$ M, $Z_{19-23} \longrightarrow$ F, Clr: K_0	$Z_{0-13} \longrightarrow$ X	Z $\longrightarrow$ X
4.1	If $Z_M = 37$, $X_{0-8} \longrightarrow$ D		$\bar{X} \longrightarrow$ D ① $\bar{A} \longrightarrow$ D
4.2	If $Z_M = 37$, Clr: X, M		Clr: X ①
4.3	If $Z_M = 37$, B $\longrightarrow$ X, $Z_{9-13} \longrightarrow$ M		A $\longrightarrow$ X ①
4.4			Clr: A ①
5.1			$\bar{D} \longrightarrow$ A ①
5.4	Clr: I-Seq	Clr: M-Seq	Clr: R-Seq
6.1	If M = 0, Set: R-Seq If M $\neq$ 0, Set: M-Seq	Set: R-Seq	Set: NI or I/O-Seq

① Enabled By Arithmetic Timing Chain

TABLE 4-61. f = 36, Instruction Timing Chart

ADB	
Time	I-Sequence
6.4	Clr: S, Z
1.1	P $\longrightarrow$ S
1.2	Clr: X, D Initiate Memory
1.3	P $\longrightarrow$ X, +1 $\longrightarrow$ D
2.2	Strobe Memory Clr: P
2.3	Adder $\longrightarrow$ P
3.2	Clr: X, D, F, M Initiate Arithmetic Timing Chain
3.3	$Z_{0-13} \longrightarrow X$, $Z_{14-18} \longrightarrow M$, $Z_{19-23} \longrightarrow F$ Clr: K_0
4.2	Clr: X (1)
4.3	A $\longrightarrow$ X (1) , B $\longrightarrow$ D (1)
4.4	Clr: A (1)
5.4	Clr: I-Seq
6.1	Set: NI or I/O-Seq Adder $\longrightarrow$ A.
6.2	Clr: B
6.3	Adder $\longrightarrow$ B

(1) Enabled By Arithmetic Timing Chain

TABLE 4-62. Interrupt Sequences, Instruction Timing Chart

Time	RC1-Sequence	WC-Sequence	RCI_N-Sequence
6.4	Clr: S, Z	Clr: S, Z	Clr: S, Z
1.1	42 → S	42 → S Adder → Z	43 → S
1.2	Initiate Memory	Initiate Memory	Initiate Memory Clr: X, INT ARM FF
1.3		Clr: Appropriate Request-One-Shot FF's	P → X Clr: Appropriate Request-One-Shot FF's
2.1			$X_{0 - 13}$ → Z
2.2	Strobe Memory		Clr: P Strobe Memory (Upper 10)
2.3			D → P
3.2	Clr: X, D		Clr: D (d)
3.3	Z → X		
4.3	If $Z_{14 - 23} \neq 0$, Set: $D_{14 - 23}$, Force Borrow Enable FF (1)		
5.1	If $Z_{14 - 23} = 0$, X → D		
5.4	Clr: RC1-Seq	Clr: WC-Seq	Clr: RCI_N-Seq
6.1	If $Z_{14 - 23}, \neq 0$, Set: WC-Seq, If $Z_{14 - 23} = 0$, Set RCI_N-Seq	Set: NI or I/O-Seq	Set: NI or I/O-Seq

(d) Don't-Care Condition
(1) Forced End-Around Borrow (WC-1, Y not changed)

V - FUNCTIONAL SYMBOLS AND TERMS

4-22. LOGIC SYMBOLOGY. - The CP-818A/U Digital Data Computer contains many similar types of transistor circuits. These circuits are mounted on printed circuit cards that are identified by an 0N number. The cards plug into chassis jacks that are arranged in a grid coordinate system on each chassis. The chassis map shows the correct card type for each jack.

The logic diagrams in Volume II contain symbols representing the various logic functions performed by the circuits. The shape of the symbol identifies the logic function. Information inside the symbol identifies the circuit type and location. Information outside the symbol gives wiring information and operating characteristics. The wiring information corresponds to that in the wire tabulations in Chapter 9, Volume III. Page xvii of Volume II also contains logic symbology diagrams.

a. Tagging Lines. - The three tagging lines inside the logic symbol serve the following purposes (see figure 4-81).

The top tagging line is a unique circuit identifier term. In all symbols except flip-flops, it consists of two digits, a letter, and two more digits. In flip-flop terms, the second digit is an X. The first two digits generally identify similar circuits. The letter identifies a functional group of circuits (see table 4-63, page 4-239). The last two digits generally indicate the circuit level. For example, the 93V02 term drives the 93V03 term.

The second tagging line is the 0N card type number.

The third tagging line is the chassis location of the card. The first digit is the logic chassis number. J designates a jack, and the following digits and letter designate the horizontal and vertical coordinates of the jack.

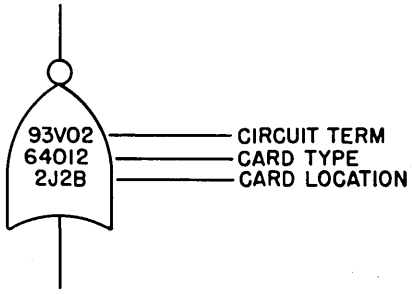


Figure 4-81. Tagging Lines

TABLE 4-63. Circuit Identifier Cross Reference

Letter	Circuit
A	A-Register, Adder, A_{24}
B	B-Register, and Bootstrap Memory
C	C-Register, Master Clock and Distribution
D	D-Register
E	Unassigned
F	F-Register, Function Coding, Halt Circuits
G	Unassigned
H	Unassigned
I	Data Input, Address Input
J	Console Control, Phase Step
K	Shift (K) Register, Repeat Count Register
L	Memory Control, Advance P, Timing Chain, Low Speed Osc
M	M-Register, Status Circuits
N	Command Enables
O	Acknowledge Circuits
P	P-Register
Q	Unassigned
R	Shift Control
S	S-Register
T	Main and Arithmetic Timing Chain, Sequence Circuits
U	Memory Voltage Regulator and Sensors
V	Command Enables (I/O), Fault Indicator Control Circuits
W	Intercomputer Circuits
X	X-Register
Y	Input Amplifiers, Output Amplifiers
Z	Z-Register, Selector, Parity

b. Signal Line Information. - The information on the input and output signal lines cross references the logic diagrams (see figure 4-82). When the source of destination term is a flip-flop, a -1 or -0 added to the circuit term designates the set or clear side. The signal name below the line (input or output) describes the active state of the signal. The H (high, 0v) or L (low, -4.5v) in the signal name denotes the logic level of the active state. A small circle on a symbol input indicates the line must be a logic low (-4.5v) to activate the circuit. No circle indicates the line must be a logic high. A circle on the symbol output indicates the line is a logic low (-4.5v) when the circuit activated; no circle indicates a logic high (0v) when activated (see figure 4-83).

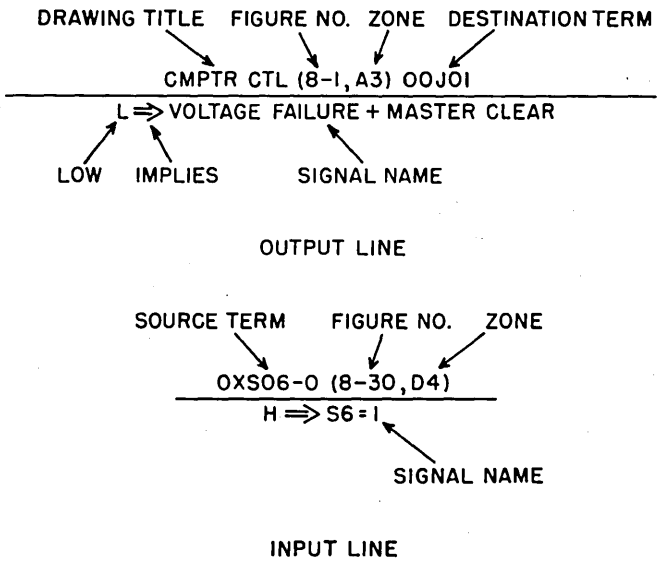


Figure 4-82. Signal Lines

Figure 4-83. Logic States

c. Connector And Test Point Information. - A connector shown on the logic diagrams is accompanied by all its location information (see figure 4-84). The number in front of the P is the chassis number. The J and following number represent the matching jack of the given plug number. The movable portion of a connector is defined as the plug; the stationary part as the jack. The number in the connector symbol is the pin number within the connector. The dashed line between signal lines indicates the lines are in the same connector. The test point shown in figure 4-84 is on a logic chassis. The memory chassis differ only in that there is no test block number.

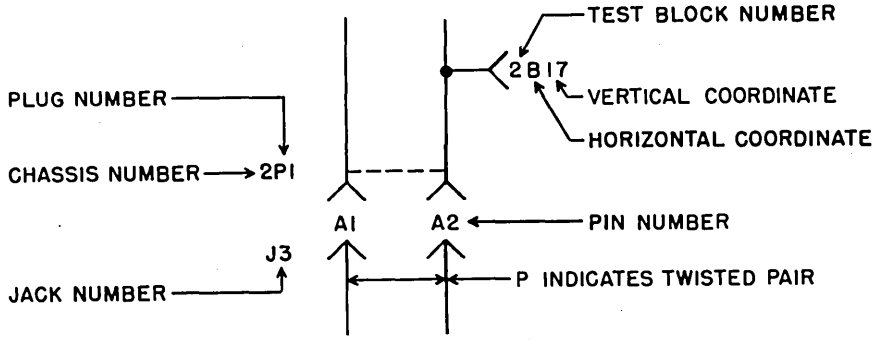


Figure 4-84. Connector and Test Point Locations

d. Indicator Switch. - The panel indicator switches are shown as a rectangle on the logic diagrams. The indicator displays the state of the driving circuit, in most cases a flip-flop, and the switch provides a means of setting the flip-flop or activating the driving circuit. Figure 4-35 shows a schematic of the indicator switch module. The logic signal connects to pin 5, pin 3 or 4 connects to ground, and pin 1 or 6 to the +15v indicator supply. The incandescent bulb can be replaced by removing the lens from the front. Connections to module are via wire wrap to pins on the back of the module.

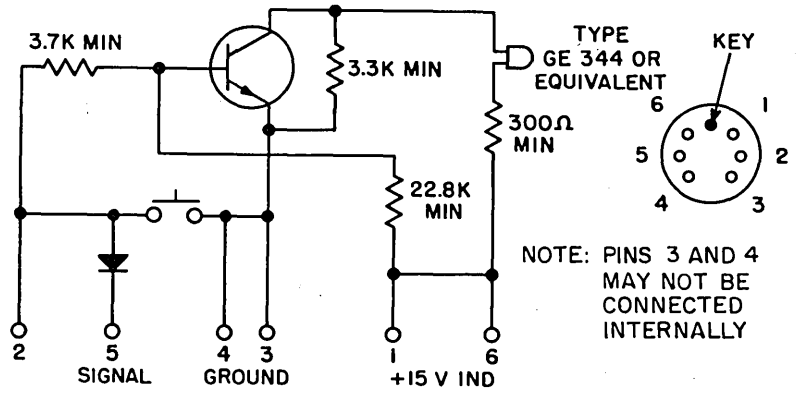


Figure 4-85. Indicator-Switch Module

4-23. CHASSIS MAPS (figures 8-104 through 8-108, pages 8-223 through 8-231). - A chassis map shows card side view of the location of each card on the chassis and the circuit terms of each card (see figure 4-86). The card can contain from one to five circuit terms depending on the card type. An unused circuit on a card is shown by five dashes.

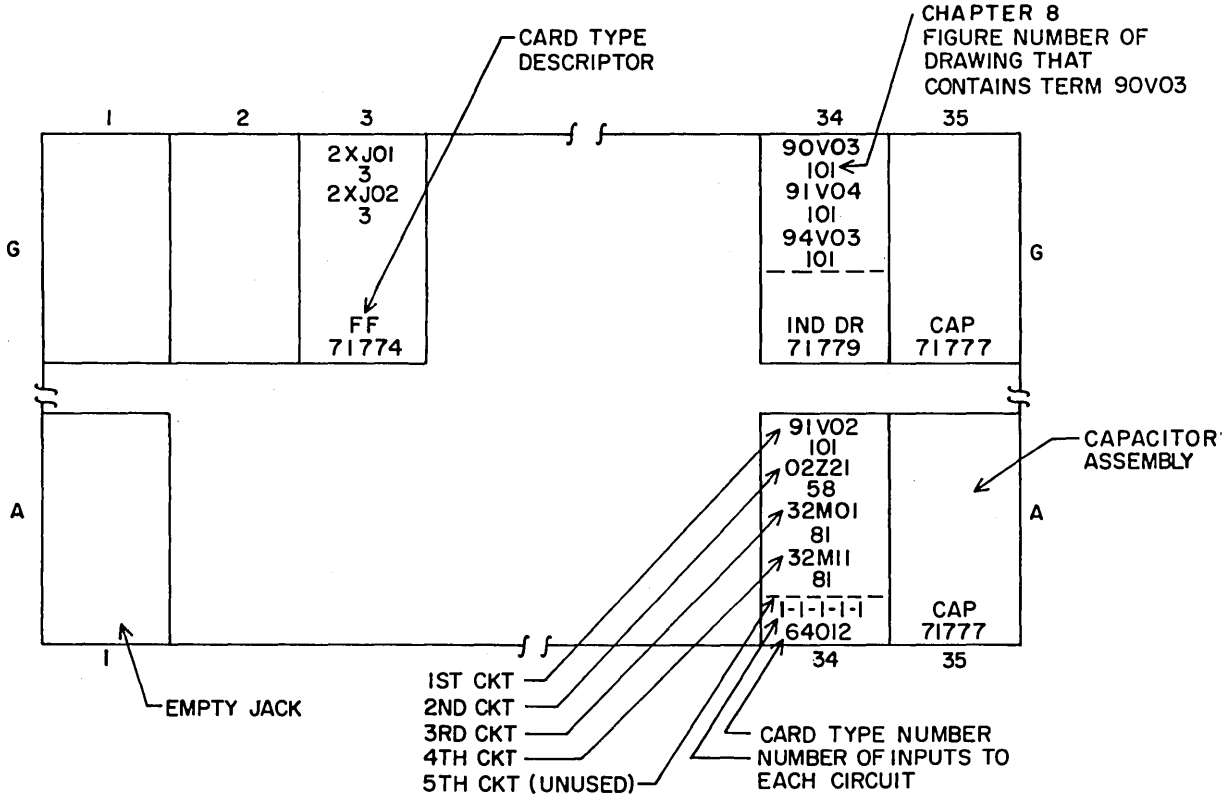


Figure 4-86. Chassis Map Card Location

4-24. ABBREVIATIONS. - Table 4-64 lists the abbreviations used on the logic schematics in addition to the abbreviations used in the instructions repertoire.

TABLE 4-64. Abbreviations

ACK	Acknowledge	FNCTN	Function
ADD	Adder	GRP	Group
ADR	Address	INHIB	Inhibit

TABLE 4-64. Abbreviations (continued)

ADV	Advance	LWR	Lower
AMPL	Amplifier	MN	Main
ARITH	Arithmetic	MA	Master
ASSY	Assembly	MEM	Memory
BTSTRP	Bootstrap	PRIOR	Priority
BRW	Borrow	PWR	Power
BFFR	Buffer	REG	Register
CKT	Circuit	REP	Repeat
CLR	Clear	REQ	Request
CMPTR	Computer	SEL	Selector/Select
CSL	Console	SEQ	Sequence
CTL	Control	T	Timing/Time
CTR	Counter	TERM	Terminate
CW	Control Word	TRNSLTR	Translator
DISTR	Distribution	UP	Upper
ENBL	Enable	•	And (x•y=>x and y)
		+	Or (x+y= > x or y)
		⊕	Logical ADD (Exclusive OR)

CHAPTER 5

PREVENTIVE MAINTENANCE

I - GENERAL

5-1. TOOLS AND TEST EQUIPMENT. - Computer maintenance requires the following tools and test equipment.

1) Oscilloscope, Tektronix Model 545B or equivalent

2) Preamplifier, Dual Trace, Tektronix Model CA or equivalent

3) Voltage Probe, X10 Attenuated, Tektronix P6006, 6 ft. or equivalent

4) Voltage Probe, X1 Straight, Tektronix P6028, 6 ft. or equivalent

5) Voltohmmeter, AN/PSM-4 Series or equivalent

6) Wire Wrap Tool, Hand Operated, Gardner-Denver #14H-1C, or equivalent

7) Nose Assembly for #14H-1C Tool, Gardner-Denver #500312, or equivalent

8) Bit and Sleeve Unit for Wire Wrap Tool, Gardner-Denver, or equivalent
   18 gauge - Bit #A-26336 - Sleeve #19688
   20 gauge - Bit #18633 - Sleeve #26245
   24 gauge - Bit #A-17612-2 - Sleeve #18840

9) Wire Unwrapping Tool, Dual Right and Left Hand
   20-26 gauge, Gardner-Denver #500130

10) Taper Pin Driver, AMP #389396-5

11) Tips for Taper Pin Driver
    18-20 gauge - Berg #35847
    22-24 gauge - Berg #34965

12) Taper Pin Crimpers
16-20 gauge, Berg #HT17
22-24 gauge, Berg #HT14

13) Hand Terminal Lug Crimper, 10-24 gauge, Thomas and Betts #WT-145A

14) Hand Terminal Lug Crimper, AMP #69061

15) Die for AMP Hand Terminal Lug Crimper, AMP #48752

16) Card Extender Cable Assembly, 0N068146

17) Indicator-Switch Wrench (spintight), Gulmite Socket, 1/2 OD#1418 or equivalent

5-2. MAINTENANCE SCHEDULES. - Regular scheduled maintenance of the computer consists of logic maintenance and cleaning.

a. Logic Maintenance. - Logic maintenance consists of running the automatic maintenance routines and diagnostic tests. The computer maintenance routines (Chapter 10, Volume IV) and diagnostic tests (Chapter 11, Volumes V and VI) contain the dynamic tests for the computer and all procedures required to run them. These tests can be used as a preventive maintenance check. Completion of the tests without an error ensures that the computer is operating properly. The schedule for running the routines and tests as preventive maintenance checks depends on the operating schedule of the system. However, they should be run on a regularly scheduled basis not exceeding a weekly schedule.

b. Cleaning. - Table 5-1, page 5-2, contains the cleaning schedules and procedures.

5-3. POWER CHECKS. - Use the following procedure to check the dc voltages on each chassis.

1. Place POWER ON/OFF switch to ON.

2. Check input voltage for 115 vac, line-to-line $\pm$1% of the average. Measure at power supply terminal board TB1, pins 4, 5, and 6.

TABLE 5-1. Cleaning Schedule and Procedures

Time	Item	Procedure
Weekly	Air filter	1. Release snap screws on filter grill (above power control panel). 2. Pull grill work out and up to expose filter. 3. Remove air filter. 4. Clean thoroughly with hot soapy water or steam. 5. Dry thoroughly. 6. Re-oil with light film of high-grade, filter oil. 7. Replace filter (reverse steps 1 through 3).
	Air exhaust vent	1. Check for obstructions in louvers. 2. Place main power switch off. 3. Extend power supply drawer (refer to paragraph 5-4b, page 5-6). 4. Vacuum exhaust port at rear of cabinet. 5. Close power supply drawer.
	Cabinet exterior	1. Place main power switch off. 2. Wipe cabinet exterior with damp cloth. 3. Using a soft brush, dust both logic panels and power control panel.
Monthly	Drawer slide lubrication	1. Place main power switch off. 2. Extend logic drawer A1.

TABLE 5-1. Cleaning Schedule and Procedures (continued)

Time	Item	Procedure
Monthly (cont.)	Drawer slide lubrication	3. Apply a light film of oil to bearing races of both drawer slides using a cloth dipped in a light lubricating oil. 4. Move drawer back and forth several times. 5. Close drawer. 6. Repeat for drawers A2, A3, A4, and PS1.
As required	Cabinet interior	1. Place main power switch off. 2. Extend logic drawer A1 (refer to paragraph 5-4a). 3. Vacuum inside of cabinet behind extended drawer. 4. Vacuum drawer. 5. Close drawer. 6. Repeat steps 2 through 5 for each drawer. 7. Vacum top connector assembly.
3. Check dc voltages at test points shown in table 5-2, page 5-5. Measure voltage between listed test point and corresponding ground test point.		

II - SERVICING

5-4. DRAWER ACCESS AND REMOVAL.

a. Logic and Memory. - To remove a logic or memory drawer complete the following procedures. To gain access to the test points perform steps 1 through 5. If it is not necessary to completely remove drawer, perform steps 1 through 8 to bring drawer to extended position.

TABLE 5-2. DC Voltage Test Points

Chassis	Test Point		Voltage (±5% Tolerance)	Max. Ripple Voltage (Peak-to-Peak)
	Number	Color		
A1A1	TB1-A4	Red	+15	0.2
	TB1-A3	Yellow	-4.5	0.2
	TB1-A2	Violet	-15	0.2
	TB1-A1	Black	Ground	
	TB2-G33		+15 indicator	
	TB2-G01		+15 indicator grd	
A1A2	TB1-A4	Red	+15	0.2
	TB1-A3	Yellow	-4.5	0.2
	TB1-A2	Violet	-15	0.2
	TB1-A1	Black	Ground	
A2A1	TB1-A4	Red	+15	0.2
	TB1-A3	Yellow	-4.5	0.2
	TB1-A2	Violet	-15	0.2
	TB1-A1	Black	Ground	
A2A2	TB1-A4	Red	+15	0.2
	TB1-A3	Yellow	-4.5	0.2
	TB1-A2	Violet	-15	0.2
	TB1-A1	Black	Ground	
	TB1-G11		+15 indicator	
	TB1-G33		+15 indicator grd	
A3A2	C27		+15	0.2
	A27		-15	0.2
	B27		-4.5	0.2
A4A2	C27		+15	0.2
	A27		-15	0.2
	B27		-4.5	0.2

1. Place POWER ON/OFF switch to OFF.

2. Lift and turn drawer door handle and swing door open.

3. To remove door swing open and lift straight up.

4. Remove knob in center of indicator panel.

5. Using Allen-end of drawer wrench, loosen three screws on edge of indicator panel.

6. Swing indicator panel open.

7. Insert drawer wrench in square socket at center of drawer and turn counterclockwise until drawer is free.

8. Pull drawer to extended position (locking catch engages).

CAUTION. - Due to weight of drawer do not attempt to remove it alone.

9. Remove drawer locking screws on upper and lower slide rails (see figure 1-5, page 1-7).

10. Release rear locking catch on lower rail.

11. Pull drawer from main cabinet and place on a hard smooth surface. Do not lay drawer on its sides.

12. To replace drawer, extend the slide rails and reverse removal procedure. To close extended drawer, release front locking catch on lower slide rail and reverse steps 1 through 8.

b. Power Supply. - To remove the power supply drawer complete the following procedure. If it is not necessary to completely remove drawer, perform steps 1 through 4 to bring drawer to extended position.

1. Place POWER ON/OFF switch to OFF.

2. Throw main power switch off.

3. Lift and turn the two catches on the front panel.

4. Pull drawer to extended position (locking catches on both slide rails engage).

5. Disconnect plugs P1 and P2 (see figure 1-7, page 1-9).

6. Release both rear locking catches.

7. Pull drawer out of cabinet.

8. Place drawer on hard smooth surface.

9. To replace drawer, extend slide rails and reverse removal procedure. To close extended drawer, release both front locking catches and reverse steps 1 through 3.

5-5. REPLACEMENT PROCEDURES.

a. Printed Circuit Cards. - To replace a printed circuit card in a logic or memory drawer complete the following procedure.

1. Place POWER ON/OFF switch to OFF.

2. Open drawer (see paragraph 5-4a, page 5-4).

3. Check associated chassis map (see paragraph 4-22, page 4-238) for chassis coordinates and card type of card to be replaced.

4. Remove card hold-down straps on each end of card.

5. Grasping card at upper and lower edge pull it out of jack with a slight rocking motion.

6. To install a card in a chassis, check chassis map for correct card type and reverse steps 4 and 5.

b. Indicator-Switch. - To remove and replace an indicator-switch or push-switch on the logic panel, complete the following procedure.

1. Place POWER ON/OFF switch to OFF.

2. Open logic drawer panel (see paragraph 5-4a, page 5-4).

3. Lift catch at top of protective plate and slide out plate.

4. Tag and remove wire-wrap connections from back of switch.

5. Remove locking nut on front panel with special wrench.

6. Remove switch.

7. Insert new switch.

8. Tighten locking nut with special wrench.

9. Rewire with wire-wrap tool. Original wires being rewrapped must also be soldered.

To replace the indicator portion complete the following procedure.

1. Turn amber lens counterclockwise and lift out.

2. Pry bulb from the lens and replace.

3. Replace bulb and lens assembly and turn clockwise until tight.

c. Power Panel.

(1) Switches. - To replace switches or indicator sockets on the power panel use the following procedure.

1. Release six snap-screws on grill and raise grill.

2. Remove filter.

3. Remove five screws along bottom edge of power panel.

4. Swing grill work up and remove five screws along inner top edge of the panel.

5. Pull panel forward and down for access to panel wiring.

6. Remove locking ring.

7. Push switch back through panel.

8. Tag and remove all wires.

9. To install new switch connect all wires and reverse removal procedure.

(2) Indicator bulbs. - To replace an indicator-bulb complete the following procedure.

1. Place POWER ON/OFF switch to OFF.
2. Unscrew the lens cover.
3. To remove bulb, press and turn counterclockwise one-quarter turn.
4. Insert new bulb, press, and turn clockwise.
5. Replace lens cover.

d. Fuses.

(1) Power supply. - To replace a fuse in the power supply complete the following procedure. Table 5-3, page 5-10, lists the location, rating, and associated circuit of fuse.

1. Place POWER ON/OFF switch to OFF.
2. Open power supply drawer (see paragraph 5-4b, page 5-6).
3. Locate faulty fuse.
4. Unscrew fuse cap.
5. Remove blown fuse from cap.
6. Replace fuse with new fuse of proper current and voltage rating.
7. Replace fuse cap.

(2) Main cabinet. - Fuses are located behind each drawer in the main cabinet. To replace a fuse located behind a drawer complete the following procedure.

1. Throw main power switch off.
2. Place POWER ON/OFF switch to OFF.

TABLE 5-3. Fuses

Fuse	Location	Rating	Volts	Circuit Protected
F16	PS1	8A *	115	115v Ø1 } Input voltage fuses
F17	PS1	8A *	115	115v Ø2 } Input voltage fuses
F18	PS1	8A *	115	115v Ø3 } Input voltage fuses
F10	PS1	2A *	115	+15v indicator supply
F11	PS1	2A *	115	+15v indicator supply
F12	PS1	2A *	115	+15v indicator supply
F13	PS1	2A *	115	A6 and A7 Blower Assembly
F14	PS1	2A *	115	A3 and A4 Blower Assembly
F15	PS1	2A *	115	A3 and A4 Blower Assembly
F1	PS1	1A *	115	-4.5v supply
F2	PS1	1A *	115	-4.5v supply
F3	PS1	1A *	115	-4.5v supply
F4	PS1	3A *	115	-15v supply
F5	PS1	3A *	115	-15v supply
F6	PS1	3A *	115	-15v supply
F7	PS1	2A *	115	+15v supply
F8	PS1	2A *	115	+15v supply
F9	PS1	2A *	115	+15v supply
F1	A1	8A	4.5	-4.5v supply

* Slow blow

TABLE 5-3. Fuses (continued)

Fuse	Location	Rating	Volts	Circuit Protected
F2	A1	10A	15	-15v supply
F3	A1	3A	15	+15v supply
F4	A1	8A	4.5	-4.5v supply
F5	A1	10A	15	-15v supply
F6	A1	3A	15	+15v supply
F1	A2	8A	4.5	-4.5v supply
F2	A2	10A	15	-15v supply
F3	A2	3A	15	+15v supply
F4	A2	8A	4.5	-4.5v supply
F5	A2	10A	15	-15v supply
F6	A2	3A	15	+15v supply
F4	A3	8A	4.5	-4.5v supply
F5	A3	10A	15	-15v supply
F6	A3	10A	15	+15v supply
F4	A4	8A	4.5	-4.5v supply
F5	A4	10A	15	-15v supply
F6	A4	10A	15	+15v supply

3. Open affected drawer (see paragraph 5-4a, page 5-4).

4. Release chassis lock at rear left-hand chassis.

5. Swing movable chassis open.

6. Locate and remove fuse cap containing faulty fuse.

7. Replace fuse with new fuse of proper current and voltage rating.

8. Replace fuse cap.

e. Wiring. - Wiring replacement should be accomplished only when the trouble has been definitely traced to the wiring or the replacement of another part requires wiring replacement. To replace a logic or memory chassis wire complete the following procedure.

1. Throw main power switch off.

2. Place POWER ON/OFF switch to OFF.

3. Open affected drawer (see paragraph 5-4a, page 5-4).

4. Release chassis lock at rear of left-hand chassis.

5. Swing movable chassis open.

6. Locate wire to be replaced.

7. Remove one end of wire with unwrapping tool.

   Note: - If the wire being replaced is on the second or third level the wires above it and all affected wires must also be replaced.

8. Remove other end of wire (see note).

9. Use wire-wrap tool to replace wire. Use the same gauge, color, and length as the original wire.

10. Repeat steps 6 through 8 until all affected wires are replaced.

11. Close chassis.

12. Close drawer.

5-6. ADJUSTMENTS.

a. Master Clock. - Adjust the master clock if the output does not meet the following requirements.

Note: - Before adjusting the clock, check for malfunction or marginal conditions in the associated circuits. Any change in circuit loading affects the clock output.

1) Cycle time: 670 ±34 nanoseconds (test point 2TB2G11, figure 5-1.

2) Pulse width: 120 nanoseconds minimum at -2v amplitude.

Testpoints: Ø1 - 2TB2G1
Ø2 - 2TB2G2
Ø3 - 2TB2G3
Ø4 - 2TB2G4.

3) No phase pulse overlap between adjacent pulses at -1v amplitude.

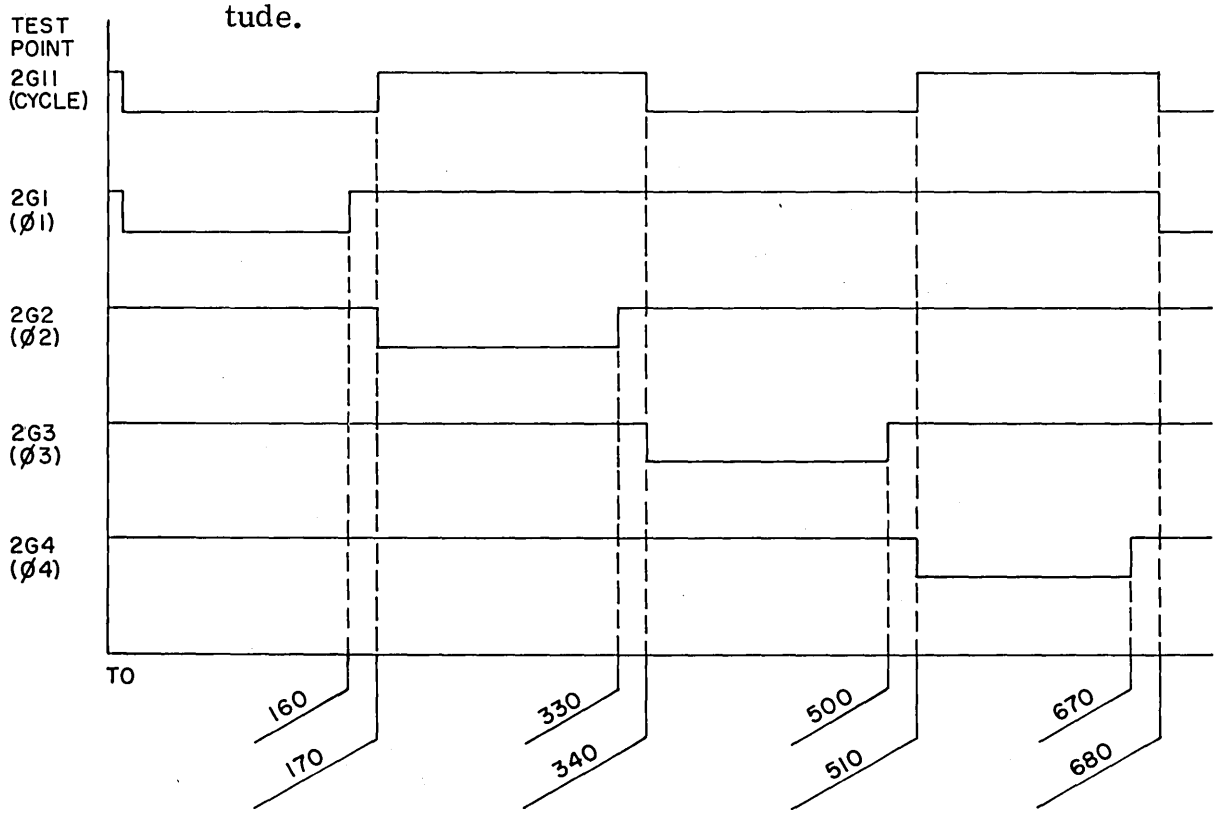


Figure 5-1. Master Clock Waveforms

(1) Cycle time adjustment. - To adjust the master-clock cycle-time, complete the following procedure.

1. Place POWER ON/OFF switch to ON.

2. Momentarily place MASTER CLEAR switch to down position.

3. Press OP STEP MODE switch.

4. Adjust oscilloscope for an amplitude of 2 volts/cm and a time base of 0.1 μsec/cm.

5. Connect scope probe to test point 2TB2G11 and measure cycle time. Figure 5-1, page 5-13, shows the idealized waveform.

6. If cycle time is greater than 704 nanoseconds, move the lead going to pin 8 of the 64016 card at 2J34C (20C00) to a delay line tap on 20C20 or 20C30 that provides less time delay (figure 5-2, page 5-15).

7. If cycle time is less than 636 nanoseconds, move the lead to a delay line tap that provides more time delay.

Changing the cycle time will affect the phase pulse timing. After adjusting the cycle time, check and adjust the phase pulse timing as required.

(2) Phase pulse adjustment. - To adjust phase pulse timing complete the following procedure.

1. Complete steps 1 through 4 of cycle-time, adjustment procedure in paragraph 5-6a(1).

2. Measure and record the pulse width of each phase pulse. Figure 5-2, page 5-15, shows initiation and termination control of each pulse. Figure 5-1, page 5-13, shows the idealized, phase-pulse waveforms.

3. Display adjacent pulses on dual traces of oscilloscope (1 and 2, 2 and 3, 3 and 4, 4 and 1) and record results.

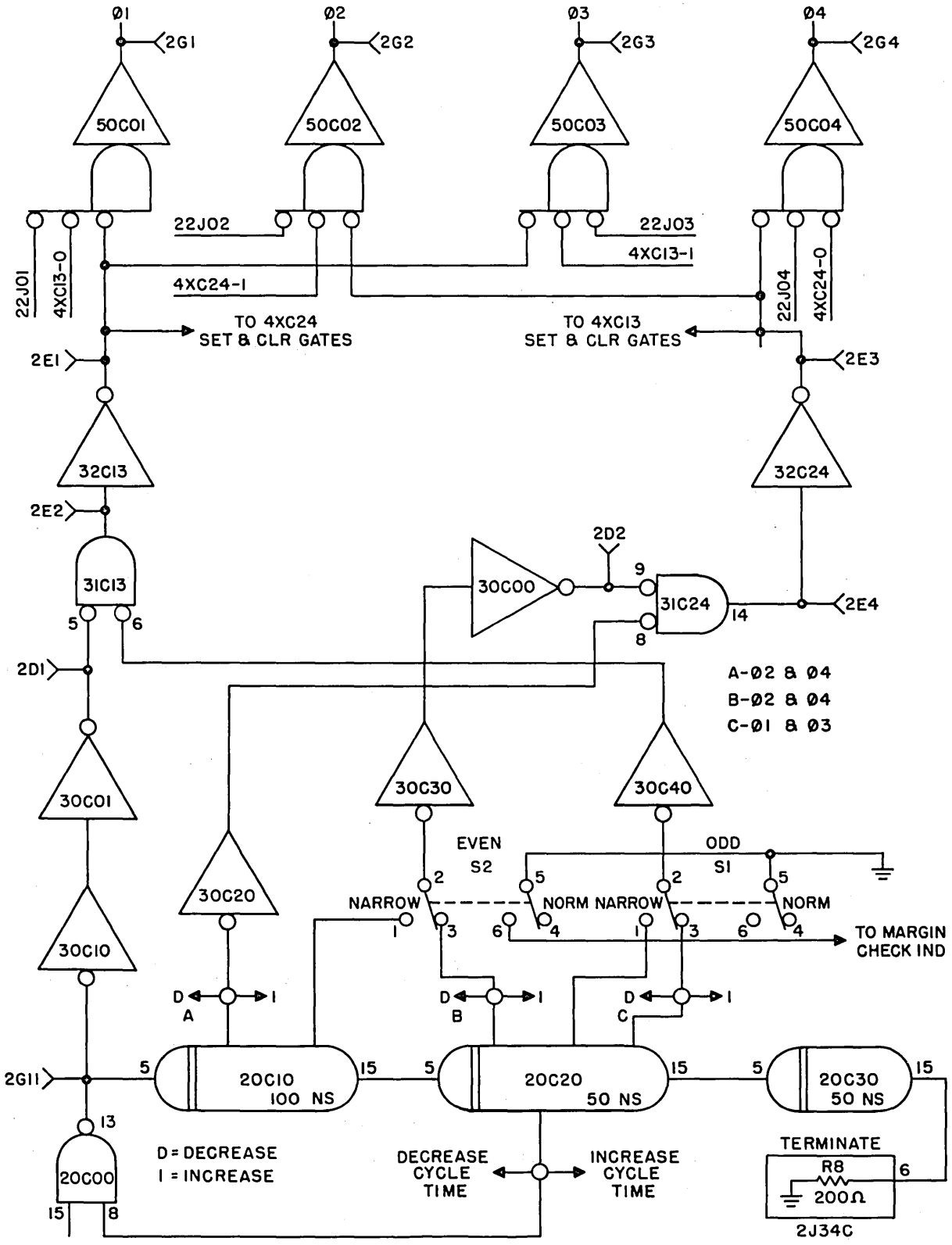


Figure 5-2. Master Clock Adjustment

4 Place clock margin switches, ODD and EVEN, to NARROW position.

5. Repeat steps 2 and 3. Phase pulse width should be between 80 and 110 nanoseconds at -2v amplitude.

6. From results of steps 2 through 5 adjust delay line taps as required.

b. Memory-Protect Voltage Adjustment. - Adjust the four voltage-sensor cards (two on each memory chassis) to force the computer into the phase-step mode when a logic voltage or the input voltage drops to 100 volts. Use the following procedure.

1. Place POWER ON/OFF switch to OFF.

2. Open chassis A4, remove cards at locations A12 and A13, and close chassis.

3. Open memory chassis A3 and remove cards at locations A12 and A13.

4. Insert card extenders in jack locations A12 and A13 and close chassis A3.

5. Insert one of the 68006 cards in A13 extender and connect oscilloscope probe to test point A3TB1G33.

6. On front panel of motor generator controller, turn AUTO VOLTAGE ADJUST rheostat to obtain A-C VOLTS meter indication of 100.

7. Check computer input voltage. If less than 100 vac repeat step 6.

8. Place POWER ON/OFF switch to ON.

9. Adjust R7 on 68006 card for a small negative signal (-0.1v) on oscilloscope. (Scope indications: ground, then slight oscillation, then -0.1v.)

10. Place POWER ON/OFF switch to OFF.

11. Place other 68006 card in extender.

12. Repeat steps 8 and 9.

13. Place POWER ON/OFF switch to OFF.

14. Remove 68006 card from extender.

15. Place one of the 68002 cards in A12 extender.

16. Place POWER ON/OFF switch to ON.

17. Adjust R3 and R8 on 68002 card for a small negative signal (-0.1v) on oscilloscope.

18. Place POWER ON/OFF switch to OFF.

19. Repeat steps 16 through 18 using other 68002 card.

20. Place one of the 68006 cards in A13 extender.

21. Place POWER ON/OFF switch to ON.

22. Press RUN MODE switch.

23. Turn AUTO VOLTAGE ADJUST rheostat to reduce A-C VOLTS meter indication by slight amount (0.5v). Computer should switch to PHASE STEP mode.

24. Place POWER ON/OFF switch to OFF.

25. Turn AUTO VOLTAGE ADJUST rheostat to obtain A-C VOLTS meter indication of 100.

26. Repeat steps 21 through 24 using other set of cards (68006 and 68002).

27. Open chassis A4, replace 68002 card in jack A13, replace 68006 card in jack A12, and close chassis.

28. Repeat step 27 with chassis A3.

29. Place POWER ON/OFF switch to ON.

30. Press RUN MODE switch.

31. Repeat step 23. Computer should switch to PHASE STEP mode. If it does not, readjust all cards.

32. Turn AUTO VOLTAGE ADJUST rheostat to obtain A-C VOLTS meter indication of 115.

33. Check computer input voltage for 115 vac, line to line $\pm$1% of average.

CHAPTER 6

CORRECTIVE MAINTENANCE

I - GENERAL

6-1. TOOLS AND TEST EQUIPMENT. - Paragraph 5-1, page 5-1, lists all tools and test equipment required for corrective maintenance.

6-2. MAINTENANCE ROUTINES AND DIAGNOSTIC TESTS. - Chapter 10, Volume IV, contains complete maintenance routines which test all computer circuits.

Chapter 11, Volumes V and VI, contains complete corrective maintenance procedures for all logic and memory circuits. The manual contains all procedures for running the tests and isolating the malfunction to a card or cards.

II - TROUBLESHOOTING

6-3. OBSERVABLE SYMPTOMS. - When a malfunction is suspected, inspect the panel switches and indicators and the fuses for any indications which may isolate the trouble. If a malfunction occurs during program loading or shortly after starting a new program, check the initial switch settings as contained in the program documentation. Table 6-1 lists malfunction indications and possible cause of the malfunction. Table 5-3, page 5-10, lists all fuses and associated circuits.

TABLE 6-1. Malfunction Indications

Indication	Probable Cause	Reference
Power not applied when POWER ON/OFF switch is placed to ON	1. Main power switch open	
	2. Fuses PS1, F16, F17, and F18	Table 5-3, page 5-10
	3. Power sequence relay PS1K1	Figure 8-102, page 8-219
	4. POWER ON/OFF switch	Figure 8-101, page 8-217

TABLE 6-1. Malfunction Indications (continued)

Indication	Probable Cause	Reference
Logic voltages not applied	1. Airflow sensor relay A5A2K1	Figure 8-101, page 8-217 and paragraph 6-6, page 6-28
	2. Time delay relay A5A2K1	Figure 8-101, page 8-217
Power applied, blowers (cabinet & memory) do not start	1. Fuses PS1, F16, F17, F18, F13, F14, or F15	Table 5-3, page 5-10
	2. Power sequence relay K1	
	3. 60°C (140°F) sensors	Figure 8-102, page 8-219
	4. PS1 interlock	
	5. Blower motors	
	6. Memory chassis not fully engaged (memory blowers only)	
Power applied, blowers start, indicators are not lighted	1. Fuses F10, F11, and F12	Table 5-3, page 5-10
	2. +15v indicator-supply transformer T2 and associated circuits	Figure 8-103, page 8-221
Indicators are not extinguished	1. Fuses F1, F2, and F3	Table 5-3, page 5-10
	2. -4.5v transformer T4 and associated circuits	Figure 8-102, page 8-219
Individual indicators are not lighted or extinguished.	1. Indicator-switch module	Paragraph 4-22d, page 4-241
	2. Indicator-driver circuit	
	3. Panel wiring	Chapter 9, Volume III

TABLE 6-1. Malfunction Indications (continued)

Indication	Probable Cause	Reference
Horn sounding and OVER TEMP alarm indicator lights	1. Cabinet temperature exceeds 46°C (115°F) 2. 46°C (115°F) sensor shorted	Figure 8-101, page 8-217
Horn sounding and OVER TEMP indicator is lighted, when all indicators are lighted	1. Cabinet temperature exceeds 60°C (140°F) 2. 60°C (140°F) sensor open	Figure 8-102, page 8-219
Horn sounds and AIR FLOW FAULT indicator lights during operation	1. Cabinet air leak (insufficient airflow) 2. Relays A5A2 K1, K2, or K3 3. Blowers inoperative	Figure 8-101, page 8-217 Figure 8-102, page 8-219
MARGINAL CHECK indicator is not lighted when memory or clock margin switch is operated	1. Indicator bulb 2. Logic terms 92V02 & 92V03 3. Memory or clock margin switch	Paragraph 5-5, page 5-7 Figure 8-101, page 8-217 Figure 8-99, page 8-213 or 8-2, page 8-5
PROGRAM RUN indicator is not lighted when RUN MODE switch is pressed	1. Indicator bulb 2. Logic term 90V03 3. Run flip-flop circuits	Paragraph 5-5, page 5-7 Figure 8-101, page 8-217 Figure 8-1, page 8-1

TABLE 6-1. Malfunction Indications (continued)

Indication	Probable Cause	Reference
FAULT indicator and one of the FAULT INDICATORS are lighted	Logic fault exists	Figure 8-90, page 8-195, and paragraph 4-16i, page 4-82

6-4. SECTIONAL TROUBLESHOOTING. - The computer comprises three troubleshooting sections, power, memory, and logic. The procedures listed for each section serve to isolate a malfunction to that particular section and to check most of the circuits in that section. The example in each section assumes that a malfunction has been isolated to that section and shows a typical procedure for further isolation of the malfunction. The symptoms used in the example may not occur in normal operation and may be caused by a circuit other than the one isolated.

a. Power Section. - Use the following procedure to isolate a malfunction within the power section.

(1) Power troubleshooting procedure. - Perform the following steps to check the power circuits.

1. Place POWER ON/OFF switch to ON. The following normal power-up sequence occurs.

    1) AIR FLOW FAULT indicator and all logic panel indicators light.

    2) Thirty seconds after power-on, AIR FLOW FAULT and logic panel indicators go out, and dc logic voltages become available.

2. If normal power-up sequence does not occur, see table 6-1, page 6-1, for indication and probable cause of malfunction.

3. Check line-to-line input voltage (115 vac, line-to-line, ±1% of average 400 Hz).

4. Check dc logic voltages. Table 5-2, page 5-5, lists test points and voltages.

5. If a dc logic voltage is not as specified in table 5-2, page 5-5, check associated fuses (table 5-3, page 5-10) and circuits (figure 8-103, page 8-221).

(2) Power troubleshooting example. - Use this example as a guide in analyzing a malfunction to isolate a defective component.

(a) Conditions and symptoms.

1) POWER ON/OFF switch placed to ON.

2) Normal power-up sequence occurs with one exception: logic panel indicators are not extinguished after 30-second delay.

(b) Logical analysis. - The +15v indicator supply, the -4.5v supply, and the individual driver circuits control the logic panel indicators. Since all indicators are affected, the individual driving circuits are not causing the malfunction. The +15v indicator supply turns on the individual collectors (see figure 4-85, page 4-241); therefore it is not causing the malfunction. The -4.5v supply provides the base bias on the indicator modules to hold the indicators extinguished until they are lighted by the individual driver circuits. Therefore the -4.5v supply is the probable cause of the malfunction. Perform the following steps to further isolate the defective component.

1. Check all dc logic voltages. The +15v and -15v are present and within tolerance. The -4.5v is not available at any chassis test points.

2. Place POWER ON/OFF switch to OFF.

3. Open power supply drawer.

4. Check fuses PS1F1, PS1F2, and PS1F3. Fuses are not defective.

5. Check diodes CR19 through CR24 for open or shorted diodes. Diodes are not defective.

6. Check inductor L2 for open circuit. Inductor L2 is an open circuit.

7. Remove and replace inductor L2.

8. Close power supply drawer.

9. Place POWER ON/OFF switch to ON. Normal power-up sequence now occurs.

10. Check output of -4.5v supply on each chassis (see table 5-2, page 5-5). Voltage is present and within tolerance; malfunction is corrected.

b. Memory Section.

(1) Memory troubleshooting procedure. - Memory errors that occur in a logical pattern generally indicate component failure, either in the memory itself or in associated logic circuits. Random memory errors generally indicate poorly adjusted drive currents or read strobe. See paragraph 6-5, page 6-22, for drive current and read strobe adjustment procedures.

CAUTION. - Do not adjust memory drive currents or read strobe timing until the equipment has been energized for at least four hours and no circuit malfunctions exist.

Paragraphs 6-4b(1)(a) through 6-4b(1)(h), pages 6-7 through 6-14, provide procedures for checking the memory section and isolating malfunctions. Perform the following preliminary procedure before performing these checks.

1. Check dc voltages (see table 5-2, page 5-5).

2. Check S and P-registers to make sure they function correctly and P advances correctly.

3. OP STEP through a 12 (STR) and then a 30 (CLA) instruction to see if logic circuits concerned with storing and reading are working correctly. Paragraph 4-21, page 4-171, contains instruction timing charts.

4. Set computer switches as follows.

   HALT DISCONNECT in up position

   FUNCTION REPEAT in up position

   MASTER CLEAR momentarily to down position

   F-register equal zero

   RUN MODE pressed

   RESTART/START STEP to START STEP

5. Cycle the computer to check the memory. Computer cycles 00 (HLT) instructions, advancing P through its entire range and reading all memory addresses.

(a) Memory control check.

1. Use the following oscilloscope settings.

Time/cm:	0.5 sec
Triggering mode:	EXT -
Trigger input:	A2A1TB1G01 (02T11)

2. Check waveforms of following circuits in both memory chassis at test points indicated (see figure 8-91, page 8-197, for waveforms).

Read enable	(10L11) N27
Write enable	(10L10) O27
Address enable	(14L01) N22
Address enable	(15L00) P27
Address enable	(17L00) Q27

3. Check the following at the test points indicated.

   Inhibit enable (12L02) A1A1TB1A10

   Inhibit enable (14L02) A1A2TB2G8

   Read strobe (mem Z) - lower (30N30) A1A1TB1G1

   Read strobe (mem Z) - upper (31N30) A1A2TB2A33

(b) Y-transformer translation check.

1. To force the computer to operate with only one stack in each memory chassis, insert jumpers listed in table 6-2.

2. Use the following oscilloscope settings.

   Time/cm: 5 sec

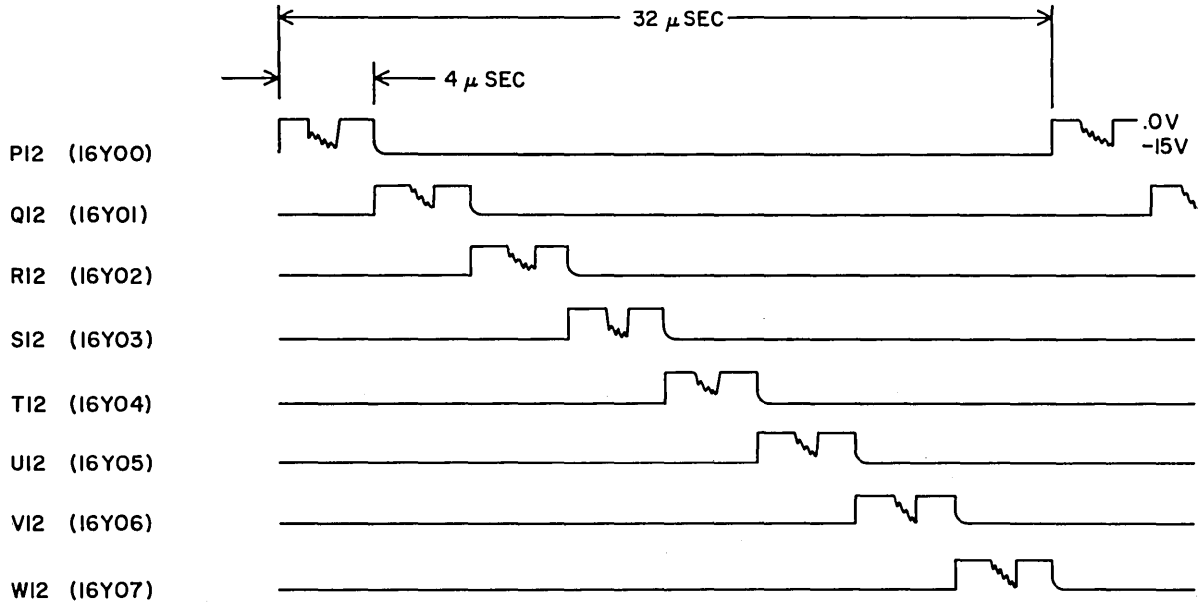
   Triggering mode: EXT +

   Trigger input: P12 (16Y00) on memory chassis

TABLE 6-2. Jumper Connections for One-Stack Memory Operation

Stack	Jumper Connections From Ground (A1A1TB2A33) to
A20 (S13 and S12) Translation 00	01P12 (A1A1TB2A23) and 00P13 (A1A2TB2C23)
A21 (S13 and S12) Translation 01	00P12 (A1A1TB2B23) and 00P13 (A1A2TB2C23)
A22 (S13 and S12) Translation 10	01P12 (A1A1TB2A23) and 00P13 (A1A2TB2D23)
A23 (S13 and S12) Translation 11	01P12 (A1A1TB2B23) and 00P13 (A1A2TB2D23)

3. Check for the following waveforms in both memory chassis.



4. Repeat waveform check for each memory stack.

(c) Y-diode translation check

1. Make jumper connections listed in table 6-2, page 6-8.

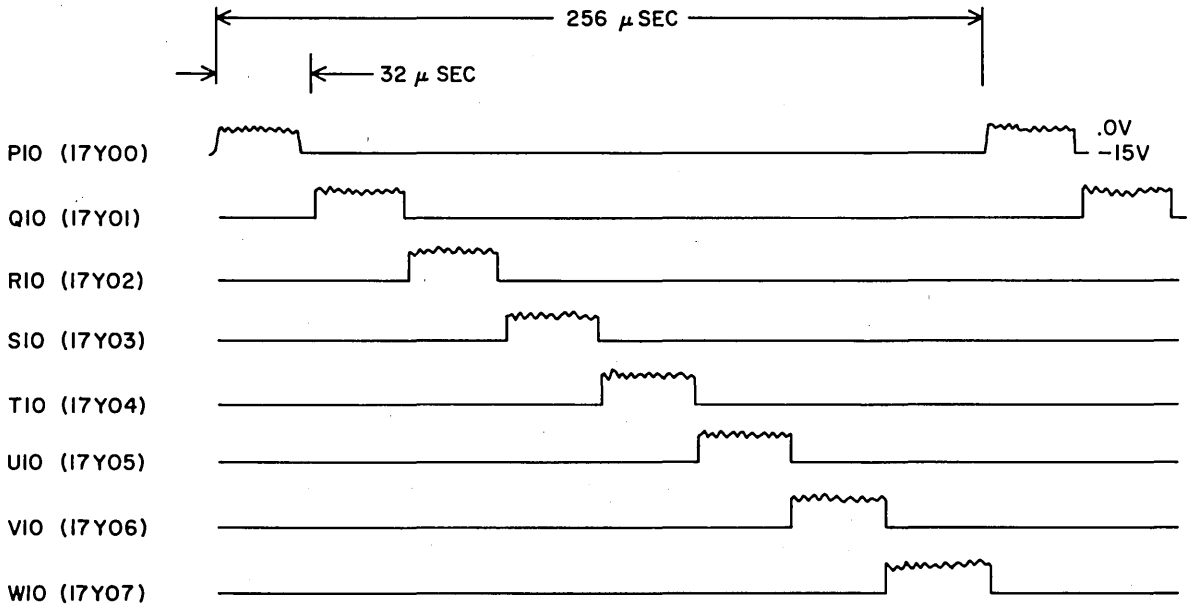
2. Use the following oscilloscope settings.

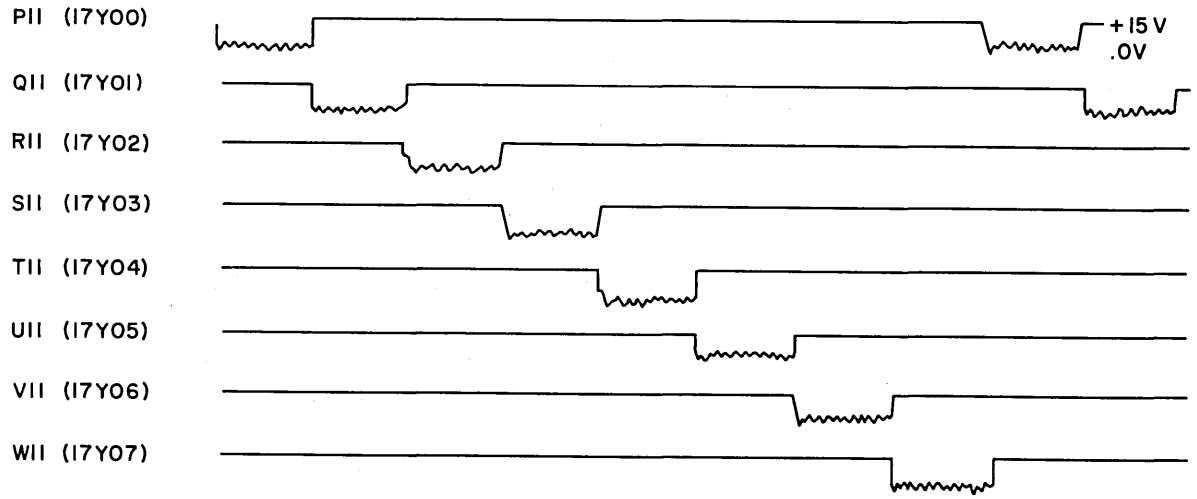
Time/cm: 50 μsec

Triggering mode: EXT +

Trigger input: P10 (17Y00)

3. Check for the following waveforms in both memory chassis.





4. Repeat waveform check for each memory stack.

(d) X-transformer translation check.

1. Make jumper connections listed in table 6-2, page 6-8.

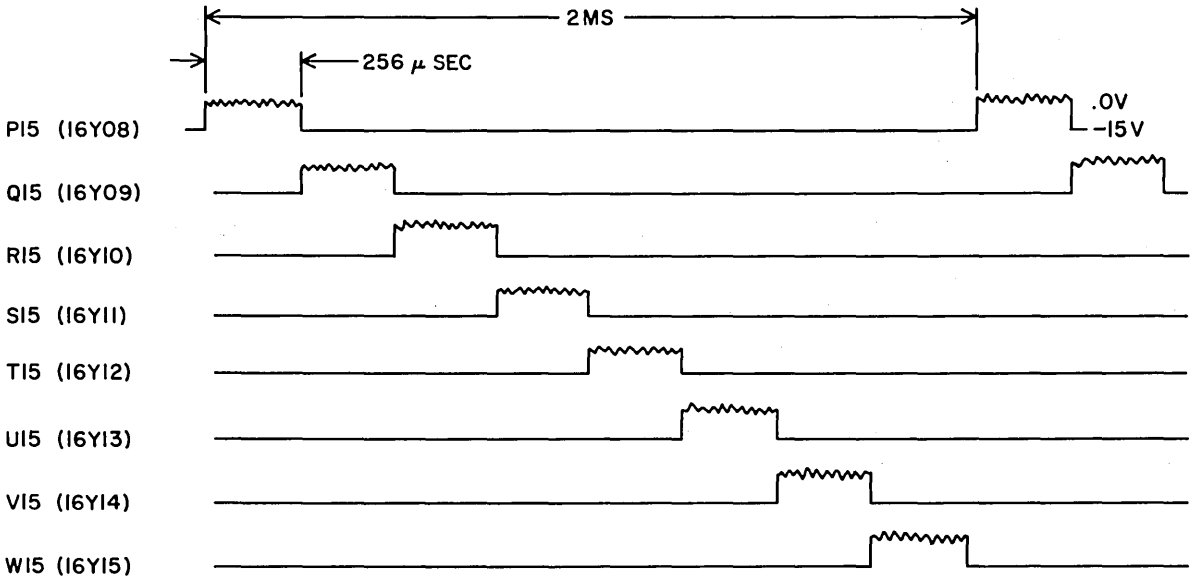
2. Use the following oscilloscope settings.

   Time/cm: 200 μsec

   Triggering mode: EXT +

   Trigger input: P15 (16Y08)

3. Check for the following waveforms in both memory chassis.



4. Repeat waveform check for each memory stack.

(e) X-diode translation check.

1. Make jumper connections listed in table 6-2, page 6-8.

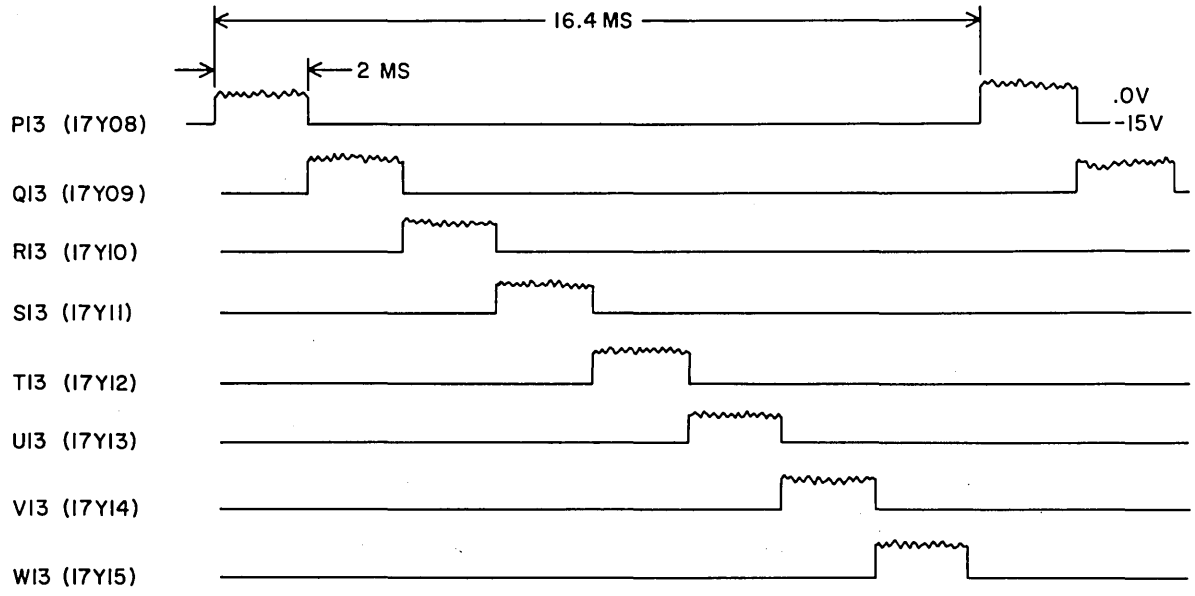
2. Use the following oscilloscope settings.

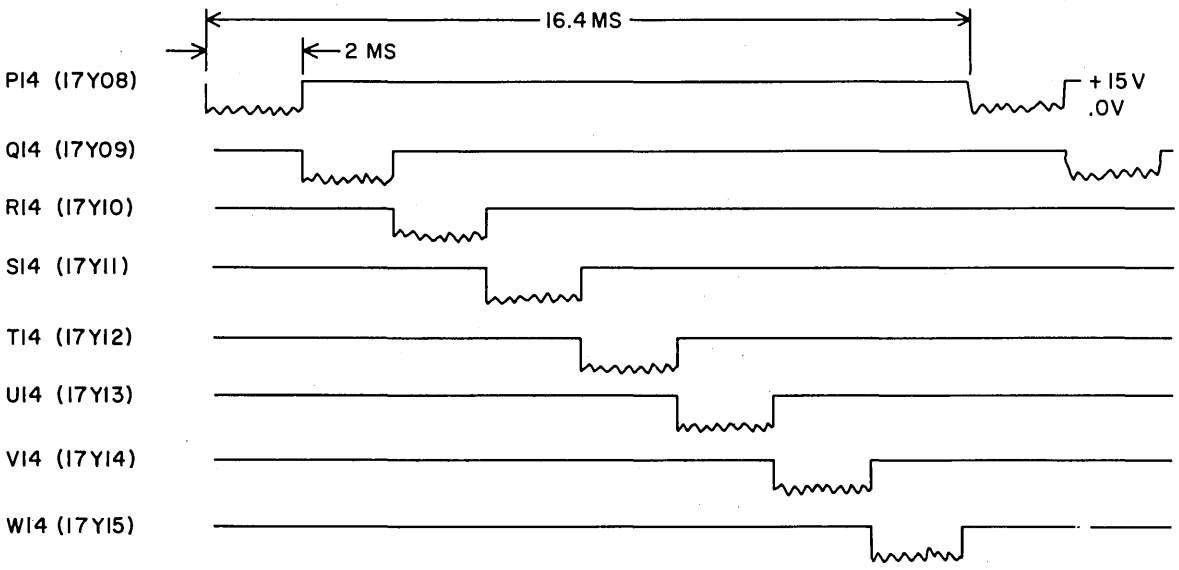
   Time/cm: 2 ms

   Triggering mode: EXT +

   Trigger input: P13 (17Y08)

3. Check for the following waveforms in both memory chassis.





4. Repeat waveform check for each memory stack.

(f) Stack selection translation check.

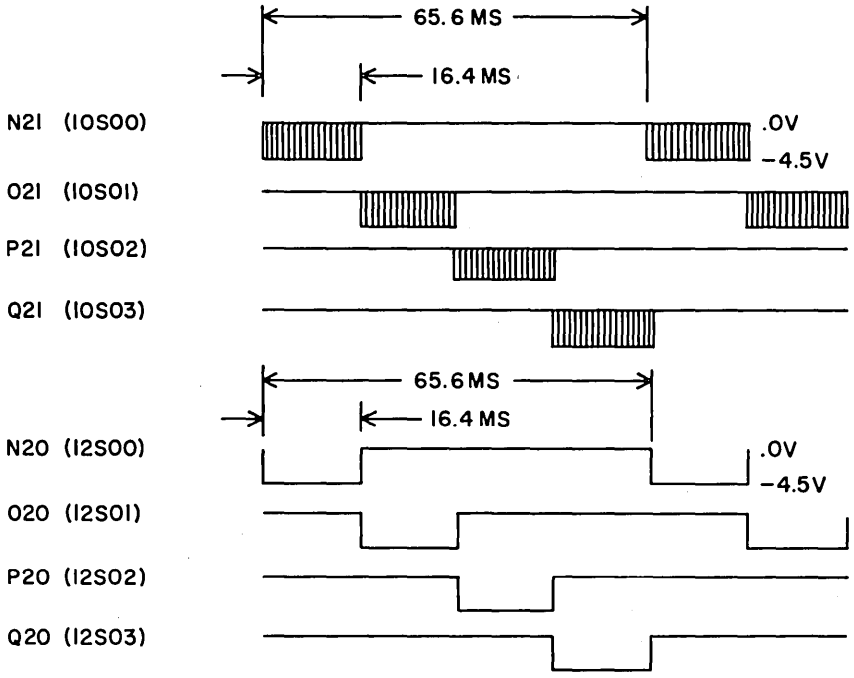
1. Use the following oscilloscope settings.

   Time/cm: 10 ms

   Triggering mode: EXT +

   Trigger input: N21 (10S00)

2. Check for the following waveforms in both memory chassis.



(g) Read/write transient checks.

1. Use the following oscilloscope settings.

   Time/cm: 1 μsec

   Triggering mode: EXT -

   Trigger input: A2A1TB1G01 (02T11)

2. Check for the following waveform in both memory chassis.

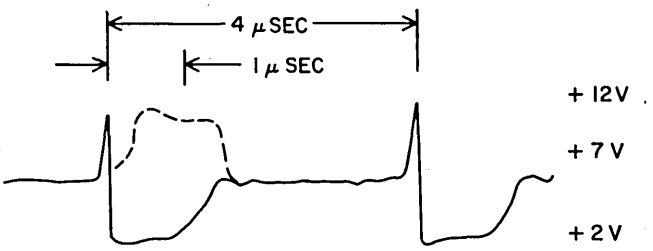
   Y Write (19Y00) T24

   Y Read (19Y01) T25

   X Write (19Y02) S22

   X Read (19Y03) T23

   Correct waveform is approximately as follows. Actual voltage levels will depend on potentiometer (current) adjustment. A waveform similar to the dotted line indicates an open circuit.



An open indication for both read and write of a particular axis usually indicates an open drive line. An open indication on only the read or the write usually indicates an open diode. Diode numbering coincides with diode translation. To discover the location of the open circuit compare the frequency of its appearance with the translation frequencies in paragraphs 6-4b(1)(b) through 6-4b(1)(f), pages 6-8 through 6-13, or load all address with ones, read them back, and observe the pattern of failing addresses.

(h) Sense output and inhibit checks. - This procedure checks the inhibit circuits by proving the ability of the memory to read and write ones and zeros.

1. Use the following oscilloscope settings.

   Time/cm: 0.5 sec

   Triggering mode: EXT -

   Trigger input: A2A1TB1G01 (02T11)

2. While computer is cycling, hold each bit of Z set momentarily to load all ones into memory.

3. Check the following in both memory chassis.

   A20 (14Y00) 2^0 or 2^{12}

   B20 (14Y01) 2^1 or 2^{13}

   C20 (14Y02) 2^2 or 2^{14}

   D20 (14Y03) 2^3 or 2^{15}

   E20 (14Y04) 2^4 or 2^{16}

   F20 (14Y05) 2^5 or 2^{17}

   G20 (14Y06) 2^6 or 2^{18}

   H20 (14Y07) 2^7 or 2^{19}

   I20 (14Y08) 2^8 or 2^{20}

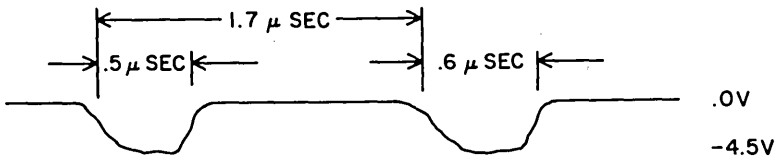
   J20 (14Y09) 2^9 or 2^{21}

   K20 (14Y10) 2^{10} or 2^{22}

   L20 (14Y11) 2^{11} or 2^{23}

   M20 (14Y12) Parity

   The waveforms should appear approximately as follows.



4. Place Marginal Check switch to HIGH position.

5. Press and hold Z-register Clear button to load all zeros into memory.

6. Repeat step 3. The signals remain at 0v.

7. Hold one bit of the Z-register set momentarily to clear parity bit to a zero.

(2) Memory troubleshooting example.

(a) Conditions and symptoms.

1) Computer running.

2) PARITY ERROR indicator is lighted.

3) Preliminary troubleshooting indicates bit 0 of the A-register does not set unless indicator-switch is pressed.

(b) Logical analysis. - Perform the following procedure to systematically isolate the malfunction.

1. Perform steps 1 and 2 of paragraph 6-4b(1), page 6-6. This procedure fails to isolate malfunction.

2. Step through a 12 (STR) instruction with all bits of the A-register set to one and P set to 0700_8.

3. Step through a 30 (CLA) instruction with P set to 0700_8. Bit 1 of the A-register fails to set.

4. Set computer to cycle 00 (HLT) instruction see step 5 of paragraph 6-4b(1), page 6-6. Since malfunction affects only bit 0, malfunction is probably in bit-0 sense, inhibit, or gating circuits.

5. Perform procedures in paragraph 6-4b(1)(h), page 6-14. Check waveform at test point A20 of chassis A3A2. Waveform is a constant ground potential.

6. Check input to bit-0 inhibit generators a bit-0 selector output (A1A1TB1 F7). Input is -4.5v necessary to write a one in bit-0.

7. Check output waveforms of all four bit-0 sense amplifiers at A21, A22, A23, and A24 on chassis A3A2. Each waveform is a positive-going, 0.5 μsec pulse every 6.8 μsec. This isolates the malfunction to logic term 14Y00 (figure 8-99, page 8-213) at card location A3A2-J2C.

8. De-energize computer (see paragraph 3-7, page 3-22.

9. Open chassis A3A2.

10. Remove and replace 71761 card at jack 2C.

11. Close chassis.

12. Energize computer (see paragraph 3-2, page 3-16).

13. Perform procedure in paragraph 6-4b(1)(h), page 6-14. Malfunction is corrected.

(3) Bootstrap memory troubleshooting procedure. - To check the operation of the bootstrap memory complete the following procedure after the computer has been energized.

1. Momentarily place MASTER CLEAR switch to down position.

2. Place FUNCTION REPEAT switch in up position.

3. Press OP STEP MODE indicator switch.

4. Set F-register to 30_8 (CLA) instruction.

5. Set P-register to 60_8 (first bootstrap address).

6. Place RESTART/START-STEP to START-STEP. The contents of the first bootstrap address should be read

into the Z-register. Table 6-3, lists the contents of all bootstrap addresses.

7. Repeat step 6 for all 20_8 addresses.

8. If a malfunction occurs refer to figure 8-100, page 8-215, and check the output, the word drivers, and the bootstrap to Z-register gates.

c. Logic Section.

(1) Troubleshooting procedures. - Logic errors that occur as solid recurring faults generally indicate component failure. Intermittent or random errors generally indicate an intermittent component failure or failure of a timing circuit component. Paragraph 5-6a, page 5-13, contains computer timing check and adjustment procedures. Use the following general procedure to check the operation of the logic section of the computer. For complete checkout procedures, see the manuals listed in paragraph 6-2, page 6-1.

1. Energize computer (see paragraph 3-2, page 3-16).

TABLE 6-3. Bootstrap Memory Contents

Address	Contents	Address	Contents
00060	20000051	00070	20000055
00061	60000067	00071	60000077
00062	24000050	00072	24000054
00063	16102351	00073	16040220
00064	36001050	00074	36000054
00065	30000064	00075	30000074
00066	30037600	00076	30037600
00067	04037600	00077	07777600

2. Check dc voltages on each logic chassis (see table 5-2, page 5-5).

3. Check master clock output (see paragraph 5-6a, page 5-13).

4. Check operation of all registers by pressing all register indicator-switches and associated clear switches.

5. Set computer switches as follows.

   HALT DISCONNECT in up position

   FUNCTION REPEAT in up position

   RESTART SPEED CONTROL turned fully counterclockwise

   MASTER CLEAR momentarily to down position

   F-register equal zero

   OP STEP MODE pressed

   RESTART/START STEP to RESTART

6. Cycle computer to check preliminary operation. Computer cycles 00 (HLT) instructions to advance P through its entire range at slow speed.

7. If the malfunction occurs, stop computer and OP STEP through the 00 (HLT) instruction. (See paragraph 4-21, page 4-171, for 00 (HLT) instruction timing.)

8. If the malfunction prevents the advance of P, check P-register enables, P-register, and adder.

9. OP STEP computer through the first three instructions in table 6-4, page 6-21, in the order listed.

10. Set computer switches as follows.

    HALT DISCONNECT in up position

MASTER CLEAR momentarily to down position

PHASE STEP MODE pressed

11. Repeatedly place RESTART/START STEP switch to START STEP to generate successive phase pulses.

12. PHASE STEP computer through the last two instructions in table 6-4, page 6-21, in the order listed.

Table 6-4, page 6-21, lists the result of each instruction if the circuits are operating properly. If the listed result is not obtained, trace the malfunction by analyzing the contents of the A-register and the events listed in the instruction timing charts.

(2) Troubleshooting example.

(a) Conditions and symptoms.

1) Computer running.

2) FAULT indicator is lighted.

3) Horn sounds.

4) FAULT INDICATORS HALT indicator is lighted.

5) P-register contains 01777.

(b) Logical analysis. - Perform the following procedures to systematically isolate the malfunction.

1. Perform steps 1 through 4 of paragraph 6-4c(1), page 6-18. This fails to isolate malfunction.

2. Set computer to op step through 00 (HLT) instruction. Normal operation continues until P-register contains 01777.

3. Stop computer and manually check operation of P-register. No malfunction is evident.

4. Set the P-register to 01776.

TABLE 6-4. Instruction Logic Checks

Instruction	Initial Register Settings	Result
LGN(f = 01)	F = 01_8 M = 00 A = 00000000	A = 77777777_8
STR(f = 12)	F = 12_8 M = 00 Z_{0-13} = 00010 A = 77777777	77777777_8 (stored in memory address 00010. Checked with next instruction).
CLA(f = 30)	F = 30_8 M = 00 Z_{0-13} = 00010	A = 77777777_8 (placed in memory address 00010 by STR instruction above).
ADD(f = 31)	F = 31_8 M = 00 A = 67777777_8 X = 01_8 (at T32 of R seq.)	A = 70000000_8
SHF(f = 06)	F = 06_8 M = 00 Z_{0-13} = 04006_8 A = 00770077	A = 77007700

5. Set computer to PHASE STEP through 00 (HLT) instructions. The P-register advances to 01777 through the first instruction but fails to advance to 02000. The advance from 01777 to 02000 requires that bit 10 set and bits 0 through 9 clear.

6. Check P-register logic schematics (figures 8-24, 8-25, and 8-26, pages 8-57, 8-59, and 8-61). P_{10} is set by either of two gates, adder or D-register.

7. Since register failed when used with adder, check adder gate on bit 10.

8. To enable the gate, set master clock Ø1 and ground test point A2A1TB1 B33 (output of term 07N02, figure 8-24, page 8-57).

9. Simulate the output of adder term 70A10 by grounding test points A1A1TB1 B17 and A1A1TB2 A6. Indicator-switch P_{10} is not lighted. Malfunction is in term 0XP10.

10. De-energize computer (see paragraph 3-7, page 3-22).

11. Open logic drawer A1.

12. Remove and replace 71760 card at A1A1J8D.

13. Close logic drawer.

14. Energize computer (see paragraph 3-2, page 3-16) and repeat steps 8 and 9.

15. Remove jumpers used for grounding in steps 8 and 9.

16. Repeat steps 4 and 5. P-register advances without error; malfunction is corrected.

III - ADJUSTMENTS

6-5. MEMORY CIRCUITS. - The read and write drive currents switch magnetic field direction in the ferrite cores in the memory stacks. The inhibit currents prevent this switching during the write cycle when zeros are written. High read or write currents usually cause a random pickup of bits, low currents usually cause a random dropping of bits.

Note: - Before adjusting memory current, make sure no failure, intermittent, or marginal conditions exist in the associated memory and computer logic circuits. Do not adjust memory currents or read strobe timing until the equipment has been energized for at least four hours.

a. Initial Setup.

1. Open memory drawer and install memory chassis extender cables (see paragraph 5-4a, page 5-4).

   Note: - The extender cables must not be used while operating.

2. Clear memory using the following procedure.

   1) Press RUN MODE switch.

   2) Momentarily place MASTER CLEAR switch to down position.

   3) Place FUNCTION REPEAT switch to up position.

   4) Set F-register to 01000_2.

   5) Place RESTART/START-STEP switch to START-STEP.

   6) Press SEQ STOP/STOP switch to STOP.

3. Store 77777777_8 at alternate addresses throughout memory using the following procedure.

   1) Momentarily place MASTER CLEAR switch to down position.

   2) Place FUNCTION REPEAT switch to up position.

   3) Set F-register to 01010_2.

   4) Set A to 7777777.

   5) Press and hold bit 0 of P-register while performing substeps 6) and 7).

   6) Place RESTART/START-STEP switch to START-STEP.

   7) Place SEQ STOP/STOP switch to STOP.

4. Ground test points A1A1TB2 A23 and C23.

Note: - Step 4 holds bits 13 and 12 of the P-register cleared. This reduces current repetition in the memory and stabilizes the oscilloscope presentation.

CAUTION. - Solid wires are used between the core stacks and the logic circuits. Do not bend or flex these wires.

5. Use the following oscilloscope settings.

Time/cm:	1 usec
Triggering mode:	EXT +, AC FAST
Trigger input:	A2A1TB1 G1 (02T11)

b. Inhibit Current Adjustment. - Use the following procedure to adjust the inhibit currents on both memory chassis.

1. Perform steps 1 through 4 of paragraph 6-5a, page 6-23 .

2. Place current probe around leads from A4J203-1 (figure 8-97, B1, page 8-209). Observe waveform A on figure 6-1, page 6-25.

3. Adjust the +V regulator potentiometer, R24 (figure 8-91, B3, page 8-197) to obtain 230 ±20% ma pulse (figure 6-1, page 6-25).

4. Connect oscilloscope probe to test point H27 (figure 8-97, B1, page 8-209) and record value obtained. It should be 2.3v ±10%. For further adjustments, this procedure and value of drive current can be used.

5. Place voltage scope probe at test point H27.

6. Adjust +V regulator potentiometer (figure 8-91, page 8-197) to obtain a 2.3v ± 10% pulse. Figure 6-1A, page 6-25, shows the approximate waveform. The pulse is the inhibit transformer primary current and is approximately 20 ma greater than the bit plane currents.

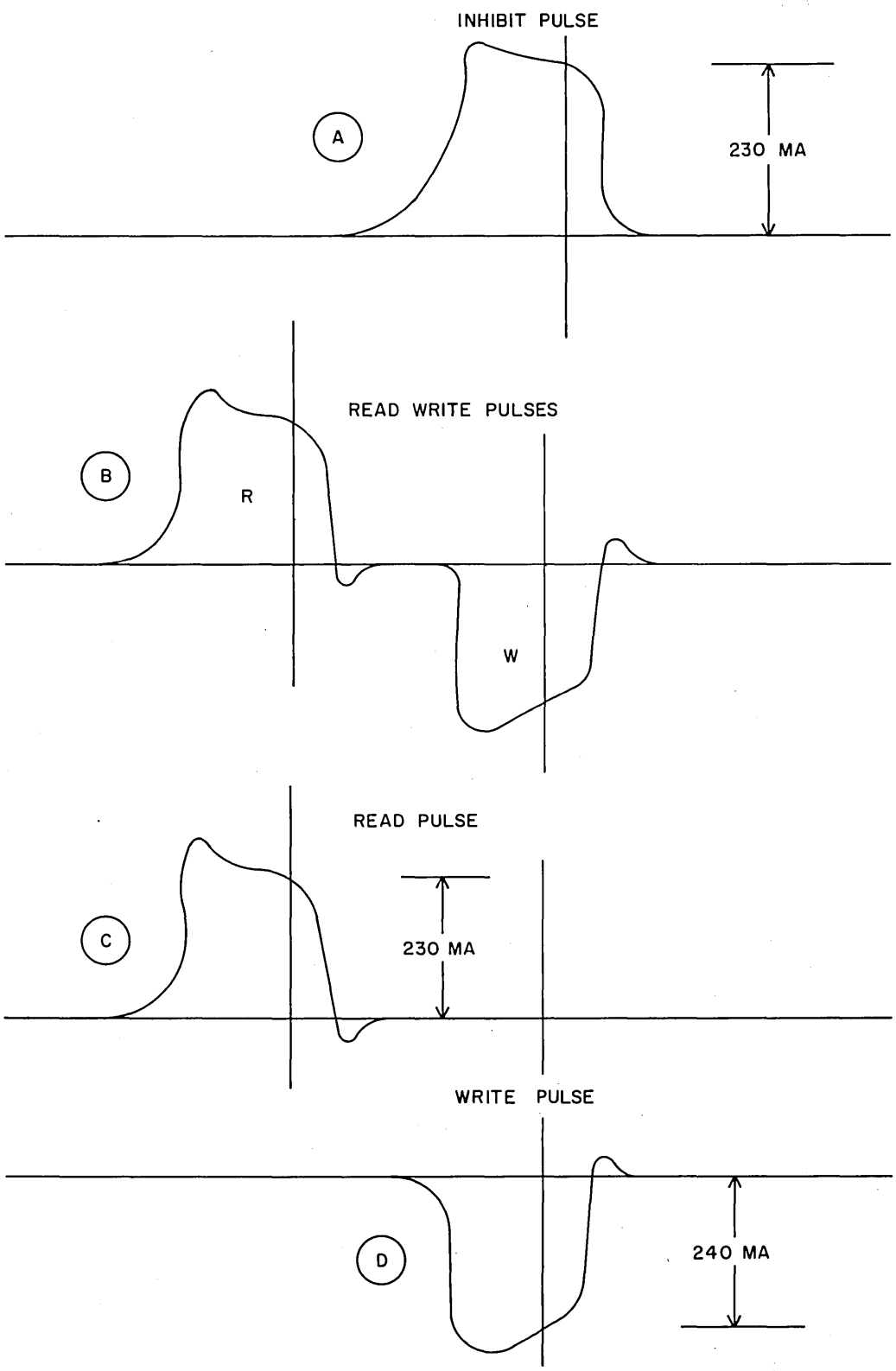


Figure 6-1. Memory Waveforms

c. X-Axis Read and Write Current Adjustment. - Use the following procedure to adjust the X read and write currents.

Note: - Adjust the inhibit current before adjusting the read and write current.

1. Perform steps 1 through 4 of paragraph 6-5a, page 6-23.

2. Place current probe around leads from J202-17 and J212-18 (figure 8-93, C4, page 8-201), observe waveform B on figure 6-1, page 6-25.

3. Adjust XR potentiometer (R22, figure 8-93, C6, page 8-201) to obtain a 230 ma read pulse (figure 6-1, C, page 6-25).

4. Connect scope probe to test point E27 and record value obtained. It should be 3.0v ± 10%. For further adjustments this procedure and value of drive current can be used.

5. Adjust XW potentiometer (R23, figure 8-93, B6, page 8-201) to obtain a 240 ma write pulse (figure 6-1, D, page 6-25).

6. Connect scope probe to test point D27 (figure 8-93, B6, page 8-201) and record value obtained. It should be 3.1v + 10%.

d. Y-Axis Read and Write Current Adjustments. - Use the following procedure to adjust Y read and write currents.

1. Perform steps 1 through 4 of paragraph 6-5a, page 6-23.

2. Place current probe around leads from J202-1 and J202-2 (figure 8-95, C4, page 8-205) and observe waveform B on figure 6-1 (page 6-25).

3. Adjust YR potentiometer (R20, figure 8-95, C6, page 8-205) to obtain 230 ±20% ma read pulse (figure 6-1, C, page 6-25).

4. Connect scope probe to test point G27 (figure 8-95, page 8-205 and record value obtained. It should be 3.1v ± 10%.

5. Adjust YW potentiometer (R21, figure 8-95, B6, page 8-205) to obtain a 240 ±20% ma write pulse (figure 6-1, D, page 6-25).

6. Connect scope probe to test point F27 and record value obtained. It should be 3.1v ± 10%.

If required, repeat procedures in paragraphs 6-5c and 6-5d, page 6-26, for the second memory chassis.

e. Memory to Z Strobe (Read Strobe) Adjustment. - An adjustable strobe pulse provides correction timing for the pulse which gates information from the memory sense amplifiers to the Z-register. An early strobe results in bits being picked up; a late strobe results in bits being dropped.

Note: - Before the strobe adjustment is made, make sure no failure, marginal, or intermittent conditions exist in the associated logic and memory circuitry.

1. Store 77777777_8 throughout memory.

2. Run a CLA (30) instruction continuously.

3. Use the following oscilloscope settings.

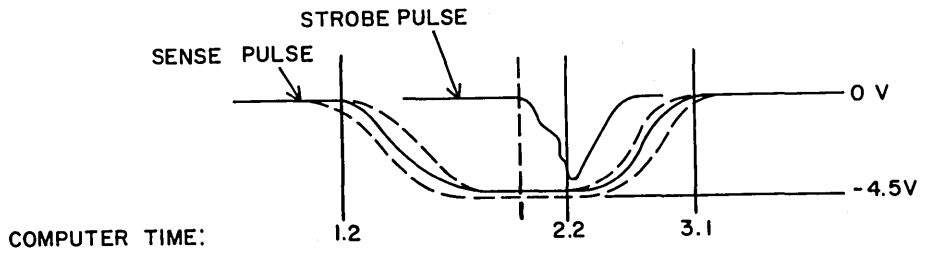
Time/cm:	0.1 μsec
Triggering mode:	EXT +, AC FAST
Trigger input:	A2A1TB1 G01 (02T11)

4. Insert channel A probe (dual-trace preamplifier) into A1A1TB1 G1 to display strobe pulse for Z_{0-13} (pulse for Z_{14-23} is identical when observed at A1A2TB2 A33). The strobe pulse is approximately 140 nanosecond at the -2v level.

5. If necessary, adjust strobe pulse on 64024 card (figure 8-54, B2, page 8-123) by increasing or decreasing total number of tap positions which separate initiations and terminating signals going to 64015 card.

6. Insert probe B into sense amplifier output test point (A20 to M20 on both memory chassis) which has narrowest pulse width.

7. Use an alternate dual-trace to compare sense output and timing of strobe. The strobe pulse occurs in the last half of the sense pulse.



8. To adjust strobe timing, move both initiating and terminating signal taps on 64024 card forward (earlier) or backward (later) an equal number of taps.

9. Run BRAINWASH memory test (refer to paragraph 10-3f, page 10-50, Volume IV). If errors occur in normal, high margin, or low margin, further adjustment is necessary.

10. Scope sense amplifiers of failing bits during BRAINWASH to check if strobe must be advanced and retarded in sense amplifier pulse.

6-6. AIRFLOW SENSOR ADJUSTMENT. - Perform the following steps to adjust the airflow sensor.

Note: - Make sure airflow sensor needs adjusting. Check fans and air intake and exhaust ports before making adjustment. Sensor operation is temperature dependent. If the ambient room temperature changes, sensor adjustment may be required.

1. Release snap screws on filter grill (above power control panel).

2. Pull grill work out and up to expose filter.

3. Remove air filter.

4. Place POWER ON/OFF switch to ON.

5. Loosen clamp and remove tape covering sensor adjustment screw hole.

6. Using a screwdriver, turn adjustment screw clockwise (switch operates at decreased airflow) 1/8 turn.

7. Replace tape covering the adjustment screw hole and tighten clamp.

   Note: - The hole for adjustment must be covered for the sensor to operate properly.

8. Replace air filter and close grill.

9. Open logic panel A1A3. The AIR FLOW FAULT indicator is lighted.

CHAPTER 7

ILLUSTRATED PARTS BREAKDOWN

I - INTRODUCTION

7-1. EXPLANATION. - The Illustrated Parts Breakdown identifies assemblies and detail parts contained in the CP-818A/U Digital Data Computer. The parts list should not be used for disassembly or assembly procedures. Maintenance, overhaul, or repair should be performed by authorized personnel using the applicable maintenance, service, or overhaul instructions. This publication is divided into three sections.

II - GROUP ASSEMBLY PARTS LIST

7-2. EXPLANATION. - The group assembly parts list consists of exploded view illustrations and listings of assemblies and detail parts. Each assembly listed in this section is followed by its component parts listing. Attaching parts are listed immediately following the assembly or part which they secure. The symbol "---*---" is used to denote the end of the attaching parts.

7-3. FIGURE AND INDEX COLUMN. - This column shows the chapter number, a figure number of an assembly and all index numbers assigned to its component parts.

7-4. REFERENCE DESIGNATION COLUMN. - This column lists the reference designator assigned to the assembly or detail part. These designators coincide with the designation marked on the equipment, drawings, and diagrams. The designator complies with MIL-STD-16.

7-5. DESCRIPTION COLUMN. - This column lists the item name of a part or assembly, followed by an identifying description, when required. The data is indented to show relationship. Whenever parts are procured from a vendor, the vendor's part number is listed in the Part Number column and the vendor's code "(ØØØØØ)" is placed after the description of the item. The Department of Defense drawing number is also listed after the vendor code number. The vendor's code number is taken from the Federal Supply Code for Manufacturer's Cataloging Handbook H4-1. These codes are listed in numerical sequence at the end of the Introduction.

7-6. PART NUMBER COLUMN - The column lists the Department of Defense drawing numbers except when military part numbers are listed.

a. "No Number" Entry. - This entry indicates that a part number has not been assigned to the part or assembly. Reference to its next procurable item is made by indenture or explanation in the Description column.

b. "Coml' Entry. - This entry indicates that the part may be procured from normal commercial sources. Sufficient descriptive information is given to permit part procurement.

7-7. UNITS PER ASSEMBLY COLUMN. - This column indicates the quantity of parts per assembly. If an equipment contains two or more identical assemblies, or if similar assemblies have been combined in one illustration, this column will indicate the quantity of parts for one assembly only.

a. "NP" (Nonprocurable) Entry. - This designation is entered when a part or assembly is listed as a "No Number" in the Part Number column.

b. "AR" (As Required) Entry. - This designation is entered when a definite quantity is not specified.

c. "Ref" (Reference) Entry. - This designation is entered when the quantity of an assembly has been previously considered.

7-8. USABLE ON CODE COLUMN. - This column has not been employed in this Illustrated Parts Breakdown.

III - NUMERICAL INDEX

7-9. EXPLANATION. - This index lists all part numbers, figure and index numbers, and quantities listed in the group assembly parts list. The part numbers are arranged in alphanumeric sequence.

IV - REFERENCE DESIGNATOR INDEX

7-10. EXPLANATION. - This index lists all reference designations assigned in the group assembly parts list. The reference designations are arranged in alphanumeric sequence with the corresponding figure and index number and part number.

VENDORS' CODES

Code	Name and Address
ØØ142	EFCO Hydraulics Inc. 235 Kilvent St. Warwick, R. I. Ø2886
Ø1295	Texas Instruments Inc. 135ØØ North Central Expressway Dallas, Texas 75231
Ø266Ø	Amphenol Corp. 28Ø1 S. 25th Ave. Broadview, Ill. 6Ø153
Ø5236	Jonathan Mfg. Co. 72Ø E. Walnut Fullerton, Calif. 92632
Ø5581	A.G.I. Rubber Co. PO Box 898 Bridgeport, Conn. Ø66Ø1
Ø5587	Couch Ordnance Inc. North Quincy, Mass.
Ø7137	Transistor Electronics Corp. Hwy 169 - Co. Rd 18 P.O. Box 6191 Minneapolis, Minn. 55424
Ø88Ø6	General Electric Co. Miniature Lamp Dept. Nela Park, Cleveland, Ohio 44112
Ø9922	Burndy Corp. Richards Ave. Norwalk, Conn. Ø6852
12881	Metex Corp. 97Ø New Durham Road Edison, N.J. Ø8817

VENDORS' CODES (continued)

Code	Name and Address
156Ø5	Cutler-Hammer Inc. 42Ø1 N. 27th St. Milwaukee, Wis. 53216
16512	National Connector Corp. 921Ø Science Center Minneapolis, Minn. 55429
22526	Berg Electronics, Inc. New Cumberland, Pa. 17Ø7Ø
37942	Mallory P.R. and Co., Inc. 3Ø29 East Washington St. Indianapolis, Ind. 462Ø6
43766	Nice Ball Bearing Co. 3Øth and Harting Park Ave. Philadelphia, Pa. 1914Ø
56289	Sprague Electric Co. Marshall St. North Adams, Mass. Ø1247
7Ø674	ADC Products Inc. 64Ø5 Cambridge St. Minneapolis, Minn. 55426
71279	Cambridge Thermionic Corp. 445 Concord Ave. Cambridge, Mass. Ø2138
71286	Camloc Fastener Corp. 22 Spring Valley Rd. Paramus, N.J. Ø7652
714ØØ	Bussmann Mfg., Division of McGraw Edison 2536 W. University St. St. Louis, Mo. 63Ø17

VENDORS' CODES (continued)

Code	Name and Address
71468	ITT, Cannon Electric Inc. 32Ø8 Humbolt St. Los Angeles, Calif. 9ØØ31
71744	Chicago Miniature Lamp Works 4433 Ravenswood Ave. Chicago, Ill. 6Ø64Ø
72619	Dialight Corp. 6Ø Stewart Ave. Brooklyn, N.Y. 11237
72962	Elastic Stop Nut Corp. of America 233Ø Vauxhall Road Union, N.J. Ø7Ø83
738Ø3	Metals and Controls, Inc. Metallurgical Products Group 34 Forest St. Attleboro, Mass. Ø27Ø3
74545	Hubbell Harvey Inc. State St. and Bostwick Ave. Bridgeport, Conn. Ø66Ø2
78189	Shakeproof, Division of Illinois Tool Works, Inc. St. Charles Road Elgin, Ill. 6Ø12Ø
8ØØ23	Schott, Oscar A. Co., Inc. 5ØØ 11th Ave. S. Minneapolis, Minn. 55415
8Ø294	Bourns Inc. 12ØØ Columbia Ave. Riverside, Calif. 925Ø7

VENDORS' CODES (continued)

Code	Name and Address
82877	Rotron Mfg. Co., Inc. 7-9 Hasbrouck Lane Woodstock, N.Y. 12498
83Ø58	Carr Fastener Co. 238 Main St. Cambridge, Mass. Ø2142
9Ø536	Univac, Division of Sperry Rand Corp. Univac Park St. Paul, Minn. 55116
915Ø6	Augat, Inc. 33 Perry Ave. Attleboro, Mass. Ø27Ø3
91637	Dale Electronics, Inc. P.O. Box 6Ø9 Columbus, Nebr. 686Ø1
91886	Malco Mfg. Co., Inc. 4Ø25 W. Lake Chicago, Ill. 6Ø624
91929	Honeywell, Inc., Micro Switch Division Chicago and Spring Streets Freeport, Ill. 61Ø32
93929	G-V Controls, Inc. 81 Okner Parkway Livingston, N.J. Ø7Ø39
94144	Raytheon Co. 465 Centre St. Quincy, Mass. Ø2169
94222	South Chester Corp. Chester, Pa.

VENDORS' CODES (continued)

Code	Name and Address
96881	Thomson Industries, Inc. 1Ø29 Plandome Rd. Manhasset, N.Y. 11Ø3Ø

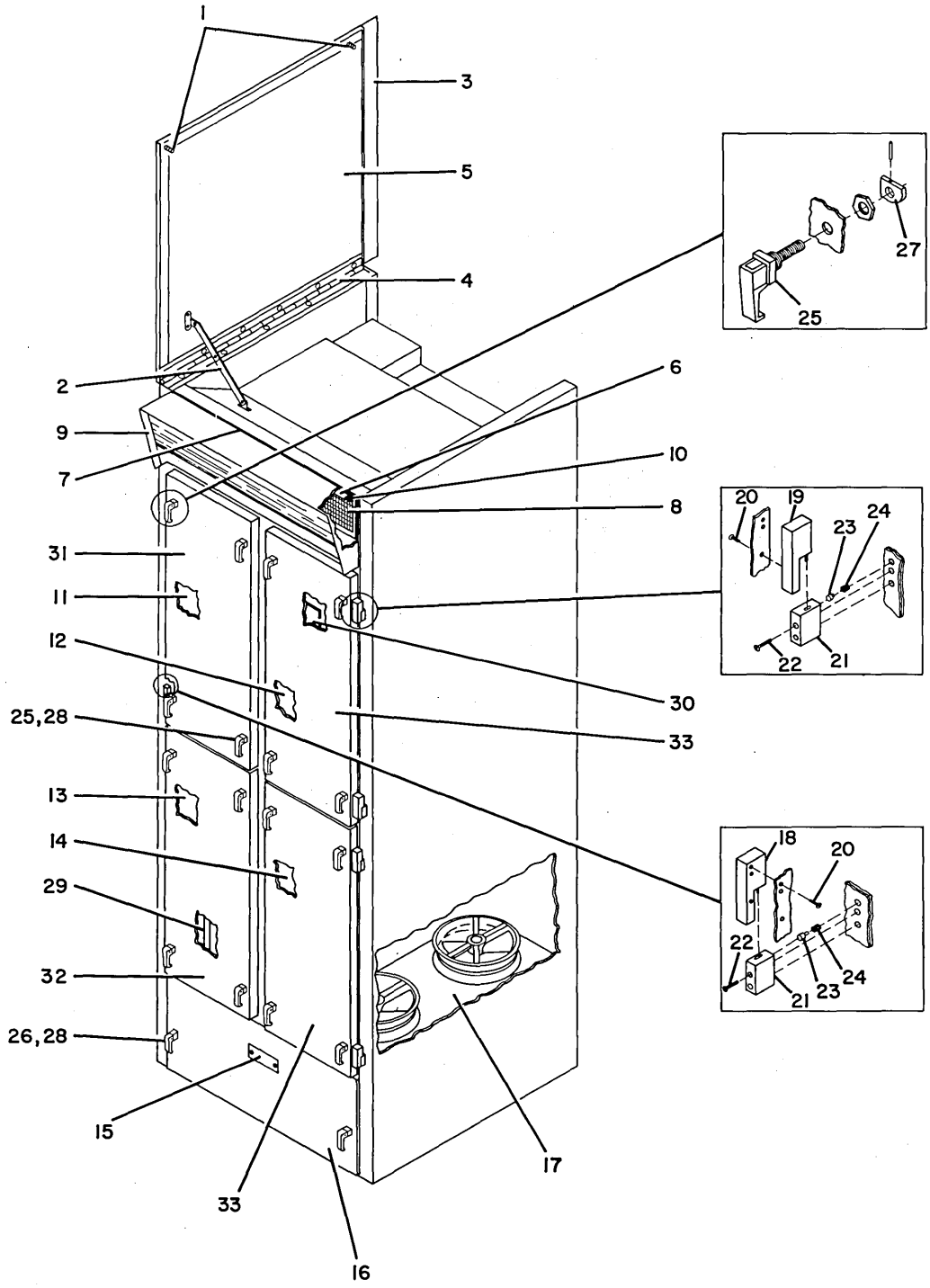


Figure 7-1. CP-818A/U Digital Data Computer

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-1-		COMPUTER, DIGITAL DATA	ØN116800	1	
		. COVER ASSEMBLY, cabinet	ØNØ68218-2	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 8-32UNC-2A by Ø.5 in. lg (DOD no. ØN123138-5)	Coml	5	
		. SCREW, pan hd, 6-32 UNC-2A by Ø.375 in. lg (DOD no. ØN123137-3)	Coml	1	
		. SPACER, sleeve	ØNØ67333	1	
		---*---			
-1		. . THUMBSCREW, ext rel body	ØNØ68251	2	
		(ATTACHING PARTS)			
		. . WASHER, flat, no. 8	MS15795-807	2	
		---*---			
-2		. . STAY, folding	ØNØ68192	1	
		(ATTACHING PARTS)			
		. . NUT, self-locking, hex	MS21044-C06	2	
		. . WASHER, flat, no. 6	MS15795-805	2	
		---*---			
-3		. . SKIN, extension	ØNØ68219-2	1	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 8-32UNC-2A by Ø.312 in. lg (DOD no. ØN123138-2)	Coml	6	
		. . WASHER, flat, no. 8	MS15795-807	6	
		---*---			
-4		. . HINGE, butt	ØNØ68238-2	1	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 8-32UNC-2A by Ø.312 in. lg (DOD no. ØN123138-2)	Coml	6	
		---*---			
-5		. . COVER, cabinet	ØNØ68133-2	1	
-6		. RETAINER, air filter	ØN116819	1	
-7		. SHIELDING, gasket, electronic	ØN123319-11	AR	
		(ATTACHING PARTS, for indexes 6 and 7)			
		. SCREW, ext rel body, 8-32UNC-2A by Ø.75 in. lg (81453) (DOD no. ØN123217-2)	CS-101	10	
		. WASHER, flat, no. 8	MS15795-807	10	
		. WASHER, lock, spring, no. 8	MS35338-137	10	
		---*---			
-8		. FILTER, air conditioning	ØN116812	1	
-9	A5	. HOOD ASSEMBLY (For breakdown see Figure 7-4, page 7-22)	ØN116816	1	
-10		. SHIELDING, gasket, electronic	ØN123319-10	AR	
		(ATTACHING PARTS, for indexes 9 and 10)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.625 in. lg (DOD no. ØN123137-6)	Coml	14	
		. WASHER, flat, no. 6	MS15795-805	14	
		---*---			
-11	A1	. CONVERTER, DIGITAL TO DIGITAL (For breakdown see Figure 7-5, page 7-26)	ØN116801-1	1	
-12	A2	. CONVERTER, DIGITAL TO DIGITAL (For breakdown see Figure 7-5, page 7-26)	ØN116801-2	1	
-13	A3	. MEMORY CHASSIS ASSEMBLY (For breakdown see Figure 7-6, page 7-32)	ØN116802-1	1	
-14	A4	. MEMORY CHASSIS ASSEMBLY (For breakdown see Figure 7-6, page 7-32)	ØN116802-2	1	

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-1-		(ATTACHING PARTS, for indexes 11 thru 14)			
		. SCREW, flat hd, ∅.312-18UNC-2A by 1 in. lg (DOD no. ∅N123131-3)	Coml	8	
		. SCREW, pan hd, ∅.312-18UNC-2A by ∅.5 in. lg (DOD no. ∅N123143-1)	Coml	8	
		. SPACER, sleeve, ∅.166 in. lg	∅N∅67∅62	8	
		---*---			
-15		. PLATE, identification (component of ∅N116826)	∅N116857-2	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 4-4∅UNC-2A by ∅.5 in. lg	MS51957-17	4	
		. WASHER, flat, no. 4	MS15795-8∅3	4	
		. NUT, self-locking, hex	MS21∅44-C∅4	4	
		---*---			
-16	PS1	. POWER SUPPLY (For breakdown see Figure 7-11, page 7-48)	∅N116826	1	
		(ATTACHING PARTS)			
		. SCREW, flat hd, 1∅-32UNF-2A by ∅.625 in. lg (DOD no. ∅N123394-4)	Coml	16	
		---*---			
-17	A6, A7	. FAN ASSEMBLY (For breakdown see Figure 7-12, page 7-52)	∅N116843	2	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 6-32UNC-2A by ∅.625 in. lg (DOD no. ∅N123137-6)	Coml	4	
		. SCREW, pan hd, 6-32UNC-2A by ∅.5 in. lg (DOD no. ∅N123137-5)	Coml	16	
		. WASHER, flat, no. 6	MS15795-8∅5	16	
		. NUT, self-locking, hex	MS21∅44-C∅6	16	
		---*---			
-18		. HINGE, upper, lh	∅N116841-1	4	
-19		. HINGE, upper, lh	∅N116463-1	4	
		(ATTACHING PARTS, for indexes 18 and 19)			
-2∅		. SCREW, flat hd, 8-32UNC-2A by ∅.375 in. lg (DOD no. ∅N123126-1)	Coml	24	
		---*---			
-21		. HINGE, lower	∅N11684∅	8	
		(ATTACHING PARTS)			
-22		. SCREW, flat hd, 8-32UNC-2A by 1.25 in. lg (DOD no. ∅N123126-9)	Coml	16	
		---*---			
-23		. PLUNGER, hinge	∅N116854	8	
-24		. SPRING, hinge	∅N116859	8	
-25		. LATCH, rim clinching (94222) (DOD no. ∅N123197-1)	62-99-193-1∅	16	
-26		. LATCH, rim clinching	∅N116853-1	2	
-27		. PAWL, latch	∅N11685∅-1	8	
-28		. PAWL, latch	∅N11685∅-2	1∅	
-29		. WRENCH, chassis engaging	∅N116856	1	
-3∅		. PLATE, identification "WARNING," 1.74 in. by 3.6 in. (9∅536) (DOD no. ∅N123282)	79∅1489-∅∅	4	
-31		. DOOR, electrical equipment	∅N1168∅7-1	1	
-32		. DOOR, electrical equipment	∅N1168∅7-3	1	
-33		. DOOR, electrical equipment	∅N1168∅7-2	2	

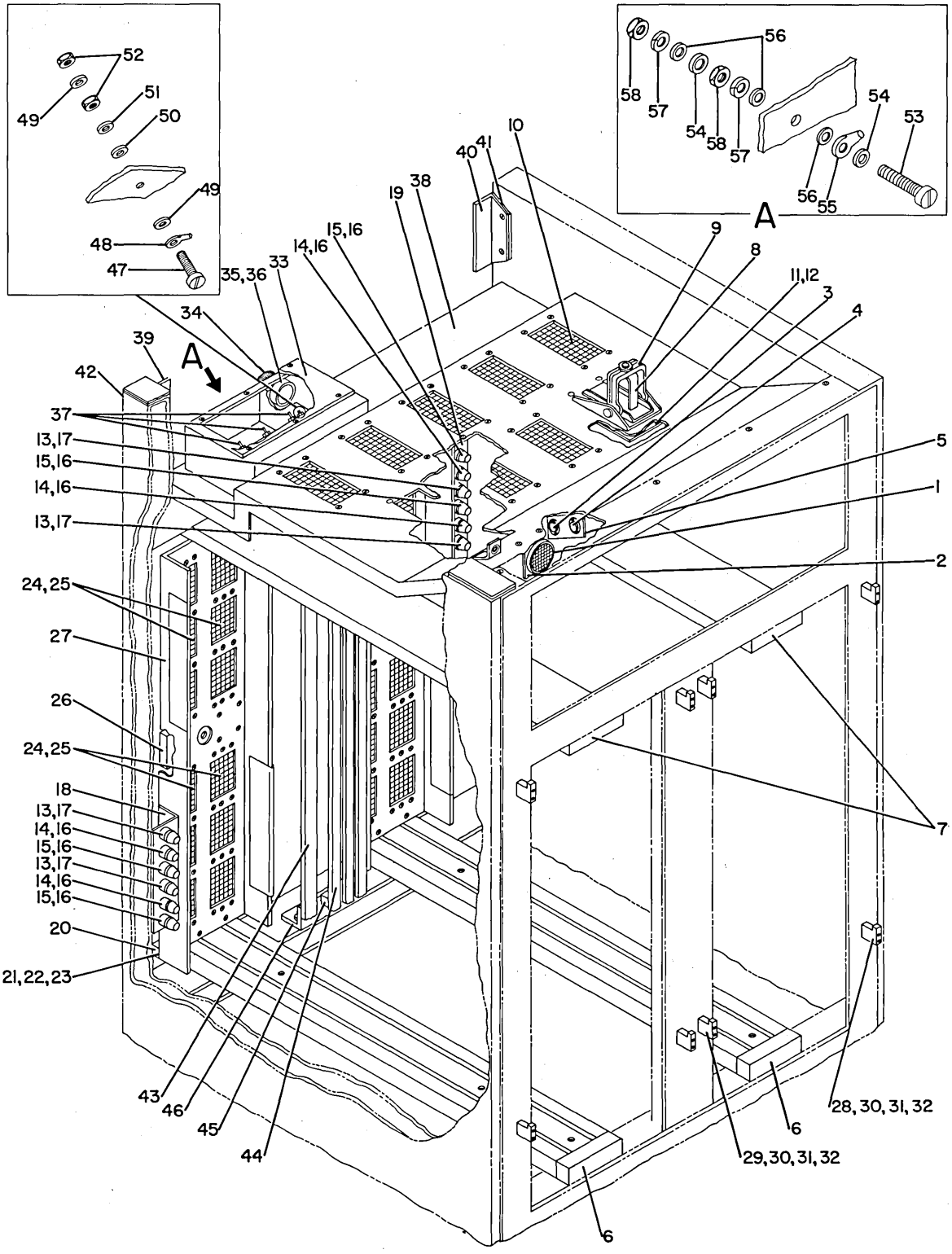


Figure 7-2. Upper Cabinet

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-2-		COMPUTER, DIGITAL DATA, upper cabinet	ØN1168ØØ	Ref	
-1	A5LS1	. HORN, electrical, solid state osc (37942) (component of ØN116816) (DOD no. ØN123233) . .	SC-628	1	
-2		. BRACKET, horn (component of ØN116816)	ØNØ682Ø4	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 8-32UNC-2A by Ø.438 in. lg (DOD no. ØN123138-4)	Coml	2	
		. WASHER, flat, no. 8	MS15795-8Ø7	2	
		---*---			
-3	S4	. SWITCH, thermostatic, spst (738Ø3) (DOD no. ØN123287-11)	M221F115Ø4Ø541	1	
-4	S5	. SWITCH, thermostatic, spst (738Ø3) (DOD no. ØN123287-1Ø)	M221L136Ø4Ø541	1	
		(ATTACHING PARTS, for indexes 3 and 4)			
		. SCREW, pan hd, 2-56UNC-2A by Ø.25 in. lg (DOD no. ØN1231Ø5-3)	Coml	4	
		. WASHER, flat, no. 2	MS15795-8Ø2	4	
		. NUT, self-locking, 2-56UNC-3B (72962) (DOD no. ØN123Ø22-1)	79LH166Ø-26	4	
		---*---			
-5		. BRACKET, thermostatic switch	ØN116448-2	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.375 in. lg (DOD no. ØN123137-3)	Coml	2	
		. WASHER, flat, no. 6	MS15795-8Ø5	2	
		. NUT, self-locking, hex	MS21Ø44-CØ6	2	
		---*---			
-6		. SLIDE, telescoping (Ø5236) (DOD no. ØN123216-1)	35Ø235-B	2	
-7		. SLIDE, telescoping (Ø5236) (DOD no. ØN123216-2)	35Ø235-T	2	
		(ATTACHING PARTS, for indexes 6 and 7)			
		. SCREW, flat hd, Ø.25-28UNF-2A by Ø.875 in. lg (DOD no. ØN123395-4)	Coml	12	
		. SHIM, steel, Ø.Ø16 in. thk by 3 in. lg	ØNØ67ØØ6	AR	
		. SHIM, steel, Ø.Ø31 in. thk by 3 in. lg	ØNØ67115	AR	
		. SHIM, steel, Ø.Ø62 in. thk by 3 in. lg	ØNØ67124	AR	
		. SHIM, steel, Ø.Ø16 in. thk by 3.5 in. lg	ØNØ67ØØ7	AR	
		. SHIM, steel, Ø.Ø31 in. thk by 3.5 in. lg	ØNØ67125	AR	
		. SHIM, steel, Ø.Ø62 in. thk by 3.5 in. lg	ØNØ67126	AR	
		---*---			
	A12	. CONNECTOR ASSEMBLY	ØNØ68228-2	1	
-8		. . COVER, connector hole	ØNØ67739	9	
-9		. . RETAINER, connector	ØNØ67ØØ5	9	
-1Ø	A12J2 thru A12J1Ø	. . CONNECTOR, receptacle, elect, male, 5Ø contact (71468) (DOD no. ØN123165)	DPD5Ø-34PIGF 32A115	9	
		(ATTACHING PARTS, for indexes 9 and 1Ø)			
		. . SCREW, flat hd, 6-32UNC-2A by Ø.625 in. lg (DOD no. ØN123125-5)	Coml	36	
		---*---			
-11		. . SHIELDING, gasket	ØNØ67322	9	
-12		. . PLATE, mounting elect conn	ØNØ681Ø2	9	
		(ATTACHING PARTS, for indexes 11 and 12)			
		. . SCREW, pan hd, 6-32UNC-2A by Ø.5 in. lg (DOD no. ØN123137-5)	Coml	36	
		. . WASHER, flat, no. 6	MS15795-8Ø5	36	
		---*---			
-13	A12A1F1, A12A1F4, A12A2F1, A12A2F4	. . FUSE, cartridge	FØ3A25ØV8AS	4	

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-2-14	A12A1F2, A12A1F5, A12A2F2, A12A2F5	. . FUSE, cartridge	FØ3A25ØV1ØAS	4	
-15	A12A1F3, A12A1F6, A12A2F3, A12A2F6	. . FUSE, cartridge	FØ2A25ØV3AS	4	
-16	A12A1XF2, A12A1XF3, A12A1XF5, A12A1XF6, A12A2XF2, A12A2XF3, A12A2XF5, A12A2XF6	. . FUSEHOLDER	FHL18G2-1	8	
-17	A12A1XF1, A12A1XF4, A12A2XF1, A12A2XF4	. . FUSEHOLDER, indicating, 2Ø amp, 4-6v (714ØØ) (DOD no. ØN123229)	HKU	4	
-18		. . BRACKET, angle, fuseholder	ØN116848-2	1	
-19		. . BRACKET, angle, fuseholder	ØN116848-1	1	
		(ATTACHING PARTS, for indexes 18 and 19)			
		. . SCREW, pan hd, 8-32UNC-2A by Ø.5 in. lg (DOD no. ØN123138-5)	Coml	6	
		---*---			
	A12A1, A12A2	. . CONNECTOR ASSEMBLY, electrical	ØNØ67Ø59-2	2	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 1Ø-32UNF-2A by 1.25 in. lg (DOD no. ØN123141Ø-8)	Coml	16	
		. . WASHER, flat, no. 1Ø	MS15795-8Ø8	16	
		. . WASHER, lock, spring, no. 1Ø	MS35338-138	16	
		---*---			
-2Ø		. . . SUPPORT, connector bracket	ØNØ672Ø3	2	
-21		. . . SHIM, Ø.Ø2 in. thk by 4.78 in. lg	ØNØ67128	AR	
-22		. . . SHIM, Ø.Ø32 in. thk by 4.78 in. lg	ØNØ67138	AR	
-23		. . . SHIM, Ø.Ø5 in. thk by 4.78 in. lg	ØNØ67139	AR	
		(ATTACHING PARTS, for indexes 2Ø thru 23)			
		. . . WASHER, flat, no. 8	MS15795-8Ø7	6	
		. . . NUT, self-locking, hex	MS21Ø44-CØ8	6	
		---*---			
-24	A12A1J1 thru A12A1J4, A12A2J1 thru A12A2J4	. . . CONNECTOR, receptacle, elect, male, 189 contact (91886) (DOD no. ØN123224)	3614875	4	
		(ATTACHING PARTS)			
		. . . WASHER, flat, no. 6	MS15795-8Ø5	16	
		. . . NUT, self-locking, hex	MS21Ø44-CØ6	16	
		---*---			
-25		. . . . CONTACT, elect, male, snap-in (91886) (DOD no. ØN123467-1)	361ØØ49-4	189	
-26		. . . NUT, plain, plate	ØN116625	1	
		(ATTACHING PARTS)			
		. . . SCREW, flat hd, 1Ø-32UNF-2A by 1.125 in. lg (DOD no. ØN123Ø64-2)	Coml	8	
		. . . WASHER, flat, no. 1Ø	MS15795-8Ø8	8	
		. . . NUT, self-locking, hex	MS21Ø44-C3	8	
		---*---			
-27		. . . BRACKET, electrical conn	ØNØ67Ø58	1	
-28		. CATCH, door latch	ØN116851-4	4	
-29		. CATCH, door latch	ØN116851-1	4	
-3Ø		. SHIM, catch	ØN116852-1	AR	

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-2-31		. SHIM, catch	ØN116852-2	AR	
-32		. SHIM, catch	ØN116852-3	AR	
		(ATTACHING PARTS, for indexes 28 thru 32)			
		. SCREW, flat hd, 8-32UNC-2A by 1 in. lg (DOD no. ØN123126-7)	Coml	8	
		. SCREW, flat hd, 8-32UNC-2A by 1.25 in. lg (DOD no. ØN123126-9)	Coml	8	
		---*---			
		. CABINET, electrical equipment	ØN116ØØ5	1	
-33		. . COVER, plate	ØNØ68152	1	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 6-32UNC-2A by Ø.5 in. lg (DOD no. ØN123137-5)	Coml	6	
		. . WASHER, flat, no. 6	MS15795-8Ø5	6	
		---*---			
-34		. . COVER, electrical connector	MS25Ø43-2ØC	1	
-35	J1	. . CONNECTOR, receptacle, elect	MS31Ø2A2Ø-15PW	1	
-36		. . SHIELDING, gasket, elect	ØNØ68132	1	
		(ATTACHING PARTS, for indexes 35 and 37)			
		. . SCREW, pan hd, 4-4ØUNC-2A by Ø.562 in. lg (DOD no. ØN123136-8)	Coml	4	
		. . WASHER, flat, no. 4	MS15795-8Ø3	4	
		. . NUT, self-locking, hex	MS21Ø44-CØ4	4	
		---*---			
-37	FL1, FL2, FL3	. . FILTER, radio interference, 4ØØ vdc, 2Ø amp (56289) (DOD no. ØN1232Ø2)	2ØJX31	3	
-38		. . BRACKET, electrical connector	ØNØ6823Ø-2	1	
		(ATTACHING PARTS)			
		. . SCREW, flat hd, 1Ø-32UNF-2A by Ø.625 in. lg (DOD no. ØN123394-4)	Coml	5	
		. . SCREW, pan hd, 1Ø-32UNF-2A by Ø.625 in. lg (DOD no. ØN12314Ø-4)	Coml	19	
		. . WASHER, flat, no. 1Ø	MS15795-8Ø8	19	
		---*---			
-39		. . BRACKET, stabilizer	ØN116863-1	1	
-4Ø		. . BRACKET, stabilizer	ØN116863-2	1	
-41		. . SHIELDING, gasket, electronic	ØN123363-34	AR	
		(ATTACHING PARTS, for indexes 39 thru 41)			
		. . SCREW, pan hd, 1Ø-32UNF-2A by Ø.75 in. lg (DOD no. ØN12314Ø-5)	Coml	4	
		. . WASHER, flat, no. 1Ø	MS15795-8Ø8	4	
		---*---			
-42		. . SHIELDING, gasket, electronic	ØN123319-17	AR	
-43	W1	. . BUS BAR, ground	ØNØ68212	1	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 6-32UNC-2A by Ø.562 in. lg (DOD no. ØN123137-9)	Coml	4	
		. . WASHER, flat, no. 6	MS15795-8Ø5	4	
		. . NUT, self-locking, hex, 6-32UNC-3B (72962) (DOD no. ØN123Ø44-2)	L79NKM-62	4	
		---*---			
-44	W2, W3, W4	. . BUS BAR	ØNØ68213	3	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 6-32UNC-2A by Ø.5 in. lg (DOD no. ØN123137-5)	Coml	12	
		. . WASHER, flat, no. 6	MS15795-8Ø5	12	
		---*---			
-45		. . INSULATOR, bus bar	ØNØ68136	2	

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 10-32UNF-2A by 0.438 in. lg (DOD no. 0N123140-2)	Coml	4	
		. . WASHER, flat, no. 10	MS15795-808	4	
		---*---			
-46		. . BRACKET, lower	0N116823-1	1	
		. . BRACKET, upper	0N116824-2	1	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 10-32UNF-2A by 0.5 in. lg (DOD no. 0N123140-3)	Coml	4	
		. . WASHER, flat, no. 10	MS15795-808	4	
		---*---			
-47		. SCREW, pan hd, 8-32UNC-2A by 0.75 in. lg (DOD no. 0N123133-3)	Coml	1	
-48		. TERMINAL, lug, insulated	MS25036-49	1	
-49		. WASHER, lock, no. 8 (DOD no. 0N123148-3)	Coml	2	
-50		. WASHER, flat, no. 8 (DOD no. 0N123147-3)	Coml	1	
-51		. WASHER, lock, spring, no. 8	AN935-B8L	1	
-52		. NUT, plain, hex, 8-32UNC-2B (DOD no. 0N123144-3)	Coml	2	
-53		. SCREW, cap, hex hd, full thd, 0.375-16UNC-2A by 2 in. lg (DOD no. 0N123274)	Coml	1	
-54		. WASHER, lock, 0.375 in. id	AN936-B616B	2	
-55		. TERMINAL, red, size 4 (00779) (DOD no. 0N123281-18)	322055	1	
-56		. WASHER, flat, brass, 0.375 in. id (DOD no. 0N123429)	Coml	3	
-57		. WASHER, lock, spring, 0.375 in. id	MS35338-141	2	
-58		. NUT, plain, hex, 0.375-16UNC-2B (DOD no. 0N123128-12)	Coml	2	

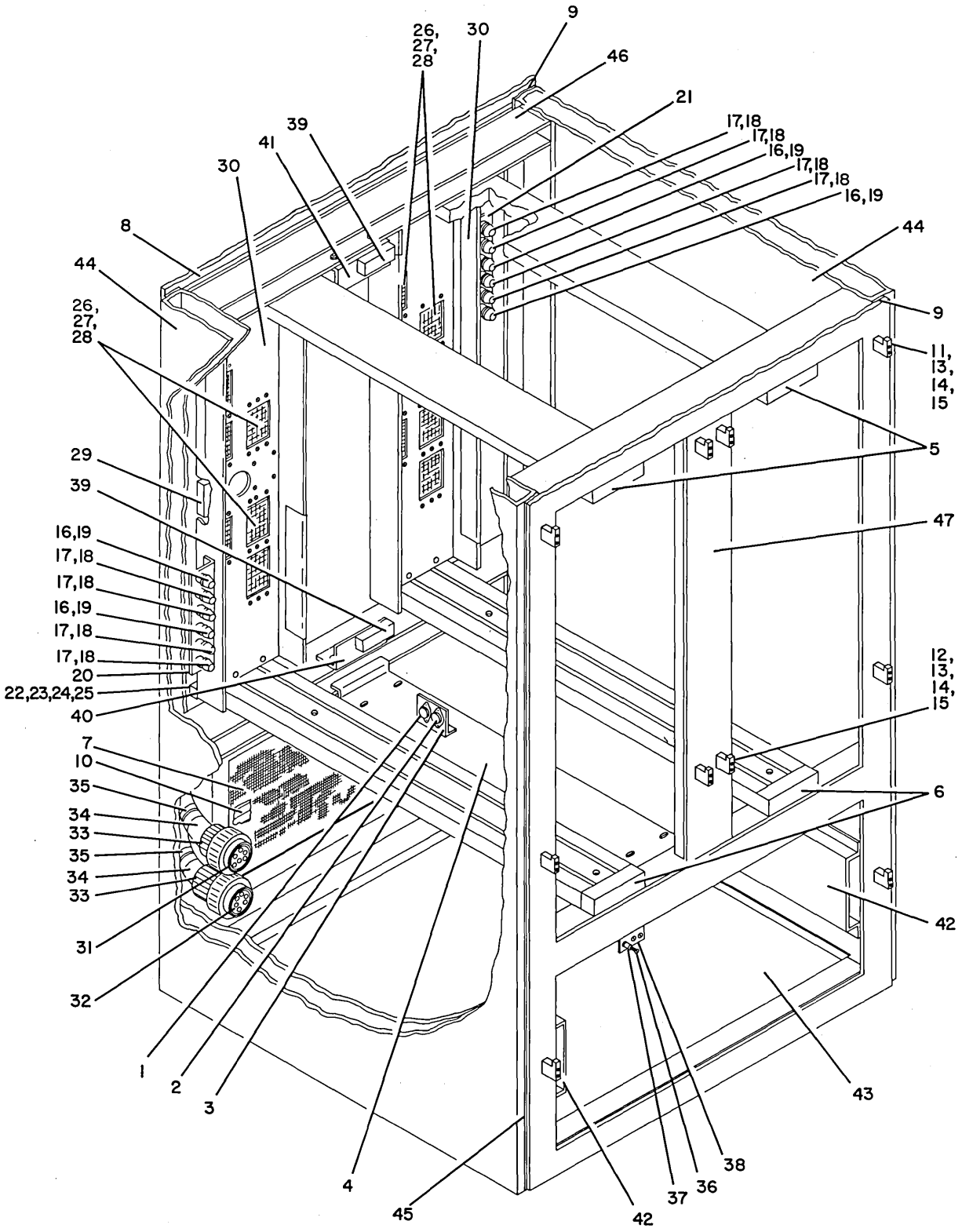


Figure 7-3. Lower Cabinet

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-3-		COMPUTER, DIGITAL DATA, lower cabinet	ØN1168ØØ	Ref	
-1	S2	. SWITCH, thermostatic, spst (738Ø3) (DOD no. ØN123287-11)	M221F115Ø4Ø541	1	
-2	S3	. SWITCH, thermostatic, spst (738Ø3) (DOD no. ØN123287-1Ø)	M221L136Ø4Ø541	1	
		(ATTACHING PARTS, for indexes 1 and 2)			
		. SCREW, pan hd, 2-56UNC-2A by Ø.25 in. lg (DOD no. ØN1231Ø5-3)	Coml	4	
		. WASHER, flat, no. 2	MS15795-8Ø2	4	
		. NUT, self-locking, 2-56UNC-3B (72962) (DOD no. ØN123Ø22-1)	79LH166Ø-26	4	
		---*---			
-3		. BRACKET, thermostatic switch	ØN116448-3	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.375 in. lg (DOD no. ØN123137-3)	Coml	2	
		. WASHER, flat, no. 6	MS15795-8Ø5	2	
		. NUT, self-locking, hex	MS21Ø44-CØ6	2	
		---*---			
-4		. BRACKET, mounting	ØN116832	1	
-5		. SLIDE, telescoping (Ø5236) (DOD no. ØN123216-2)	35Ø235-T	2	
-6		. SLIDE, telescoping (Ø5236) (DOD no. ØN123216-1)	35Ø235-B	2	
		(ATTACHING PARTS, for indexes 5 and 6)			
		. SCREW, flat hd, Ø.25-28UNF-2A by Ø.875 in. lg (DOD no. ØN123395-4)	Coml	12	
		. SHIM, steel, Ø.Ø16 in. thk by 3 in. lg	ØNØ67ØØ6	AR	
		. SHIM, steel, Ø.Ø31 in. thk by 3 in. lg	ØNØ67115	AR	
		. SHIM, steel, Ø.Ø62 in. thk by 3 in. lg	ØNØ67124	AR	
		. SHIM, steel, Ø.Ø16 in. thk by 3.5 in. lg	ØNØ67ØØ7	AR	
		. SHIM, steel, Ø.Ø31 in. thk by 3.5 in. lg	ØNØ67125	AR	
		. SHIM, steel, Ø.Ø62 in. thk by 3.5 in. lg	ØNØ67126	AR	
		---*---			
-7		. SHIELD, air vent, 7 in. by 2Ø.5 in (12881) (DOD no. ØN12321Ø-12)	Ø6-Ø32Ø2-To be est.	1	
-8		. SKIN, cabinet, rear	ØN116845	1	
-9		. SHIELDING, gasket, electronic	ØN123319-17	AR	
-1Ø		. COVER, louvered	ØN116828	1	
		(ATTACHING PARTS, for indexes 7 thru 1Ø)			
		. SCREW, pan hd, 1Ø-32UNF-2A by Ø.75 in. lg	MS51958-65	52	
		. SCREW, pan hd, 1Ø-32UNF-2A by 1 in. lg.	MS51958-67	26	
		. SCREW, pan hd, 1Ø-32UNF-2A by 1.25 in. lg	MS51958-68	2Ø	
		. WASHER, flat, no. 1Ø	MS15795-8Ø8	98	
		. NUT, self-locking, hex	MS21Ø44-C3	2Ø	
		---*---			
-11		. CATCH, door latch.	ØN116851-4	6	
-12		. CATCH, door latch.	ØN116851-1	4	
-13		. SHIM, catch	ØN116852-1	AR	
-14		. SHIM, catch	ØN116852-2	AR	
-15		. SHIM, catch	ØN116852-3	AR	
		(ATTACHING PARTS, for indexes 11 thru 15)			
		. SCREW, flat hd, 8-32UNC-2A by 1 in. lg (DOD no. ØN123126-7)	Coml	12	
		. SCREW, flat hd, 8-32UNC-2A by 1.25 in. lg (DOD no. ØN123126-9)	Coml	8	
		---*---			
	A12	. CONNECTOR ASSEMBLY	ØNØ68228-2	Ref	
-16	A12A3F1, A12A3F4, A12A4F1, A12A4F4	. . FUSE, cartridge	FØ3A25ØV8AS	4	

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
-17	A12A3F2, A12A3F3, A12A3F5, A12A3F6, A12A4F2, A12A4F3, A12A4F5, A12A4F6	. . FUSE, cartridge	F03A25V10AS	8	
-18	A12A3XF2, A12A3XF3, A12A3XF5, A12A3XF6, A12A4XF2, A12A4XF3, A12A4XF5, A12A4XF6	. . FUSEHOLDER	FHL18G2-1	8	
-19	A12A3XF1, A12A3XF4, A12A4XF1, A12A4XF4	. . FUSEHOLDER, indicating, 20 amp 4-6v (71400) (DOD no. 0N123229)	HKU	4	
-20		. . BRACKET, angle, fuseholder	0N116848-2	1	
-21		. . BRACKET, angle, fuseholder	0N116848-1	1	
		(ATTACHING PARTS, for indexes 20 and 21)			
		. . SCREW, pan hd, 8-32UNC-2A by 0.5 in. lg (DOD no. 0N123138-5)	Coml	6	
		---*---			
	A12A3, A12A4	. . CONNECTOR ASSEMBLY	0N06818-2	2	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 10-32UNF-2A by 1.25 in. lg (DOD no. 0N12314-8)	Coml	16	
		. . WASHER, flat, no. 10	MS15795-808	16	
		. . WASHER, lock, spring, no. 10	MS35338-138	16	
		---*---			
-22		. . . SUPPORT, connector bracket	0N06720 3	2	
-23		. . . SHIM, 0.02 in. thk by 4.78 in. lg	0N067128	4	
-24		. . . SHIM, 0.032 in. thk by 4.78 in. lg	0N067138	2	
-25		. . . SHIM, 0.05 in. thk by 4.78 in. lg	0N067139	2	
		(ATTACHING PARTS, for indexes 22 thru 25)			
		. . . NUT, self-locking, hex	MS21044-C08	6	
		. . . WASHER, flat, no. 8	MS15795-807	6	
		---*---			
-26	A12A3J1 thru A12A3J4, A12A4J1 thru A12A4J4	. . . CONNECTOR, receptacle, elect, 73 male and 4 female contact (91886) (DOD no. 0N123228)	3614679	4	
		(ATTACHING PARTS)			
		. . . NUT, self-locking, hex	MS21044-C06	16	
		---*---			
-27		. . . . CONTACT, elect, male, snap-in (91886) (DOD no. 0N123467-1)	3614792-4-36100013	73	
-28		. . . . CONTACT, elect, female, snap-in (91886) (DOD no. 0N123231-2)	3614791-4-36101 0W	4	
-29		. . . NUT, plain, plate	0N116625	1	
		(ATTACHING PARTS)			
		. . . SCREW, flat hd, 10-32UNF-2A by 1 in. lg (DOD no. 0N123394-7)	Coml	8	
		. . . NUT, self-locking, hex	MS21044-C3	8	
		---*---			
-30		. . . BRACKET, electrical connector	0N068181	1	
-31	A12P1	. . CONNECTOR, receptacle, elect	MS3106A32-6S	1	
-32	A12P2	. . CONNECTOR, receptacle, elect	MS3106A32-6SW	1	
-33		. . ADAPTER, cable to connector	MS3057-20A	2	
-34		. . BUSHING, elect conductor	MS39056-7	2	
-35		. . BAND, marker, black, 4.75 in. lg (DOD no. 0N12345)	Coml	2	

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-3-		. CABINET, electrical equipment	ØN1168Ø5	Ref	
-36		. . SCREW, pan hd, 6-32UNC-2A by Ø.5 in. lg (DOD no. ØN123137-5)	Coml	1	
-37	S1	. . SWITCH, push, interlock, 10 amp (91929) (DOD no. ØN122982)	2AC6	1	
		(ATTACHING PARTS)			
		. . SCREW, flat hd, 6-32UNC-2A by Ø.312 in. lg (DOD no. ØN123125-1)	Coml	2	
		---*---			
-38		. . BRACKET, interlock switch	ØN116861	1	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 6-32UNC-2A by Ø.312 in. lg (DOD no. ØN123137-2)	Coml	2	
		. . WASHER, flat, no. 6	MS15795-8Ø5	2	
		---*---			
-39		. . INSULATOR, bus bar	ØNØ68136	2	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 1Ø-32UNF-2A by Ø.438 in. lg (DOD no. ØN12314Ø-2)	Coml	4	
		. . WASHER, flat, no. 1Ø	MS15795-8Ø8	4	
		---*---			
-40		. . BRACKET, lower	ØN116823-2	1	
-41		. . BRACKET, upper	ØN116824-1	1	
		(ATTACHING PARTS, for indexes 4Ø and 41)			
		. . SCREW, pan hd, 1Ø-32UNF-2A by Ø.5 in. lg (DOD no. ØN12314Ø-3)	Coml	4	
		. . WASHER, flat, no. 1Ø	MS15795-8Ø8	4	
		---*---			
-42		. . BRACKET, telescoping slide	ØNØ6822Ø	2	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 1Ø-32UNF-2A by Ø.625 in. lg (DOD no. ØN12314Ø-4)	Coml	16	
		. . WASHER, flat, no. 1Ø	MS15795-8Ø8	16	
		---*---			
-43		. . COVER, cabinet, bottom	ØN116833	1	
		(ATTACHING PARTS)			
		. . SCREW, flat hd, 8-32UNC-2A by Ø.625 in. lg (DOD no. ØN123126-4)	Coml	4Ø	
		---*---			
-44		. . CABINET SIDE, elect equipment	ØNØ6819-2	2	
-45		. . SHIELDING, gasket, electronic	ØN123363-15	AR	
		(ATTACHING PARTS, for indexes 44 and 45)			
		. . SCREW, pan hd, 1Ø-32UNF-2A by Ø.75 in. lg (DOD no. ØN12314Ø-5)	Coml	88	
		. . WASHER, flat, no. 1Ø	MS15795-8Ø8	88	
		---*---			
-46		. . FRAME, electrical equipment	ØN116831	1	
-47		. . FRAME, electrical equipment	ØN11683Ø	1	

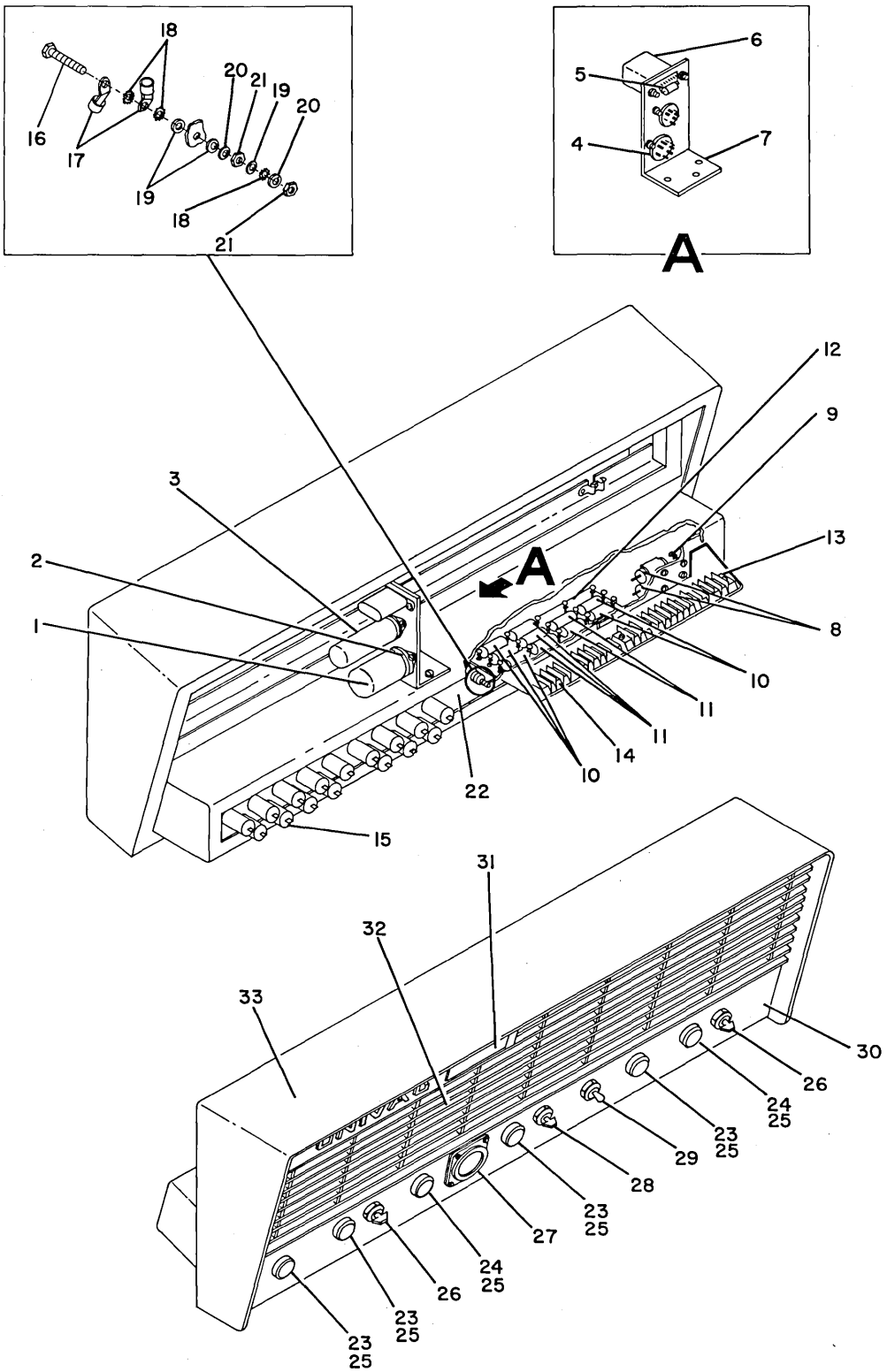


Figure 7-4. Hood Assembly

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-4-	A5	HOOD ASSEMBLY (For NHA see Figure 7-1, page 7-8)	ØN116816	Ref	
	A2	. SWITCH ASSEMBLY, airflow	ØN116846	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.375 in. lg (DOD no. ØN123137-3)	Coml	2	
		. WASHER, flat, no. 6	MS15795-8Ø5	2	
		---*---			
-1	A2K1	. . RELAY, thermal, 15 sec, 5ØØ-125Ø fpm (93929) (DOD no. ØN123276-2)	FS31Ø4	1	
-2		. . RETAINER, electron tube (915Ø6) (DOD no. ØN123Ø72)	251Ø-2	1	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 4-4ØUNC-2A by Ø.375 in. lg (DOD no. ØN123136-5)	Coml	1	
		. . WASHER, flat, no. 4	MS15795-8Ø3	1	
		---*---			
-3	A2K2	. . RELAY, thermal, 3Ø sec delay (93929) (DOD no. ØN123Ø19-1)	RF-6Ø-NC-115-6Ø	1	
-4	A2XK1	. . SOCKET, electron tube	TS1Ø3PØ3	1	
		(ATTACHING PARTS, for indexes 3 and 4)			
		. . SCREW, pan hd, 4-4ØUNC-2A by Ø.375 in. lg (DOD no. ØN123136-5)	Coml	4	
		. . WASHER, flat, no. 4	MS15795-8Ø3	4	
		. . NUT, self-locking, hex, 4-4ØUNC-3B (72962) (DOD no. ØN123Ø22-3)	79LH166Ø-4Ø	4	
		---*---			
-5	A2CR1	. . SEMICONDUCTOR DEVICE, diode (Ø7263)	1N4Ø86	1	
-6	A2K3	. . RELAY, armature, 25ØØ ohm, 2 spdt	RY4XX2B3L32	1	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 2-56UNC-2A by Ø.375 in. lg (DOD no. ØN1231Ø5-5)	Coml	2	
		. . WASHER, flat, no. 2	MS15795-8Ø2	2	
		. . NUT, self-locking, hex, 2-56 (72962) (DOD no. ØN123Ø12-3)	L79NM-26	2	
		---*---			
-7		. . BRACKET, angle, airflow switch	ØN116847	1	
-8	C1, C2	. CAPACITOR, fixed	CPØ9A1KC1Ø4K3	2	
-9		. TERMINAL, stud, insulated (71279) (DOD no. ØN123Ø78-1)	365Ø-1-Ø5	4	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 4-4ØUNC-2A by Ø.312 in. lg (DOD no. ØN123136-4)	Coml	4	
		. WASHER, flat, no. 4	MS15795-8Ø3	4	
		. WASHER, lock, spring, no. 4	MS35338-135	4	
		---*---			
	A1	. RESISTOR ASSEMBLY	ØNØ68147	1	
		(ATTACHING PARTS)			
		. SCREW, flat hd, 4-4ØUNC-2A by Ø.375 in. lg	ØN123124-3	2	
		. WASHER, flat, no. 4	MS15795-8Ø3	2	
		. NUT, self-locking, hex, 4-4ØUNC-3B (72962) (DOD no. ØN123Ø22-3)	79LH166Ø-4Ø	2	
		---*---			
-1Ø	A1R1, A1R4, A1R5, A1R8, A1R9	. . RESISTOR, fixed	RC32GF1ØØJ	5	
-11	A1R2, A1R3, A1R6, A1R7, A1R1Ø	. . RESISTOR, fixed	RC32GF681J	5	
-12		. . BRACKET, angle, resistor	ØNØ68247	1	
-13	TB2	. TERMINAL BOARD	26TB12	1	
-14	TB1	. TERMINAL BOARD	26TB8	1	

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-4-		(ATTACHING PARTS, for indexes 13 and 14)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.625 in. lg (DOD no. ØN123137-6)	Coml	4	
		. WASHER, flat, no. 6	MS15795-8Ø5	4	
		---*---			
-15	C3 thru C11, C13 thru C19	. CAPACITOR, fixed	CZ24BKF1Ø3	16	
-16	E1	. SCREW, pan hd, 8-32UNC-2A by Ø.875 in. lg (DOD no. ØN123133-4)	Coml	1	
-17		. TERMINAL, lug	MS25Ø36-53	2	
-18		. WASHER, lock, ext tooth, no. 8 (DOD no. ØN123148-3)	Coml	3	
-19		. WASHER, flat, no. 8 (DOD no. ØN123147-3)	Coml	3	
-2Ø		. WASHER, lock, spring, no. 8	AN935-B8L	2	
-21		. NUT, plain, hex, no. 8 (DOD no. ØN123144-3)	Coml	2	
-22		. BRACKET, electrical equipment	ØN11682Ø	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.375 in. lg (DOD no. ØN123137-3)	Coml	14	
		. WASHER, flat, no. 6	MS15795-8Ø5	14	
		---*---			
-23	XDS2 thru XDS5	. LIGHT, indicator, red lens (72619) (DOD no. ØN12329Ø-1)	81-Ø41Ø-Ø111-2Ø3	4	
-24	XDS1, XDS6	. LIGHT, indicator, green lens (72619) (DOD no. ØN12329Ø-2)	81-Ø41Ø-Ø112-2Ø3	2	
-25	DS1 thru DS6	. LAMP, incandescent, 18v, 15Ø ma (71744) (DOD no. ØN1232Ø7)	1826	6	
-26	S4, S5	. SWITCH, toggle, 2 pole, 3 position (91929) (DOD no. ØN1232Ø5-3)	13AT4Ø1-T2	2	
-27	M1	. METER, time totalizing	MS17325-1	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 4-4ØUNC-2A by Ø.312 in. lg	MS51957-14	4	
		. WASHER, flat, no. 4	MS15795-8Ø3	4	
		. NUT, self-locking, hex, 4-4ØUNC-3B (72962) (DOD no. ØN123Ø22-3)	79LH166Ø-4Ø	4	
		---*---			
-28	S1	. SWITCH, toggle, 2 pole, 3 position (91929) (DOD no. ØN1232Ø5-2)	13AT4Ø3-T2	1	
-29	S2	. SWITCH, toggle	MS35Ø59-21	1	
-30		. PANEL, control-indicator	ØN116821	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.375 in. lg (DOD no. ØN123137-3)	Coml	7	
		. WASHER, flat, no. 6	MS15795-8Ø5	7	
		---*---			
-31		. PLATE, identification	ØN116858-2	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 4-4ØUNC-2A by Ø.312 in. lg	MS51957-14	2	
		. WASHER, flat, no. 4	MS15795-8Ø3	2	
		---*---			
-32		. GRILL ASSEMBLY	ØN116818	1	
		(ATTACHING PARTS)			
		. SCREW, flat hd, 6-32UNC-2A by Ø.375 in. lg	MS51959-25	3	
		. NUT, self-locking, hex	MS21Ø44-CØ6	3	
		. STUD, turnlock, fastener (71286) (DOD no. ØN1232Ø3-4)	15S11-1AC-15S1-7-1AC	2	
		. SOCKET, pushbutton fastener (71286) (DOD no. ØN1232Ø4)	15R1-1AC-15R1Ø-1AC	2	
		---*---			
-33		. HOOD, cabinet	ØN116817	1	

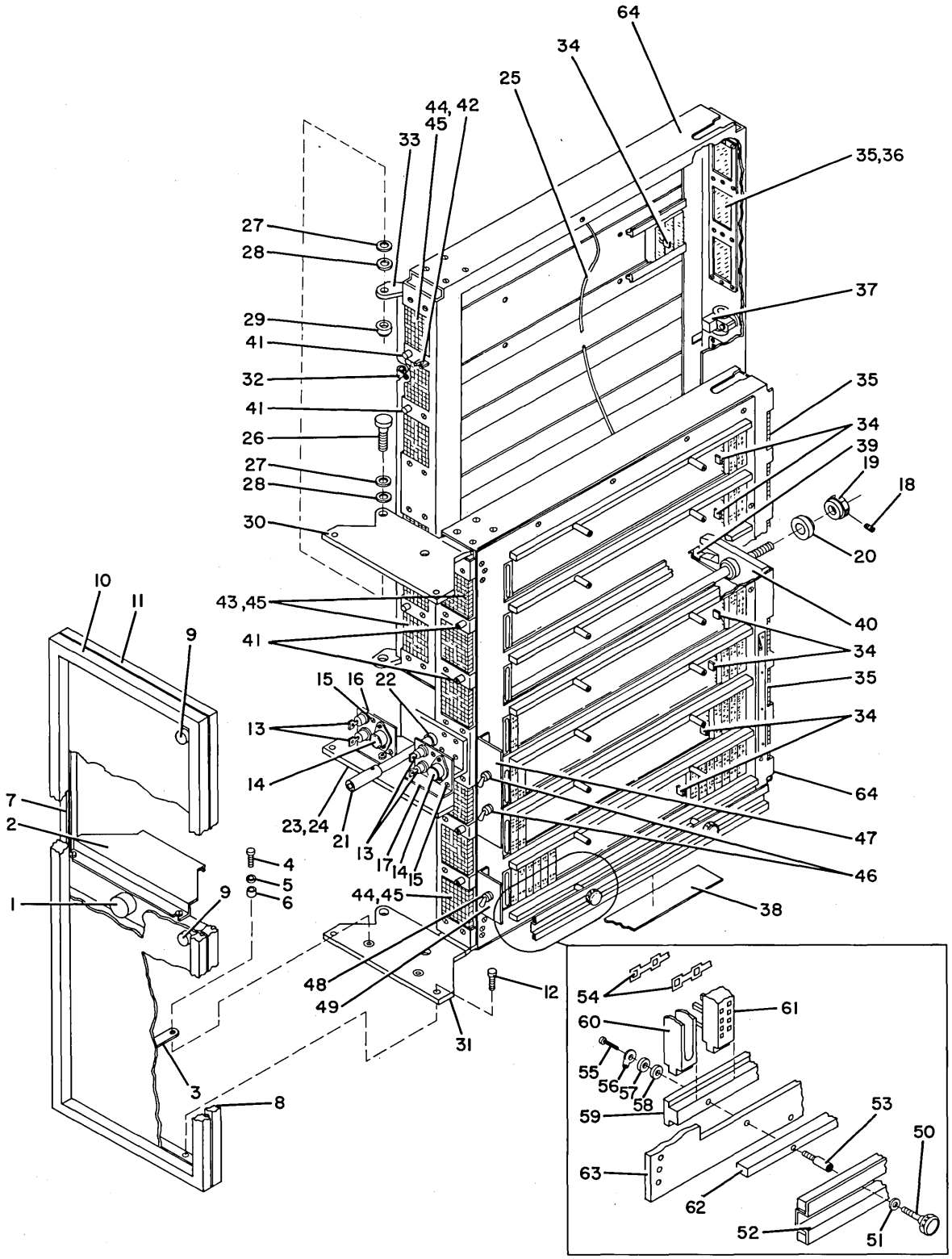


Figure 7-5. Digital to Digital Converter

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-5-	A1	CONVERTER, digital to digital (For NHA see figure 7-1, page 7-8)	ØN1168Ø1-1	Ref	
	A2	CONVERTER, digital to digital (For NHA see figure 7-1, page 7-8)	ØN1168Ø1-2	Ref	
-1		. CAP, end seal	ØNØ67Ø33	1	
-2		. SHIELD, semiconductor device	ØNØ681Ø5	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, Ø.25-2ØUNC-2A by Ø.5 in. lg (DOD no. ØN123141-1)	Coml	2	
		. WASHER, flat, Ø.25 in. id	MS15795-81Ø	2	
		---*---			
-3		. STAY, folding (used on A1)	ØNØ68192	1	
		. STAY, folding (used on A2)	ØNØ67Ø74	1	
		(ATTACHING PARTS)			
		. NUT, self-locking	MS21Ø444-CØ6	2	
-4		. SCREW, pan hd, 6-32UNC-2A by Ø.375 in. lg (DOD no. ØN123137-3)	Coml	1	
-5		. WASHER, flat, no. 6	MS15795-8Ø5	3	
-6		. SPACER, sleeve	ØNØ67333	1	
		---*---			
-7		. HINGE, butt	ØNØ67Ø18	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.375 in. lg (DOD no. ØN123137-3)	Coml	24	
		---*---			
-8		. SHIELDING, gasket, electronic	ØN123319-6	AR	
-9		. THUMBSCREW	ØN116671	3	
-1Ø	A3	. CONTROL-INDICATOR ASSEMBLY (used on A1) (For breakdown see figure 7-7, page 7-36)	ØN1168Ø6	1	
	A3	. CONTROL-INDICATOR ASSEMBLY (used on A2) (For breakdown see figure 7-8, page 7-40)	ØN11681Ø	1	
-11		. FRAME, panel	ØN116661	1	
		(ATTACHING PARTS)			
-12		. SCREW, cad, hex hd, Ø.25-2ØUNC-2A by Ø.625 in. lg	MS353Ø7-3Ø5	6	
		---*---			
-13	CR1, CR2, CR4, CR5	. SEMICONDUCTOR DEVICE, diode	1N1186	4	
-14	CR3, CR6	. SEMICONDUCTOR DEVICE, diode	1N28Ø4RB	2	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.438 in. lg (DOD no. ØN123137-4)	Coml	4	
		. WASHER, flat, no. 6	MS15795-8Ø5	4	
		. WASHER, lock, spring, no. 6	MS35338-136	4	
		---*---			
-15	XCR3, XCR6	. SOCKET, semiconductor device (915Ø6) (DOD no. ØN123177-1)	8Ø38-1G13	2	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 2-56UNC-2A by Ø.438 in. lg (DOD no. ØN1231Ø5-6)	Coml	4	
		. WASHER, flat, no. 2	MS15795-8Ø2	4	
		. WASHER, lock, spring, no. 2	MS35338-134	4	
		. NUT, plain, hex, no. 2	MS35649-249	4	
		---*---			
-16		. BRACKET, semiconductor device	ØNØ67Ø56	1	
-17		. BRACKET, semiconductor device	ØNØ67136	1	
		(ATTACHING PARTS, for indexes 16 and 17)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.625 in. lg (DOD no. ØN123125-5)	Coml	4	
		---*---			

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-5-18		. SETSCREW, hex, socket, 1Ø-32UNF-2A by Ø.25 in. lg	MS51Ø23-49	2	
-19		. NUT, plain	ØN116626	2	
-2Ø		. BEARING, ball (43766) (DOD no. ØN123188-6)	6Ø3-1/4	2	
-21		. LOCK ROD ASSEMBLY	ØN116627	1	
-22		. BEARING, sleeve, double flanged (96881) (DOD no. ØN123138-2)	8L2-FF	1	
-23		. BRACKET, chassis center	ØNØ67Ø55	1	
-24		. SPACER, plate, chassis	ØNØ68119	1	
		(ATTACHING PARTS, for indexes 23 and 24)			
		. SCREW, pan hd, 8-32UNC-2A by Ø.625 in. lg (DOD no. ØN123138-6)	Coml	4	
		. WASHER, flat, no. 6	MS15795-8Ø7	4	
		---*---			
-25		. CORD	ØNØ67325	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 8-32UNC-2A by Ø.5 in. lg (DOD no. ØN123126-3)	Coml	2	
		. NUT, self-locking	MS21Ø44-CØ8	2	
		---*---			
-26		. SCREW, shoulder	ØNØ68117	2	
-27		. WASHER, nonmetallic	ØNØ67Ø64	4	
-28		. WASHER, nonmetallic	ØNØ67249	4	
-29		. NUT, self-locking	MS1783Ø-4F	2	
-3Ø		. BRACKET, chassis, top	ØNØ67ØØ3	1	
-31		. BRACKET, chassis, bottom	ØNØ67Ø54	1	
		(ATTACHING PARTS for indexes 3Ø and 31)			
		. SCREW, flat hd, 1Ø-32UNF-2A by Ø.625 in. lg (DOD no. ØN123394-4)	Coml	8	
		---*---			
	A1	. LOGIC CHASSIS ASSEMBLY, LH (used on A1)	ØN1168Ø3-1	1	
	A1	. LOGIC CHASSIS ASSEMBLY, LH (used on A2)	ØN1168Ø3-2	1	
	A2	. LOGIC CHASSIS ASSEMBLY, RH (used on A1)	ØN116813-1	1	
	A2	. LOGIC CHASSIS ASSEMBLY, RH (used on A2)	ØN116813-2	1	
-32		. . CLAMP, loop, nylon (Ø9922) (DOD no. ØN122981-2) (used on A1A1 and A2A1)	HP-2N	6	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 6-32UNC-2A by Ø.625 in . lg (DOD no. ØN123137-6)	Coml	6	
		. . WASHER, flat, no. 6	MS15795-8Ø5	6	
		. . NUT, self-locking	MS21Ø44-CØ6	6	
		---*---			
-33		. . HINGE, chassis (used on A1A1 and A2A1)	ØNØ67Ø52	1	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 8-32UNC-2A by Ø.625 in. lg (DOD no. ØN123138-6)	Coml	9	
		. . WASHER, flat, no. 8	MS15795-8Ø7	9	
		---*---			
-34	A1C1 thru A1C42, A2C1 thru A2C42	. . CAPACITOR, fixed, ceramic dielectric, 25 vdc, Ø.47 uf (56289) (DOD no. ØN12317Ø-5)	5C11A9	42	
-35	A1P1, A1P2, A2P1, A2P2	. . CONNECTOR, receptacle, elect, 189 contacts (91886) (DOD no. ØN123225-1)	3614676	2	
		(ATTACHING PARTS)			
		. . SCREW, flat hd, 6-32UNC-2A by Ø.438 in. lg (DOD no. ØN123125-3)	Coml	16	
		---*---			
-36		. . . CONTACT, elect, female, 2 wire wrap, white (91886) (DOD no. ØN123231-2)	3614791-4-361ØØ1ØW	189	

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-5-37		. . BEARING, block (used on A1A1 and A2A1)	ØNØ68145	1	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, Ø.25-28UNF-2A by Ø.5 in. lg (DOD no. ØN123142-1)	Coml	2	
		. . WASHER, lock, spring, Ø.25 in. id	MS35338-139	2	
		. . WASHER, flat, Ø.25 in. id	MS15795-81Ø	2	
		. . SHIM	ØNØ682Ø3	1	
		. . SHIM	ØNØ682Ø6	1	
		---*---			
-38		. . SHIM (used on A1A2 and A2A2)	ØNØ672Ø2	1	
-39		. . CLIP, spring, tension (used on A1A2 and A2A2) . .	ØNØ68197	1	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 6-32UNC-2A by Ø.375 in. lg (DOD no. ØN123137-3)	Coml	2	
		. . WASHER, flat, no. 6	MS15795-8Ø5	2	
		. . WASHER, lock, no. 6	MS35338-136	2	
		---*---			
-4Ø		. . BEARING PLATE, lock rod (used on A1A2 and A2A2)	ØNØ68194	1	
		(ATTACHING PARTS)			
		. . SCREW, flat hd, 1Ø-32UNF-2A by Ø.625 in. lg (DOD no. ØN123394-4)	Coml	4	
		---*---			
-41		. . STUD, extension, 6-32UNC (Ø5587) (DOD no. ØN1231Ø1-3)	R1Ø9Ø	4	
-42		. . CLAMP, loop	ØNØ681Ø4	AR	
-43	A1TB1, A2TB1	. . TEST POINT ASSEMBLY, 264 cont (91886) (DOD no. ØN123295)	3617351	1	
-44	A1TB2, A2TB2	. . TEST POINT ASSEMBLY, 264 cont (91886) (DOD no. ØN123295-1)	No Number	1	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 6-32UNC-2A by Ø.438 in. lg (DOD no. ØN123137-4)	Coml	12	
		---*---			
-45		. . . CONTACT, elect, female, 1 wire wrap, white (91886) (DOD no. ØN123231-1)	3614798-2-361ØØ1ØW	264	
-46	A2S1, A2S2	. . SWITCH, toggle, dpdt (used on A1A2) (156Ø5) (DOD no. ØN123187-1)	8869-K4	2	
-47		. . BRACKET, angle, switch	ØNØ68151	1	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 8-32UNC-2A by Ø.625 in. lg (DOD no. ØN123138-6)	Coml	2	
		---*---			
-48	A2S1	. . SWITCH, toggle, dpdt (used on A2A2) (156Ø5) (DOD no. ØN123187-1)	8869-K4	1	
-49		. . BRACKET, angle, switch (used on A2A2)	ØN116842	1	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 8-32UNC-2A by Ø.25 in. lg (DOD no. ØN123138-6)	Coml	2	
		---*---			
-5Ø		. . THUMBSCREW	ØNØ67332	16	
-51		. . WASHER, lock, spring (DOD no. ØN123485-1) . . .	Coml	16	
-52		. . RETAINER, electronic circuit plug-in unit	ØNØ67Ø66	8	
-53		. . STUD, extension	ØNØ67Ø67	16	
		. . CONNECTOR ASSEMBLY (used on A1A1, A1A2 and A2A1)	ØNØ67Ø51-1	1	
		. . CONNECTOR ASSEMBLY (used on A2A2)	ØNØ67Ø51-2	1	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 8-32UNC-2A by Ø.438 in. lg (used on A1A1 and A1A2) (DOD no. ØN123138-4)	Coml	11	

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-5-		. . SCREW, pan hd, 8-32UNC-2A by Ø.438 in. lg (used on A1A2) (DOD no. ØN123138-4)	Coml	18	
		. . SCREW, pan hd, 8-32UNC-2A by Ø.438 in. lg (used on A2A2) (DOD no. ØN123138-4)	Coml	2Ø	
		---*---			
-54		. . . BUS BAR, chain, preformed (22526) (DOD no. ØN123176-1Ø)	4Ø829	28	
-55		. . . SCREW, pan hd, 6-32UNC-2A by 1.Ø in. lg	MS51957-34	64	
-56		. . . TERMINAL, lug	ØNØ68281	56	
-57		. . . WASHER, flat, no. 6	MS15795-8Ø5	64	
-58		. . . WASHER, lock, no. 6	MS35338-136	64	
-59		. . . RETAINER, electrical conn	ØNØ67Ø27	8	
-6Ø		. . . GROMMET, special shaped	ØNØ67Ø65	7	
-61	A1J1A thru A1J35A, A1J1B thru A1J35B, A1J1C thru A1J35C, A1J1D thru A1J35D, A1J1E thru A1J35E, A1J1F thru A1J35F, A1J1G thru A1J35G, A2J1A thru A2J35A, A2J1B thru A2J35B, A2J1C thru A2J35C, A2J1D thru A2J35D, A2J1E thru A2J35E, A2J1F thru A2J35F, A2J1G thru A2J35G	. . . CONNECTOR, receptacle, electrical, female (22526) (DOD no. ØN123189-2)	A2345-10	245	
-62		. . . NUT STRIP	ØNØ67Ø5Ø	8	
-63		. . . PANEL, mounting, elect conn (used on A1A1, A1A2 and A2A1)	ØNØ67Ø48-1	1	
		. . . PANEL, mounting, elect conn (used on A2A2)	ØNØ67Ø48-2	1	
-64		. . CHASSIS FRAME (used on A1A1, A1A2 and A2A1)	ØN1168Ø4-1	1	
		. . CHASSIS FRAME (used on A2A2)	ØN1168Ø4-2	1	

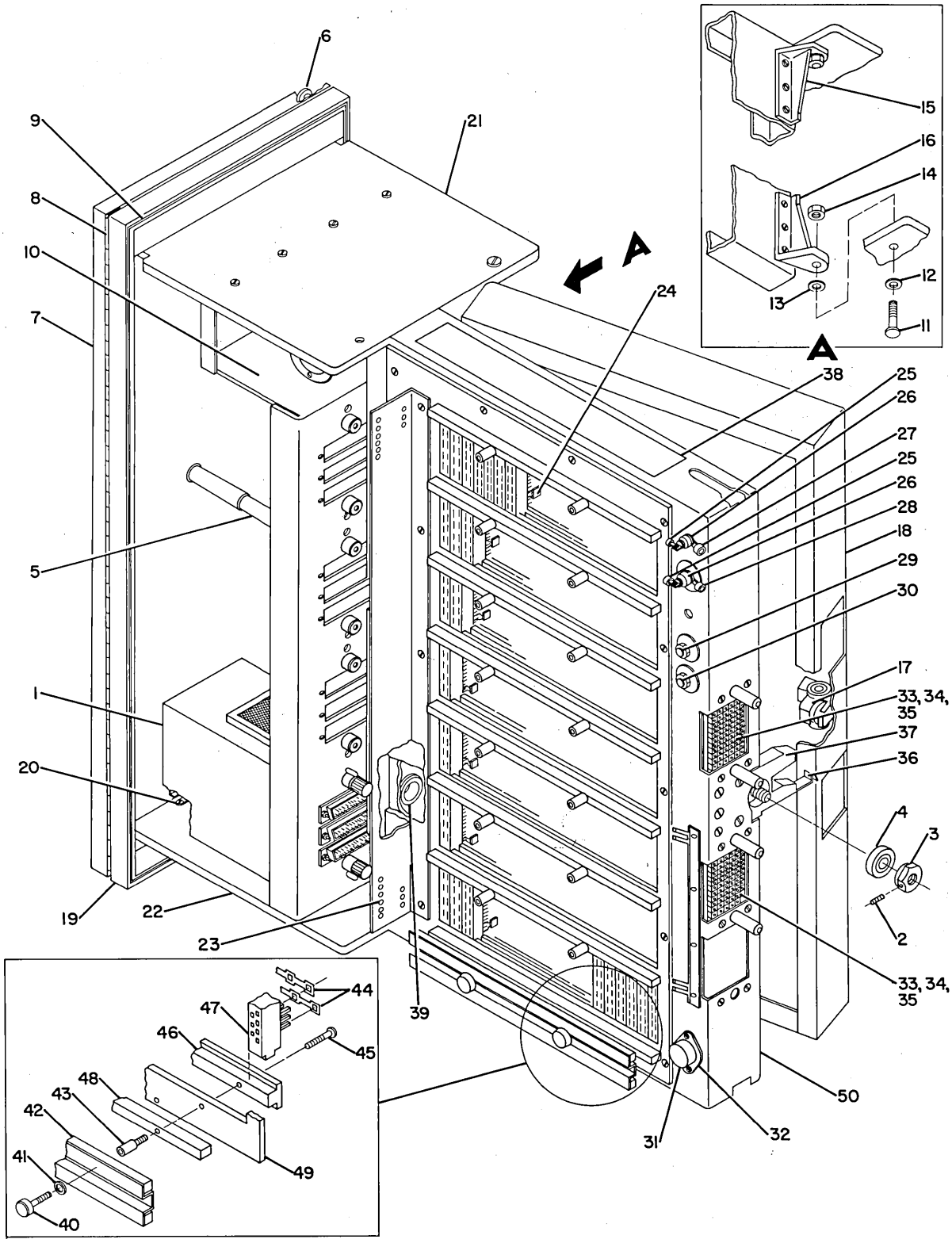


Figure 7-6. Memory Chassis Assembly

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-6-	A3	MEMORY CHASSIS ASSEMBLY (For NHA see figure 7-1, page 7-8)	ØN1168Ø2-1	Ref	
	A4	MEMORY CHASSIS ASSEMBLY (For NHA see figure 7-1, page 7-8)	ØN1168Ø2-2	Ref	
-1	A2Ø, A21, A22, A23	. CORE MEMORY STACK	ØNØ68229	4	
-2		. SETSCREW, hex, socket, 1Ø-32UNF-2A by Ø.25 in. lg	MS51Ø23-49	2	
-3		. NUT, plain, hex	ØN116626	2	
-4		. BEARING, ball (43766) (DOD no. ØN123188-6)	6Ø3-1/4	2	
-5		. LOCK ROD ASSEMBLY	ØN116627	1	
-6		. THUMBSCREW	ØN116671	2	
-7		. PANEL CONTROL-INDICATOR (used on A3)	ØN116814	1	
		. PANEL CONTROL-INDICATOR (used on A4)	ØN116815	1	
-8		. HINGE, butt	ØNØ67Ø18	1	
		(ATTACHING PARTS, for indexes 7 and 8)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.375 in. lg (DOD no. ØN123137-3)	Coml	24	
		---*---			
-9		. SHIELDING, gasket, electronic	ØN123319-6	AR	
-1Ø	A4	. PANEL, memory array stack (For breakdown see figure 7-9, page 7-44)	ØNØ68174	1	
		(ATTACHING PARTS)			
		. SCREW, flat hd, 8-32UNC-2A by Ø.625 in. lg (DOD no. ØN123136-4)	Coml	8	
		. SCREW, pan hd, 8-32UNC-2A by Ø.438 in. lg (DOD no. ØN123138-4)	Coml	4	
		. WASHER, flat, no. 8	MS15795-8Ø7	4	
		---*---			
	A1	. CHASSIS, blank	ØNØ68178	1	
		(ATTACHING PARTS)			
-11		. SCREW, shoulder	ØNØ68117	2	
-12		. WASHER, nonmetallic	ØNØ67Ø64	4	
-13		. WASHER, nonmetallic	ØNØ67249	4	
-14		. NUT, self-locking	MS1783Ø-4F	2	
		---*---			
-15		. . HINGE, chassis, upper	ØNØ68172	1	
-16		. . HINGE, chassis, lower	ØNØ68173	1	
		(ATTACHING PARTS, for indexes 15 and 16)			
		. . SCREW, pan hd, 8-32UNC-2A by Ø.625 in. lg (DOD no. ØN123138-6)	Coml	6	
		---*---			
-17		. . BEARING, block	ØNØ68145	1	
		(ATTACHING PARTS)			
		. . SCREW, flat hd, 1Ø-32UNF-2A by Ø.438 in. lg (DOD no. ØN123394-2)	Coml	1	
		. . SCREW, pan hd, Ø.25-28UNF-2A by Ø.5 in. lg (DOD no. ØN123142-1)	Coml	2	
		. . WASHER, lock, spring, Ø.25 in. id	MS35338-139	2	
		. . WASHER, flat, Ø.25 in. id	MS15795-81Ø	2	
		. . SHIM, copper	ØNØ682Ø3	1	
		. . SHIM, copper	ØNØ682Ø6	1	
		---*---			
-18		. . CHASSIS, blank	ØNØ68179	1	
-19		. FRAME, front panel, memory	ØN1168Ø8	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 1Ø-32UNF-2A by Ø.625 in. lg (DOD no. ØN12314Ø-4)	Coml	4	
		. SCREW, pan hd, 6-32UNC-2A by Ø.312 in. lg (DOD no. ØN123137-3)	Coml	1	
		. SPACER, sleeve	ØNØ67333	1	
		. WASHER, flat, no. 6	MS15795-8Ø5	1	
		---*---			

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-6-2Ø		. STAY, folding (used on A3)	ØNØ68192	1	
		. STAY, folding (used on A4)	ØNØ67Ø74	1	
		(ATTACHING PARTS)			
		. WASHER, flat, no. 6	MS15795-8Ø5	2	
		. NUT, self-locking	MS21Ø44-CØ6	2	
		---*---			
-21		. BRACKET, top	ØNØ6817Ø	1	
-22		. BRACKET, bottom	ØNØ68171	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 8-32UNC-2A by Ø.625 in. lg (DOD no. ØN123138-6)	Coml	8	
		---*---			
	A2	. MEMORY CHASSIS ASSEMBLY	ØNØ68165-2	1	
-23	A2A2	. . RESISTOR-CAPACITOR ASSEMBLY (For breakdown see figure 7-1Ø, page 7-46)	ØNØ68148	1	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 8-32UNC-2A by Ø.5 in. lg (DOD no. ØN123133-2)	Coml	5	
		. . WASHER, lock, external tooth, no. 8 (DOD no. ØN123148-3)	Coml	5	
		---*---			
-24	A2C1 thru A2C42	. . CAPACITOR, fixed, ceramic dielectric, 25 vdc, Ø.47 uf (56289) (DOD no. ØN12317Ø-5)	5C11A9	42	
-25		. . TERMINAL, lug, crimping	MS25Ø36-2	2	
-26	A2CR2, A2CR3	. . SEMICONDUCTOR DEVICE, diode	1N1186	2	
-27		. . TERMINAL, lug, crimping	MS25Ø36-5Ø	1	
-28		. . TERMINAL, lug, crimping	MS25Ø36-54	1	
-29	A2Q2	. . TRANSISTOR (Ø1295) (DOD no. ØN123214-1)	SP4167	1	
-3Ø	A2Q1	. . TRANSISTOR (Ø1295) (DOD no. ØN123213-1)	SP4166	1	
-31	A2CR1	. . SEMICONDUCTOR DEVICE, diode	1N28Ø4RB	1	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 6-32UNC-2A by Ø.5 in. lg (DOD no. ØN123137-5)	Coml	2	
		. . WASHER, lock, spring, no. 6	MS35338-136	2	
		---*---			
-32	A2XCR1	. . SOCKET, semiconductor device (915Ø6) (DOD no. ØN123177-1)	8Ø38-1G13	1	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 2-56UNC-2A by Ø.5 in. lg (DOD no. ØN1231Ø5-7)	Coml	2	
		. . WASHER, flat, no. 2	MS15795-8Ø2	2	
		. . WASHER, lock, spring, no. 2	MS35338-134	2	
		. . NUT, plain, hex, no. 2	MS35649-224	2	
		---*---			
-33	A2P1, A2P2	. . CONNECTOR, receptacle, elect, 77 contacts, 73 female, 4 male contacts (91886) (DOD no. ØN12323Ø-1)	361468Ø	2	
		(ATTACHING PARTS)			
		. . SCREW, flat hd, 6-32UNC-2A by Ø.5 in. lg (DOD no. ØN123125-4)	Coml	8	
		---*---			
-34		. . . CONTACTS, electrical, male (91886) (DOD no. ØN123467-1)	3614792-4-361ØØ13	4	
-35		. . . CONTACTS, electrical, female (91886) (DOD no. ØN123231-1)	3614798-2-361ØØ1ØW	73	
-36		. . CLIP, spring, tension	ØNØ68197	1	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 6-32UNC-2A by Ø.375 in. lg (DOD no. ØN123132-3)	Coml	2	
		. . WASHER, flat, no. 6	MS15795-8Ø5	2	
		. . WASHER, lock, spring, no. 6	MS35338-136	2	
		---*---			

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-6-37		. . BEARING PLATE	ØNØ68194-2	1	
		(ATTACHING PARTS)			
		. . SCREW, flat hd, 1Ø-32UNF-2A by Ø.75 in. lg (DOD no. ØN123394-5)	Coml	4	
		---*---			
-38		. . SHIM	ØNØ6816Ø	2	
-39		. . GROMMET, rubber, Ø.375 in. groove	MS35489-46	5	
-4Ø		. . THUMBSCREW	ØNØ67332	16	
-41		. . WASHER, lock, spring, high collar, no. 6 (DOD no. ØN123485-3)	Coml	16	
-42		. . RETAINER, electronic circuit	ØNØ68184	8	
-43		. . STUD	ØNØ68185	16	
	A2A1	. . CONNECTOR ASSEMBLY	ØNØ68166	1	
		(ATTACHING PARTS)			
		. . SCREW, pan hd, 8-32UNC-2A by Ø.5 in. lg (DOD no. ØN123138-5)	Coml	18	
		---*---			
-44		. . . BUS BAR, chain, preformed (22526) (DOD no. ØN123176-11)	473Ø9	28	
-45		. . . SCREW, pan hd, 6-32UNC-2A by 1.Ø in. lg	MS51957-34	4Ø	
-46		. . . RETAINER, electrical conn	ØNØ68122	8	
-47	A2A1J1A thru A2A1J22A, A2A1J1B thru A2A1J22B, A2A1J1C thru A2A1J22C, A2A1J1D thru A2A1J22D, A2A1J1E thru A2A1J22E, A2A1J1F thru A2A1J22F, A2A1J1G thru A2A1J22G	. . . CONNECTOR, receptacle, elect, female, 15 solder contacts (16512) (DOD no. ØN123189-2)	A2345-1Ø	154	
-48		. . . NUT STRIP	ØNØ68168	8	
-49		. . . PANEL, mounting, elect conn	ØNØ68167	1	
-50		. . CHASSIS FRAME	ØNØ68169	1	

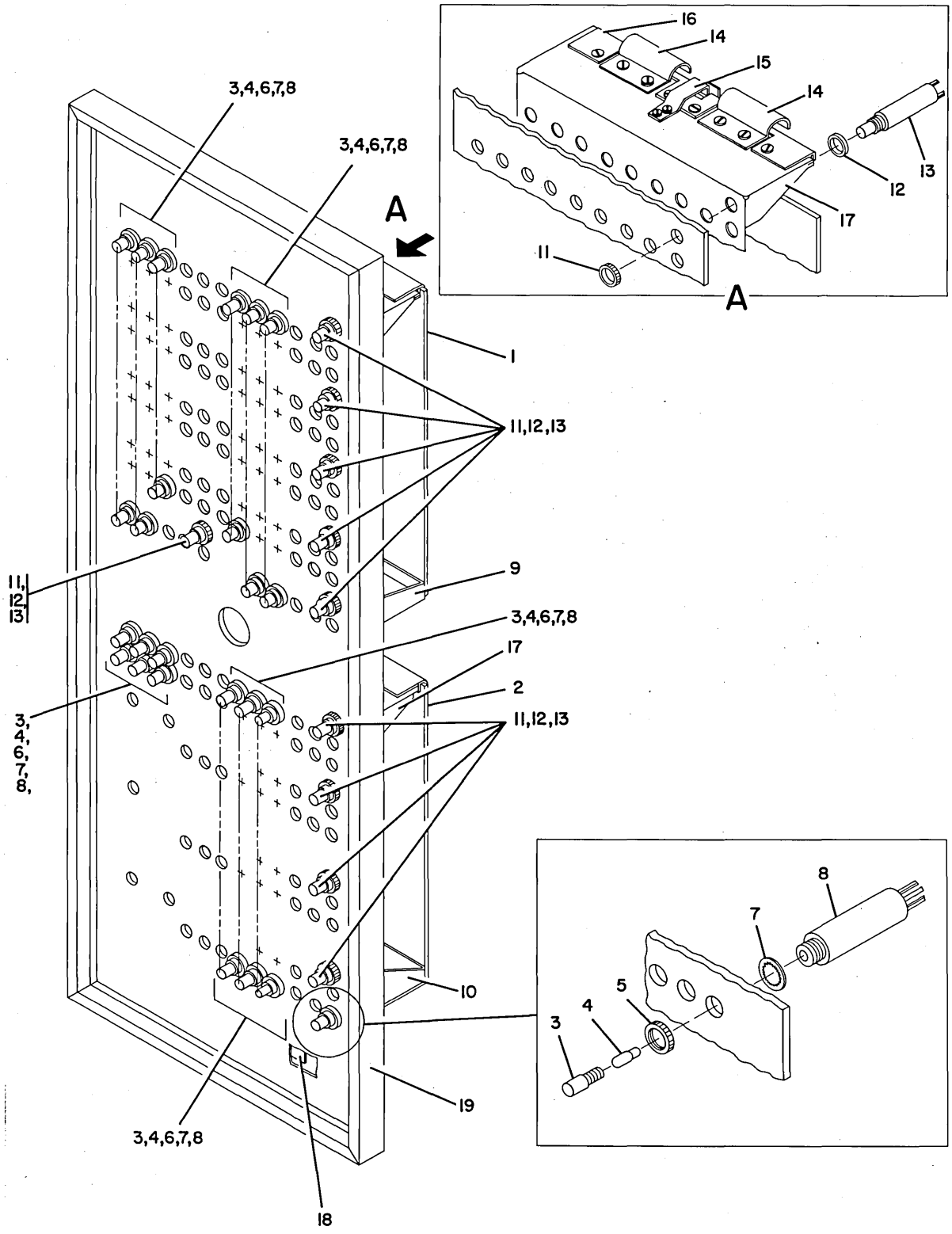


Figure 7-7. Control Indicator, A1A3

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-7-	A1A3	CONTROL-INDICATOR (For NHA see figure 7-5, page 7-26)	ØN1168Ø6	Ref	
-1		. SHIELDING, control-indicator	ØNØ68271	1	
-2		. SHIELDING, control-indicator	ØNØ6827Ø	1	
	XDS1A thru XDS1L, XDS2A thru XDS2L, XDS3A thru XDS3L, XDS4A thru XDS4L, XDS5A thru XDS5L, XDS6A thru XDS6L, XDS7A thru XDS7L, XDS8A thru XDS8L, XDS9A thru XDS9E, XDS9H thru XDS9L, XDS1ØA thru XDS1ØL, XDS11A thru XDS11L, XDS12A thru XDS12E, XDS12J, XDS12L, XDS13A thru XDS13I, XDS14A thru XDS14E, XDS14L, XDS15A thru XDS15I, XDS16A thru XDS16E, XDS16J, XDS16L, XDS17A thru XDS17G, XDS17I	. SWITCH, push, indicator type (72619) (DOD no. ØN123195)	9Ø8-1166-1634-526	177	
-3		. . LENS, indicator light, amber (72619) (DOD no. ØN123441-2)	ST1-6ØØØ-1633	1	
-4		. . LAMP, incandescent, 1Øv, Ø.Ø14 amp (Ø88Ø6) (DOD no. ØN12344Ø)	344	1	
-5		. . NUT, plain, round, black, 3/8-32NEF-2 (Ø7137) (DOD no. ØN123236-2)	1112-1	1	
-6		. . NUT, plain, round, clear, 3/8-32NEF-2 (Ø7137) (DOD no. ØN123236-1)	1112-2	1	
-7		. . WASHER, lock, external tooth, Ø.375 in. id (78189) (DOD no. ØN123446)	112Ø-12-CPDD	1	
-8		. . SWITCH, push, indicator type	No Number	NP	
-9		. SUPPORT, shield	ØNØ68255-1	1	
-1Ø		. SUPPORT, shield	ØNØ68255-2	1	
-11		. NUT, plain, round, clear, 3/8-32NEF-2 (Ø7137) (DOD no. ØN123236-1)	1112-2	1Ø	
-12		. WASHER, lock, internal tooth, Ø.375 in. id (78189) (DOD no. ØN123446)	112Ø-12-CPDD	1Ø	
-13	S1 thru S1Ø	. SWITCH, push, spdt, white button (Ø7137) (DOD no. ØN12325Ø-1)	MBS-S-1838A-9	1Ø	
-14		. RETAINER, electrical cable	ØNØ68257	2	
-15		. CLIP, spring tension	ØNØ68279	2	
		(ATTACHING PARTS, for indexes 14 and 15)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.312 in. lg (DOD no. ØN123137-2)	Coml	12	
		. WASHER, flat, no. 6	MS15795-8Ø5	12	
		---*---			
-16		. RETAINER, shield	ØNØ68256	2	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.312 in. lg (DOD no. ØN123137-2)	Coml	8	
		---*---			

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-7-17		. SUPPORT, shield	ØNØ68273	2	
-18		. BRACKET, angle, indicator	ØN116839	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.312 in. lg (DOD no. ØN123137-2)	Coml	2	
		. WASHER, flat, no. 6	MS15795-8Ø5	2	
		. NUT, self-locking	MS21Ø44-CØ6	2	
		---*---			
-19		. PANEL, control-indicator	ØN116836	1	

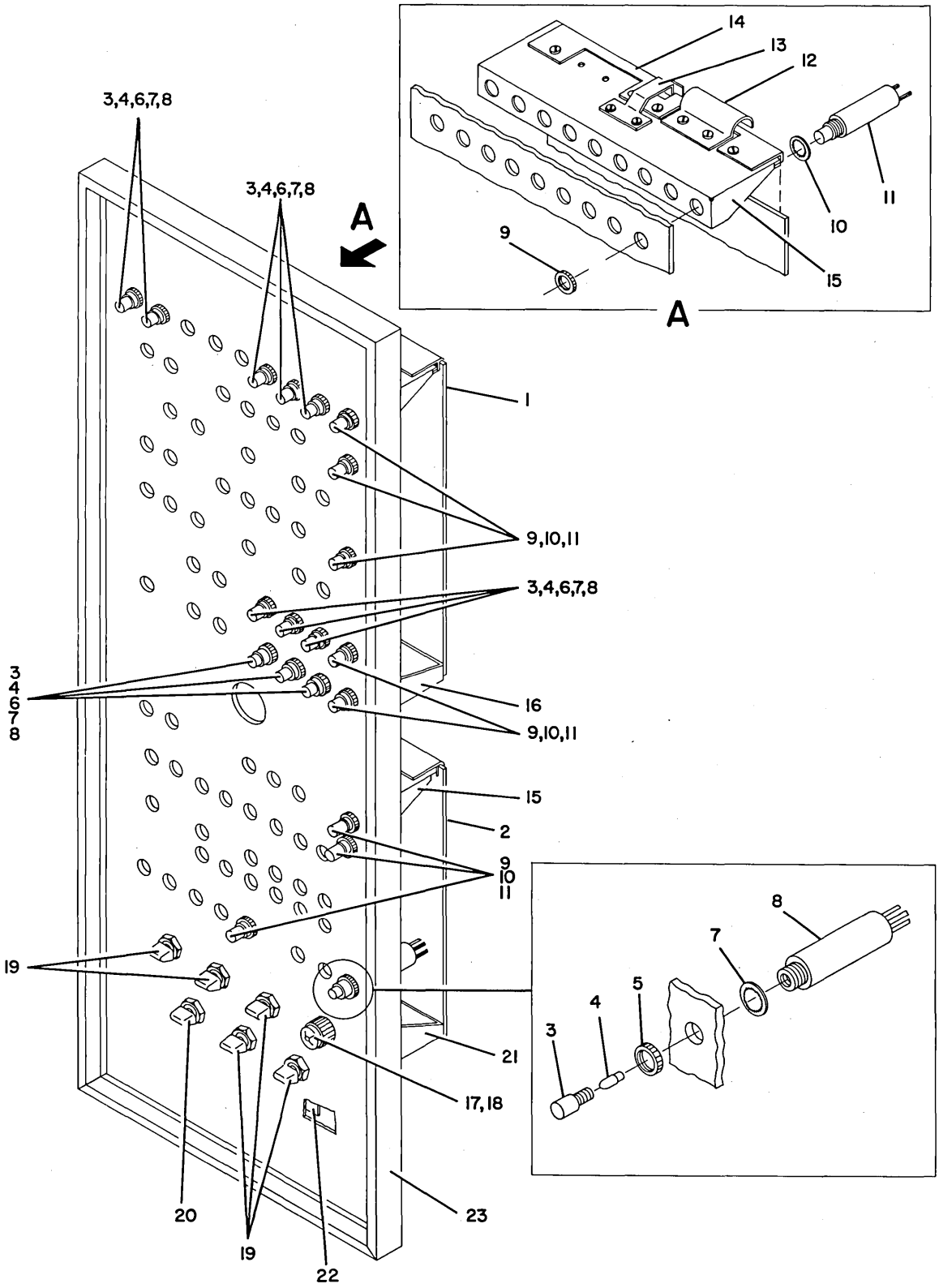


Figure 7-8. Control Indicator, A2A3

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-8-	A2A3A1	CONTROL-INDICATOR (For NHA see figure 7-5, page 7-26)	ØN11681Ø	Ref	
-1		. SHIELD, control-indicator	ØNØ6827Ø	1	
-2		. SHIELD, control-indicator	ØNØ68272	1	
	XDS1B thru XDS1I, XDS2C thru XDS2F, XDS2H, XDS2I, XDS3B, XDS3C, XDS3E, XDS3G, XDS3H, XDS4C thru XDS4F, XDS4H, XDS4I, XDS5B, XDS5C, XDS5E, XDS5G, XDS5H, XDS5I, XDS6B thru XDS6D, XDS6F, XDS6G, XDS7B thru XDS7D, XDS7F, XDS7G, XDS7I, XDS8C, thru XDS8E, XDS8H, XDS8I, XDS9A thru XDS9I, XDS1ØB thru XDS1ØE, XDS1ØG, XDS1ØI, XDS11B thru XDS11G, XDS12A thru XDS12C, XDS12F thru XDS12I	. SWITCH, push, indicator type	ØN123195-24	76	
-3		. . LENS, indicator light, amber (72619) (DOD no. ØN123441-2)	ST1-6ØØØ-1633	1	
-4		. . LAMP, incandescent, 10v, Ø.Ø14 amp (Ø88Ø6) (DOD no. ØN12344Ø)	344	1	
-5		. . NUT, plain, round, clear, 3/8-32NEF-2 (Ø7137) (DOD no. ØN123236-1)	1112-1	1	
-6		. . NUT, plain, round, black, 3/8-32NEF-2 (Ø7137) (DOD no. ØN123236-2)	1112-2	1	
-7		. . WASHER, lock, external tooth, Ø.375 in. id (78189) (DOD no. ØN123446)	112Ø-12-CPDD	1	
-8		. . SWITCH, push, indicator type	No Number	NP	
-9		. NUT, plain, round, clear, 3/8-32NEF-2 (Ø7137) (DOD no. ØN123236-1)	1112-2	8	
-1Ø		. WASHER, lock, internal tooth, Ø.375 in. id (78189) (DOD no. ØN123446)	112Ø-12-CPDD	8	
-11	S1 thru S8	. SWITCH, push, spdt, white button (Ø7137) (DOD no. ØN12325Ø-1)	MBS-S-1836A-9	8	
-12		. RETAINER, electrical cable	ØNØ68268	2	
-13		. CLIP, spring tension	ØNØ68261	2	
		(ATTACHING PARTS, for indexes 12 and 13)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.312 in. lg (DOD no. ØN123137-2)	Coml	8	
		. WASHER, flat, no. 6	MS15795-8Ø5	8	
		---*---			
-14		. RETAINER, shield	ØNØ68267	2	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.312 in. lg (DOD no. ØN123137-2)	Coml	8	
		---*---			
-15		. SUPPORT, shield	ØNØ68153	2	
-16		. SUPPORT, shield	ØNØ68263	1	
-17		. KNOB-CONTROL, round	MS91528-1N2B	1	
-18	R1	. RESISTOR, variable, 1 meg ohm, ±1Ø pct, 1w (Ø1121) (DOD no. ØN123Ø82-14)	1N056S1Ø5UA	1	
-19	S9 thru S13	. SWITCH, toggle, 2 pole, 3 position (91927) (DOD no. ØN1232Ø5-2)	13AT4Ø3-T2	5	
-2Ø	S14	. SWITCH, toggle, 2 pole, 3 position (91927) (DOD no. ØN1232Ø5-2)	13AT4Ø1-T2	1	

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-8-21		. SUPPORT, shield	ØNØ68258-2	1	
-22		. BRACKET, angle, indicator	ØN116838	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.312 in. lg (DOD no. ØN123137-2)	Coml	2	
		. WASHER, flat, no. 6	MS15795-8Ø5	2	
		. NUT, self-locking, hex	MS21Ø44-CØ6	2	
		---*---			
-23		. PANEL, control-indicator	ØN116837	1	

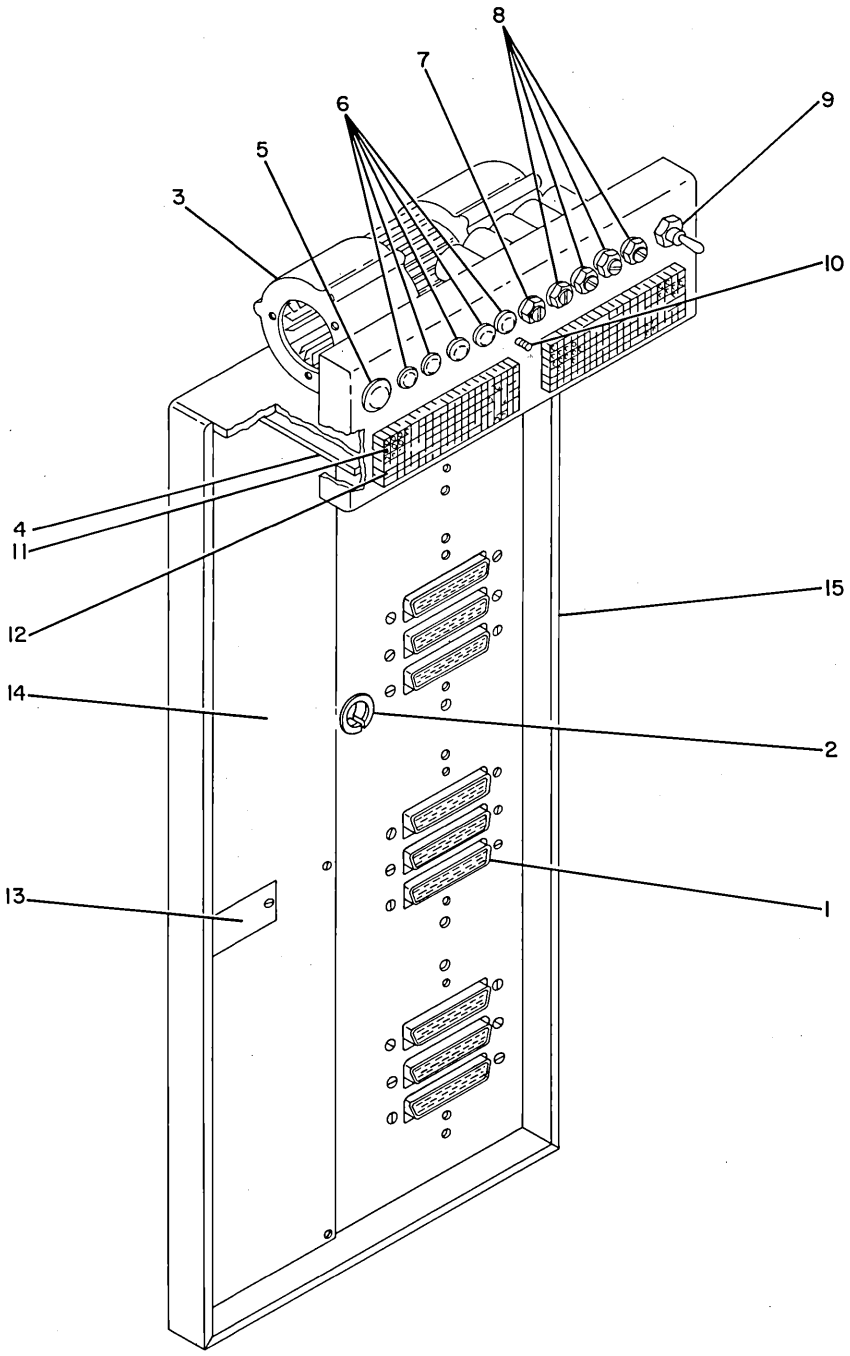


Figure 7-9. Memory Array Stack Panel

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-9-	A3A4, A4A4	PANEL, memory array stack (For NHA see figure 7-6, page 7-32)	ØNØ68174	Ref	
-1	J2Ø1 thru J2Ø3, J211 thru J213, J221 thru J223, J231 thru J233	. CONNECTOR, receptacle, elect (71468) (DOD no. ØN123183-1)	DDM-5ØS	12	
		(ATTACHING PARTS)			
		. SCREW, flat hd, 4-4ØUNC-2A by Ø.438 in. lg (DOD no. ØN123124-4)	Coml	24	
		. NUT, self-locking	MS21Ø44-CØ4	24	
		---*---			
-2		. BEARING, sleeve, Ø.5Ø1 in. id (96881) (DOD no. ØN123168-2)	863-FF	1	
-3	B1	. FAN, centrifugal, 115 v, 42 cfm (82877) (DOD no. ØN123Ø91-1)	A0-185668	1	
		(ATTACHING PARTS)			
		. SCREW, flat hd, 6-32UNC-2A by Ø.5 in. lg (DOD no. ØN123137-4)	Coml	8	
		---*---			
-4		. BAFFLE, air	ØNØ68183	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 8-32UNC-2A by Ø.5 in. lg (DOD no. ØN123525-5)	Coml	2	
		. WASHER, lock, spring, no. 8	MS35338-137	2	
		---*---			
-5		. BUTTON, plug, plain, nickel plated steel (83Ø58) (DOD no. ØN122992-2)	SS-48152	1	
-6		. BUTTON, plug, plain, nickel plated steel (83Ø58) (DOD no. ØN122992-14)	SS-48151	5	
-7	R24	. RESISTOR, variable, ww, 1ØØØ ohm (8Ø294) (DOD no. ØN12315Ø-11)	224S-1-1Ø2(M)	1	
-8	R2Ø thru R23	. RESISTOR, variable, ww, 15 ohm (8Ø294) (DOD no. ØN12315Ø-19)	224S-1-15Ø(M)	4	
-9	S2	. SWITCH, toggle, dpdt (156Ø5) (DOD no. ØN123187-1)	8869-K4	1	
-1Ø		. STUD, extension, cres, 6-32UNC (Ø5581) (DOD no. ØN1231Ø1-3)	R1Ø9Ø	1	
-11		. CONTACT, electrical, female, white, wire wrap (91886) (DOD no. ØN1232Ø1-12)	5191884-12B-529ØØØ9	184	
-12		. CONTACT, electrical, female, (black) wire wrap (91886) (DOD no. ØN1232Ø1-13)	5191761-12A-529ØØØ9	184	
-13		. PLATE, warning, airflow (component of ØN116802-1)	ØN116862	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 4-4ØUNC-2A by Ø.438 in. lg (DOD no. ØN123136-6)	Coml	2	
		. WASHER, flat, no. 4	MS15795-8Ø3	2	
		. NUT, self-locking	MS21Ø44-CØ4	2	
		---*---			
-14		. COVER, memory array	ØNØ68266	1	
		(ATTACHING PARTS)			
		. SCREW, flat hd, 1Ø-32UNF-2A by Ø.375 in. lg (DOD no. ØN123394-1)	Coml	6	
		---*---			
-15		. PANEL, electrical equipment	ØNØ68182	1	

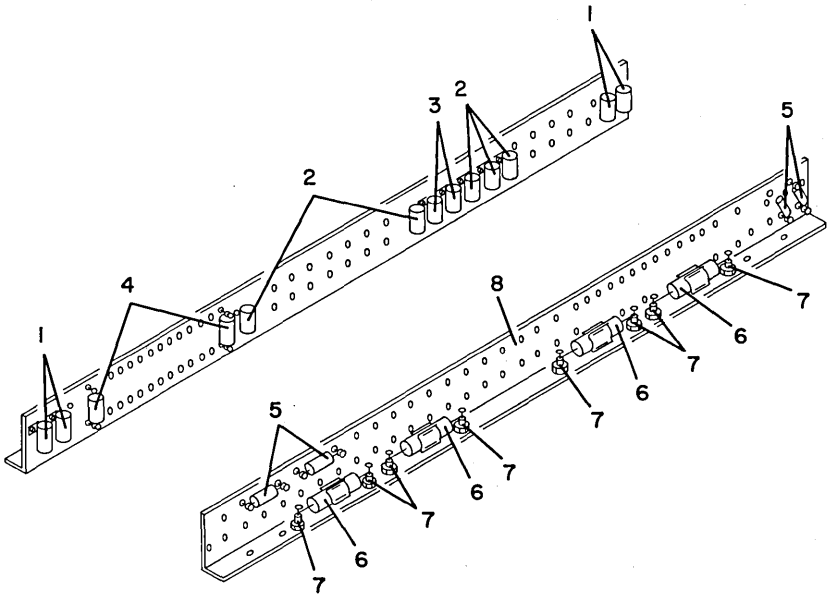


Figure 7-10. Resistor-Capacitor Assembly

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-1Ø-	A3A2A2 A4A2A2	RESISTOR-CAPACITOR ASSEMBLY (For NHA see figure 7-6, page 7-32)	ØNØ68148	Ref	
-1	R1, R2, R37, R38	. RESISTOR, fixed, ww, 1Ø ohm (91637) (DOD no. ØN123196-1)	RE651ØRØ	4	
-2	R18 thru R27, R3Ø thru R32	. RESISTOR, fixed, ww, 15 ohm (91637) (DOD no. ØN123196-18)	RE6515RØ	13	
-3	R28, R29	. RESISTOR, fixed, ww, 43.2 ohm (91637) (DOD no. ØN123196-62)	RE6542R2	2	
		(ATTACHING PARTS, for indexes 1, 2 and 3)			
		. SCREW, pan hd, 2-56UNC-2A by Ø.375 in. lg (DOD no. ØN1231Ø5-5)	Coml	38	
		. WASHER, lock, spring, no. 2	Coml	38	
		. NUT, plain, hex, no. 2	MS35649-224	38	
		---*---			
-4	R4 thru R17	. RESISTOR, fixed	RC42GF15ØJ	14	
-5	R39 thru R42	. RESISTOR, fixed	RC32GF6R8J	4	
-6	C1 thru C4	. CAPACITOR, fixed, electrolytic, 3Ø vdc, 22Ø uf . . .	CL25BH221UP3	4	
-7		. TERMINAL STUD, silver plated (71279) (DOD no. ØN123Ø78-1)	365Ø-1-Ø5	8	
		(ATTACHING PARTS)			
		. SCREW, flat hd, 4-4ØUNC-2A by Ø.25 in. lg (DOD no. ØN123124-1)	Coml	8	
		. WASHER, lock, spring, no. 4	MS35338-135	8	
		---*---			
-8		. BRACKET, electrical equipment	ØNØ68149	1	

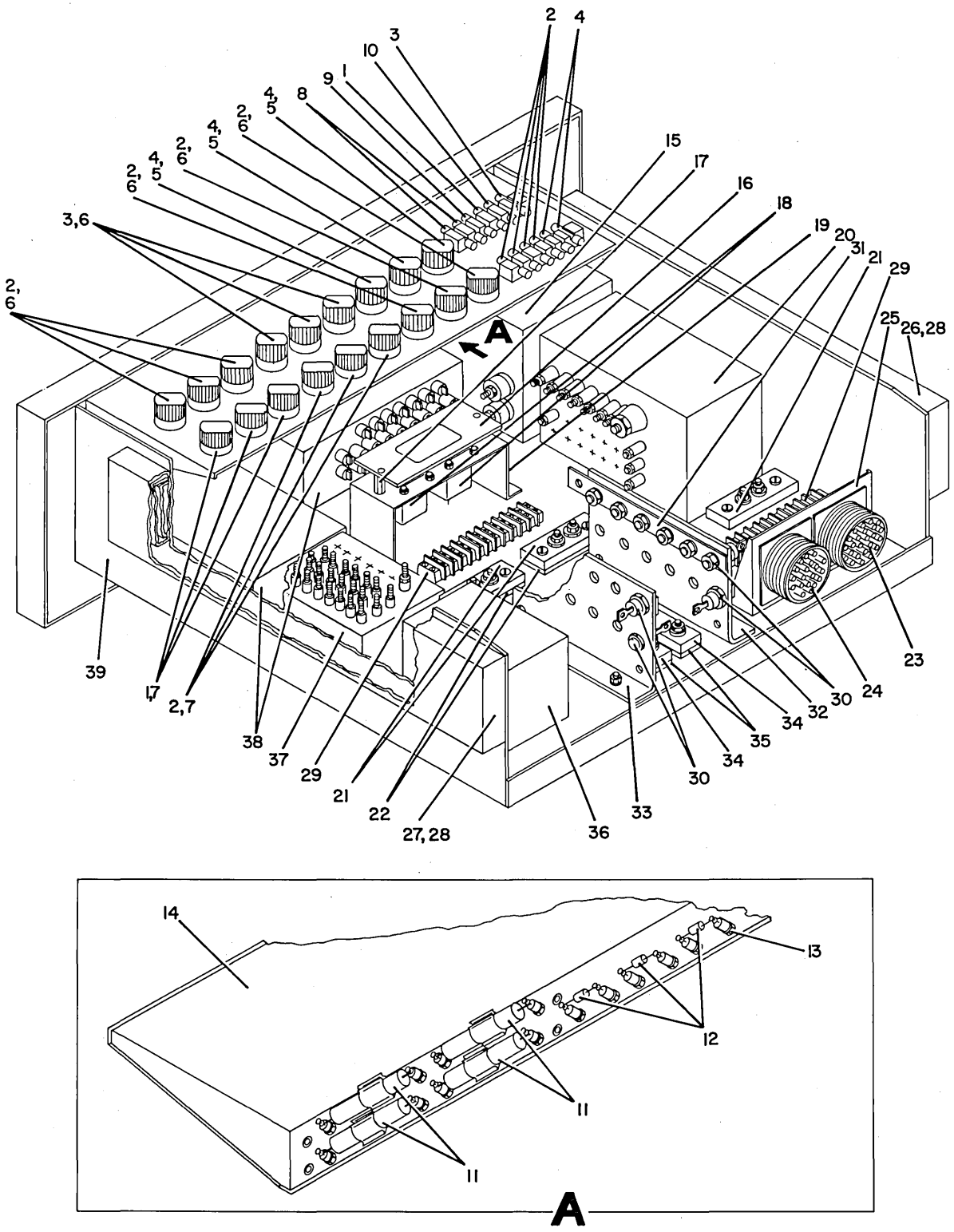


Figure 7-11. Power Supply

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-11-	PS1	POWER SUPPLY (For NHA see figure 7-1, page 7-8)	ØN116826	Ref	
-1	F16, F17, F18	. FUSE, cartridge	FØ3B32V8AS	4	
-2	F7 thru F15	. FUSE, cartridge	FØ2B125V2AS	13	
-3	F4, F5, F6	. FUSE, cartridge	FØ3B125V3AS	4	
-4	F1, F2, F3	. FUSE, cartridge	FØ2B25ØV1AS	5	
-5	XF1, XF2, XF3	. FUSEHOLDER	HKU	3	
-6	XF4 thru XF12	. FUSEHOLDER	FHL18G2-1	9	
-7	XF13 thru XF18	. FUSEHOLDER	FHL17G	6	
-8		. FUSE, cartridge (spare for A12)	FØ3A25ØV1ØAS	2	
-9		. FUSE, cartridge (spare for A12)	FØ2A25ØV8AS	1	
-1Ø		. FUSE, cartridge (spare for A12)	FØ2A25ØV3AS	1	
-11	C1 thru C4	. CAPACITOR, fixed, electrolytic, 3Ø vdc, 22Ø uf	CL25BH221UP3	4	
-12	R1, R2, R3	. RESISTOR, fixed	RCØ7GF1Ø4J	3	
-13		. TERMINAL, stud, silver plated (71279) (DOD no. ØN123Ø78-1)	365Ø-1-Ø5	14	
		(ATTACHING PARTS)			
		. SCREW, flat hd, 4-4ØUNC-2A by Ø.25 in. lg (DOD no. ØN123124-1)	Coml	14	
		. WASHER, lock, spring, no. 4	MS35338-135	14	
		---*---			
-14		. BRACKET, electrical equipment	ØN116811	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 8-32UNC-2A by Ø.5 in. lg	MS51959-45	6	
		---*---			
-15	L1	. REACTOR, filter, 5ØØv, Ø.35 mh, 5Ø amp (8ØØ23) (DOD no. ØN123155-1)	S38Ø7	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, Ø.25-2ØUNC-2A by Ø.5 in. lg (DOD no. ØN123141-1)	Coml	4	
		. WASHER, flat, Ø.25 in. id	MS15795-81Ø	4	
		---*---			
-16		. SHIELD, relay, armature	ØNØ68239	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.5 in. lg (DOD no. ØN123137-5)	Coml	2	
		. WASHER, flat, no. 6	MS15795-8Ø5	2	
		. WASHER, lock, spring, no. 6	MS35338-136	2	
		---*---			
-17		. NUT, sleeve	ØNØ68211	2	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.5 in. lg (DOD no. ØN123137-5)	Coml	2	
		---*---			
-18	K1, K2	. RELAY, armature	MS25271-A1	2	
-19		. BRACKET, relay armature	ØNØ68233	1	
		(ATTACHING PARTS, for indexes 18 and 19)			
		. NUT, self-locking	MS21Ø44-CØ6	12	
		. WASHER, flat	MS15795-8Ø5	12	
		. WASHER, lock	MS35338-136	12	
		---*---			
-2Ø	T1	. TRANSFORMER, power step-down, pri 115v, 4ØØ Hz (7Ø674) (DOD no. ØN123154-1)	A17438	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 1Ø-32UNF-2A by Ø.875 in. lg (DOD no. ØN12314Ø-6)	Coml	4	
		. WASHER, flat, no. 1Ø	MS15795-8Ø8	4	
		---*---			
-21	W1, W4, W5	. BUS BAR	ØNØ67Ø14	3	
-22		. INSULATOR, plate	ØNØ67324	2	

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
		(ATTACHING PARTS, for indexes 21 and 22)			
		. SCREW, pan hd, 6-32UNC-2A by 1.125 in. lg (DOD no. ØN123Ø65-2)	Coml	6	
		. SCREW, pan hd, 6-32UNC-2A by Ø.875 in. lg (DOD no. ØN123137-1Ø)	Coml	6	
		. WASHER, flat, no. 6	MS15795-8Ø5	12	
		. INSULATOR	ØNØ67Ø13	12	
		. NUT, self-locking	MS21Ø44-CØ6	6	
		---*---			
-23	J1	. CONNECTOR, receptacle, elect	MS31Ø2A32-6P	1	
-24	J2	. CONNECTOR, receptacle, elect	MS31Ø2A32-6PW	1	
		(ATTACHING PARTS, for indexes 23 and 24)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.75 in. lg (DOD no. ØN123137-7)	Coml	8	
		. NUT, self-locking	MS21Ø44-CØ6	8	
		---*---			
-25		. BRACKET, electrical connector	ØN116829	1	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 8-32UNC-2A by Ø.5 in. lg (DOD no. ØN123138-5)	Coml	2	
		---*---			
-26		. SLIDE, telescoping, 22 in. lg, rh (Ø5236) (DOD no. ØN123259-2)	35Ø266-R	1	
-27		. SLIDE, telescoping, 22 in. lg, lh (Ø5236) (DOD no. ØN123259-1)	35Ø266-L	1	
-28		. SHIM, alum, Ø.Ø2 in. thk by 17 in. lg	ØNØ68221	AR	
		(ATTACHING PARTS, for indexes 26, 27 and 28)			
		. SCREW, flat hd, 1Ø-32UNF-2A by Ø.625 in. lg (DOD no. ØN123394-4)	Coml	8	
		---*---			
-29	TB1, TB2	. TERMINAL BOARD, barrier type	37TB-11	2	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.75 in. lg (DOD no. ØN123137-7)	Coml	8	
		. WASHER, flat, no. 6	MS15795-8Ø7	8	
		. NUT, self-locking	MS21Ø44-CØ6	8	
		---*---			
-3Ø	CR1 thru CR24	. SEMICONDUCTOR DEVICE, diode	1N1186	24	
-31	W6, W7	. BUS BAR	ØNØ68112	2	
-32		. BRACKET, angle	ØNØ68124	1	
-33		. BRACKET, angle	ØNØ68125	1	
		(ATTACHING PARTS, for indexes 32 and 33)			
		. SCREW, pan hd, 8-32UNC-2A by Ø.625 in. lg (DOD no. ØN123138-5)	Coml	4	
		. NUT, self-locking	MS21Ø44-CØ8	4	
		---*---			
-34	W2, W3	. BUS BAR	ØNØ6811Ø	2	
-35		. INSULATOR, plate	ØNØ68111	2	
		(ATTACHING PARTS, for indexes 34 and 35)			
		. SCREW, pan hd, 6-32UNC-2A by 1.125 in. lg (DOD no. ØN123Ø65-2)	Coml	4	
		. WASHER, flat, no. 6	MS15795-8Ø5	8	
		. INSULATOR	ØNØ67Ø13	8	
		. NUT, self-locking	MS21Ø44-CØ6	4	
		---*---			
-36	L2	. REACTOR, choke filter, 5ØØ uh min, 35 amp (8ØØ23) (DOD no. ØN123119-1)	S3898	1	

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-11-37	T4	. TRANSFORMER, power, step-down, pri 115v, 400 Hz (80023) (DOD no. 0N123169-1)	S4111B	1	
-38	T2, T3	. REACTOR-TRANSFORMER, 1 fixed inductor and 1 transformer (70674) (DOD no. 0N123116-1). . .	A17437	2	
		(ATTACHING PARTS, for indexes 36, 37 and 38)			
		. SCREW, pan hd, 10-32UNF-2A by 0.875 in. lg (DOD no. 0N123137-6).	Coml	16	
		. WASHER, flat, no. 10	MS15795-808	16	
		---*---			
-39		. DRAWER, power supply	0N116825	1	

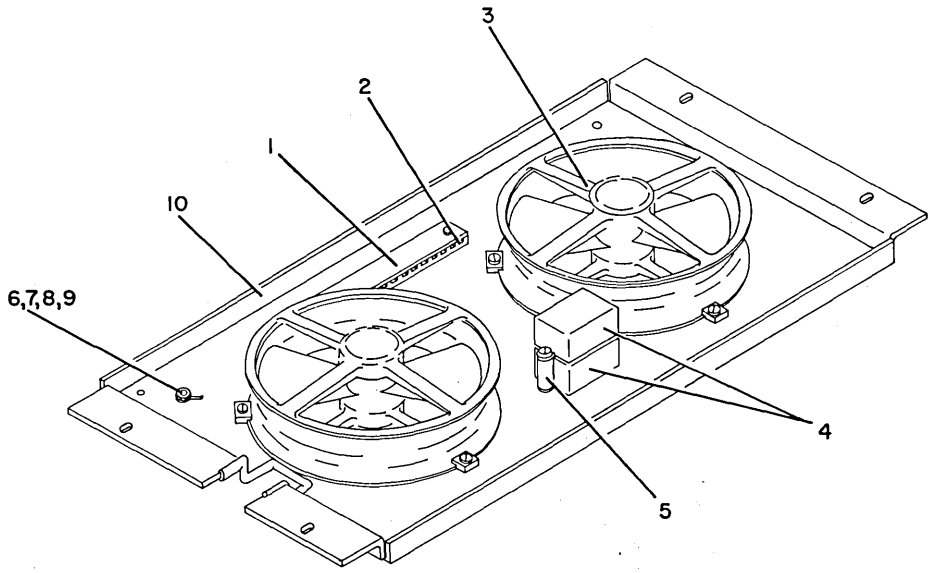
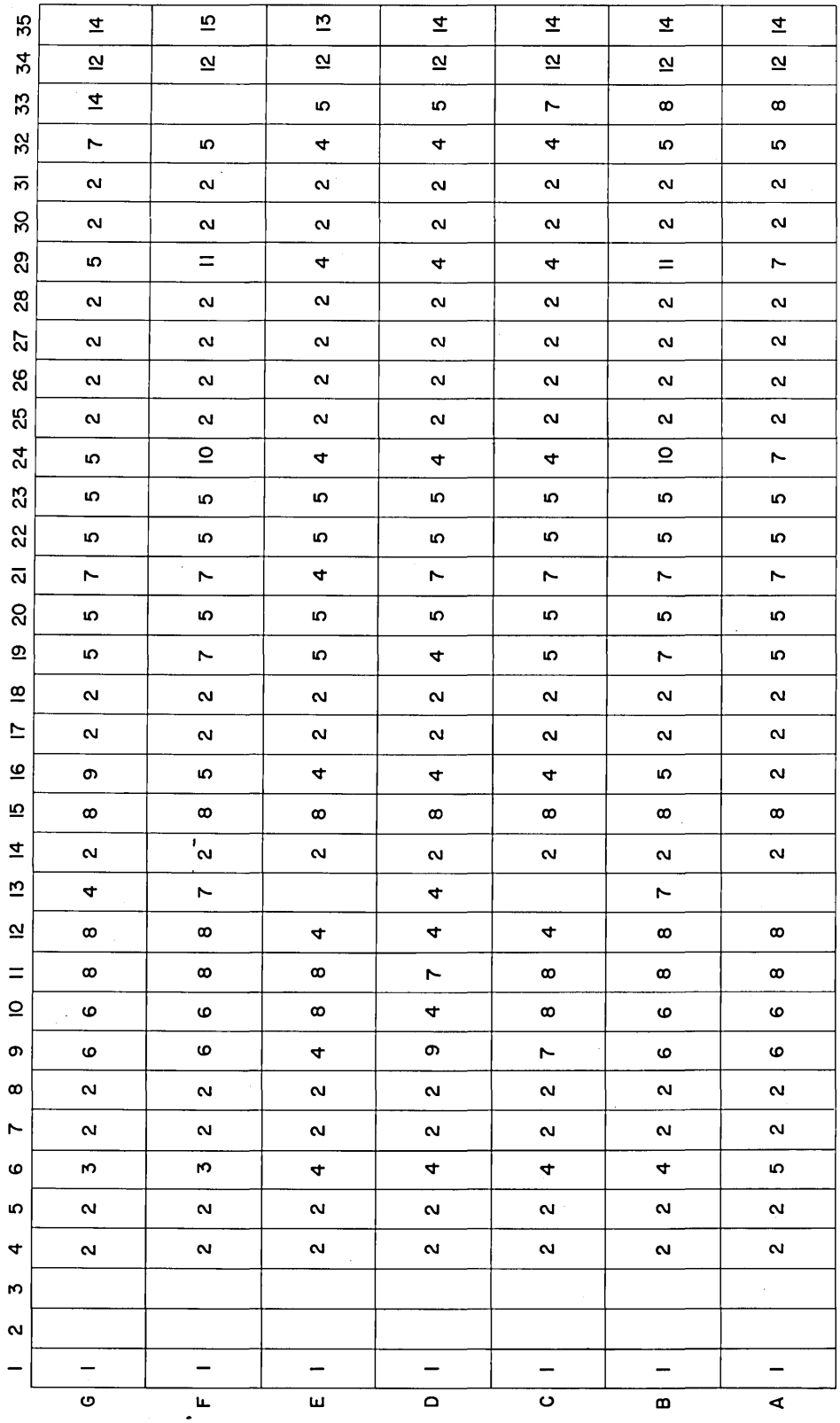


Figure 7-12. Fan Assembly

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-12-	A6, A7	FAN ASSEMBLY (For NHA see figure 7-1, page 7-8) . . .	ØN116843	Ref	
-1		. PLATE, warning high voltage	ØNØ6765Ø	1	
-2	TB1	. TERMINAL BOARD	26TB12	1	
		(ATTACHING PARTS, for indexes 1 and 2)			
		. SCREW, pan hd, 6-32UNC-2A by 1.5 in. lg (DOD no. ØN123137-13)	Coml	2	
		. WASHER, flat, no. 6	MS15795-8Ø5	4	
		. SPACER, sleeve (ØØ141) (DOD no. ØN123Ø83-6)	B8-15	2	
		. NUT, self-locking	MS21Ø44-CØ6	2	
		. WASHER, lock	MS35338-136	2	
		---*---			
-3	B1, B2	. FAN, tubeaxial, 115 vac, 4ØØ Hz, single phase (82877) (DOD no. ØN123Ø37-3)	654DS	2	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 4-4ØUNC-2A by Ø.688 in. lg (DOD no. ØN123Ø68-1)	Coml	6	
		. BLOCK, fan retaining	ØNØ67ØØ8	6	
		. WASHER, flat, no. 4	MS15795-8Ø3	6	
		. NUT, self-locking	MS21Ø44-CØ4	6	
		---*---			
-4	C1, C2	. CAPACITOR, fixed	CH53B1MF1Ø5K	2	
-5		. SPACER, sleeve	ØNØ67Ø11	2	
		(ATTACHING PARTS, for indexes 4 and 5)			
		. SCREW, pan hd, 8-32UNC-2A by 1.5 in. lg (DOD no. ØN123138-11)	Coml	2	
		. WASHER, flat, no. 8	MS15795-8Ø7	2	
		. NUT, self-locking	MS21Ø44-CØ8	2	
		---*---			
-6		. NUT, plain, hex, no. 6	MS35649-264	3	
-7		. WASHER, lock, spring, no. 6	MS35338-136	1	
-8		. TERMINAL, lug, crimping	MS25Ø36-6	1	
-9		. WASHER, lock, ext tooth, no. 6 (DOD no. ØN123148-1)	Coml	1	
-1Ø		. PLATE, mounting fan	ØN116844	1	

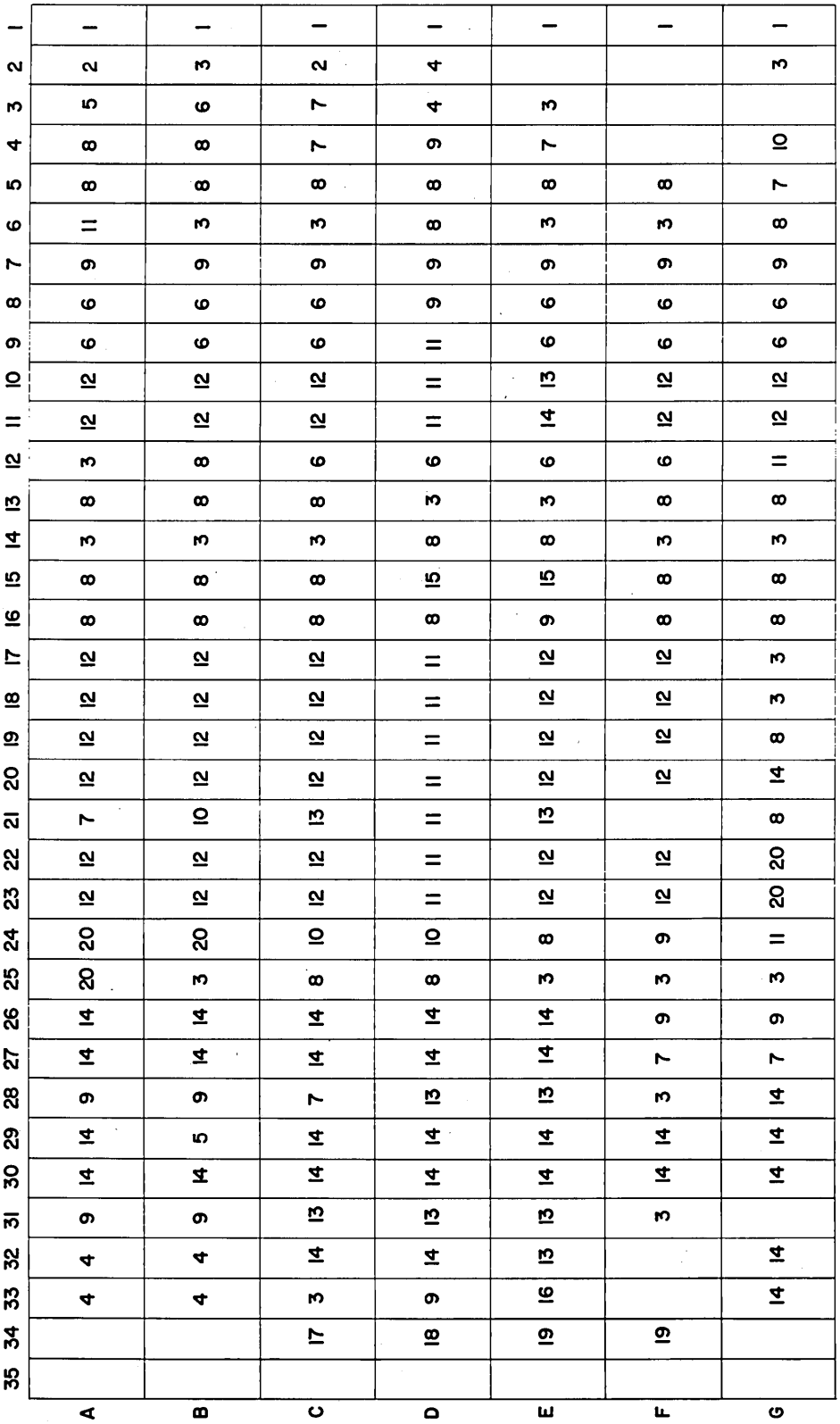


	G	F	E	D	C	B	A
35	14	15	13	14	14	14	14
34	12	12	12	12	12	12	12
33	14		5	5	7	8	8
32	7	5	4	4	4	5	5
31	2	2	2	2	2	2	2
30	2	2	2	2	2	2	2
29	5	11	4	4	4	11	7
28	2	2	2	2	2	2	2
27	2	2	2	2	2	2	2
26	2	2	2	2	2	2	2
25	2	2	2	2	2	2	2
24	5	10	4	4	4	10	7
23	5	5	5	5	5	5	5
22	5	5	5	5	5	5	5
21	7	7	4	7	7	7	7
20	5	5	5	5	5	5	5
19	5	7	5	4	5	7	5
18	2	2	2	2	2	2	2
17	2	2	2	2	2	2	2
16	9	5	4	4	4	5	2
15	8	8	8	8	8	8	8
14	2	2	2	2	2	2	2
13	4	7		4		7	
12	8	8	4	4	4	8	8
11	8	8	8	7	8	8	8
10	6	6	8	4	8	6	6
9	6	6	4	9	7	6	6
8	2	2	2	2	2	2	2
7	2	2	2	2	2	2	2
6	3	3	4	4	4	4	5
5	2	2	2	2	2	2	2
4	2	2	2	2	2	2	2
3							
2							
1	1	1	1	1	1	1	1

Figure 7-13. Printed Circuit Module Location A1A1

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-13-		PRINTED-CIRCUIT MODULE LOCATION, chassis A1A1	No Number	NP	
-1	A1A thru A1G	. CAPACITOR ASSEMBLY, #3	ØNØ71777	7	
-2	A4A thru A4G, A5A thru A5G, A7A thru A7G, A8A thru A8G, A14A thru A14G, A16A, A17A thru A17G, A18A thru A18G, A25A thru A25G, A26A thru A26G, A27A thru A27G, A28A thru A28G, A3ØA thru A3ØG, A31A thru A31G	. FLIP FLOP, AND OR 222-1	ØNØ7176Ø	92	
-3	A6F, A6G	. INVERTER, AND 5-4	ØNØ71761	2	
-4	A6B thru A6E, A9D, A9E, A1ØD, A12C, A12D, A12E, A13D, A13G, A16C, A16D, A16E, A19D, A21E, A24C, A24D, A24E, A29C, A29D, A29E, A32C, A32D, A32E	. AMPLIFIER, driver, clock and logic 2-3	ØNØ68Ø23	26	
-5	A6A, A16B, A16F, A19A, A19C, A19E, A19G, A2ØA thru A2ØG, A22A thru A22G, A23A thru A23G, A24G, A29G, A32A, A32B, A32F, A33D, A33E	. INVERTER, AND OR 22-23	ØNØ64Ø1Ø	35	
-6	A9A, A9B, A9F, A9G, A1ØA, A1ØB, A1ØF, A1ØG	. INVERTER, AND 3-3-2	ØNØ64Ø11	8	
-7	A9C, A11D, A13B, A13F, A19B, A19F, A21A thru A21D, A21F, A21G, A24A, A29A, A32G, A33C	. INVERTER, 1-1-1-1-1	ØNØ64Ø12	16	
-8	A1ØC, A1ØE, A11A, A11B, A11C, A11E, A11F, A11G, A12A, A12B, A12F, A12G, A15A thru A15G, A33A, A33B	. INVERTER, AND OR 22222	ØNØ64ØØ9	21	
-9	A16G	. FLIP FLOP, AND OR 33-3	ØNØ64ØØ8	1	
-1Ø	A24B, A24F	. INVERTER, AND 3-6	ØNØ71762	2	
-11	A29B, A29F	. INVERTER, AND 1-8	ØNØ71764	2	
-12	A34A thru A34G	. FLIP FLOP, 2(2C/21C)	ØNØ71774	7	
-13	A35E	. CAPACITOR-RESISTOR ASSEMBLY	ØNØ68Ø21	1	
-14	A33G, A35A thru A35D, A35F, A35G	. FLIP FLOP - 2(221C)	ØNØ68Ø17	7	



	A	B	C	D	E	F	G
1	1	1	1	1	1	1	1
2	2	3	2	4			3
3	5	6	7	4	3		
4	8	8	7	9	7		10
5	8	8	8	8	8	8	7
6	11	3	3	8	3	3	8
7	9	9	9	9	9	9	9
8	6	6	6	9	6	6	6
9	6	6	6	11	6	6	6
10	12	12	12	11	13	12	12
11	12	12	12	11	14	12	12
12	3	8	6	6	6	6	11
13	8	8	8	3	3	8	8
14	3	3	3	8	8	3	3
15	8	8	8	15	15	8	8
16	8	8	8	8	9	8	8
17	12	12	12	11	12	12	3
18	12	12	12	11	12	12	3
19	12	12	12	11	12	12	8
20	12	12	12	11	12	12	14
21	7	10	13	11	13		8
22	12	12	12	11	12	12	20
23	12	12	12	11	12	12	20
24	20	20	10	10	8	9	11
25	20	3	8	8	3	3	3
26	14	14	14	14	14	9	9
27	14	14	14	14	14	7	7
28	9	9	7	13	13	3	14
29	14	5	14	14	14	14	14
30	14	14	14	14	14	14	14
31	9	9	13	13	13	3	
32	4	4	14	14	13		14
33	4	4	3	9	16		14
34			17	18	19	19	
35							

Figure 7-14. Printed Circuit Module Location A1A2

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-14-		PRINTED-CIRCUIT MODULE LOCATION, chassis A1A2	No Number	NP	
-1	A1A thru A1G	. CAPACITOR ASSEMBLY, #3	ØNØ71777	7	
-2	A2A, A2C	. AMPLIFIER, driver, panel lamp	ØNØ71779	2	
-3	A2B, A2G, A3E, A6B, A6C, A6E, A6F, A12A, A13D, A13E, A14A, A14B, A14C, A14F, A14G, A17G, A18G, A25B, A25E, A25F, A25G, A28F, A31F, A33C	. INVERTER, 1-1-1-1-1	ØNØ64Ø12	24	
-4	A2D, A3D, A32A, A32B, A33A, A33B	. FLIP FLOP, 2(2C/21C)	ØNØ71774	6	
-5	A3A	. RESISTOR ASSEMBLY	ØNØ68Ø19	1	
-6	A3B, A8A, A8B, A8C, A8E, A8F, A8G, A9A, A9B, A9C, A9E, A9F, A9G, A12C thru A12F	. INVERTER, AND OR 22222	ØNØ64ØØ9	17	
-7	A3C, A4C, A4E, A5G, A21A, A27F, A27G, A28C	. INVERTER, AND 5-4	ØNØ71761	8	
-8	A4A, A4B, A5A thru A5F, A6D, A6G, A12B, A13A, A13B, A13C, A13F, A13G, A14D, A14E, A15A, A15B, A15C, A15F, A15G, A16A thru A16D, A16F, A16G, A19G, A21G, A24E, A25C, A25D	. INVERTER, AND OR 22-23	ØNØ64Ø1Ø	34	
-9	A4D, A7A thru A7G, A8D, A16E, A24F, A26F, A26G, A28A, A28B, A31A, A31B, A33D	. INVERTER, AND 3-3-2	ØNØ64Ø11	18	
-1Ø	A4G, A21B, A24C, A24D	. INVERTER, AND 1-8	ØNØ71764	4	
-11	A6A, A9D, A1ØD, A11D, A12G, A17D, A18D, A19D, A2ØD, A21D, A22D, A23D, A24G	. AMPLIFIER, driver, clock and logic 2-3	ØNØ67517	13	
-12	A1ØA, A1ØB, A1ØC, A1ØF, A1ØG, A11A, A11B, A11C, A11F, A11G, A17A, A17B, A17C, A17E, A17F, A18A, A18B, A18C, A18E, A18F, A19A, A19B, A19C, A19E, A19F, A2ØA, A2ØB, A2ØC, A2ØE, A2ØF, A22A, A22B,	. FLIP FLOP, AND OR 2222-1	ØNØ7176Ø	4Ø	

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-14-12 (Cont.)	A22C, A22E, A22F, A23A, A23B, A23C, A23E, A23F				
-13	A1ØE, A21C, A21E, A28D, A28E, A31C, A31D, A31E, A32E	. AMPLIFIER, driver, clock and logic 2-3	ØNØ68Ø23	9	
-14	A11E, A2ØG, A26A thru A26E, A27A thru A27E, A28G, A29A thru A29G, A3ØA thru A3ØG, A32C, A32D, A32G, A33G	. FLIP FLOP, AND OR 33-3	ØNØ64ØØ8	31	
-15	A15D, A15E	. INVERTER, AND 3-6	ØNØ71762	2	
-16	A33E	. DRIVER, emitter follower-inverter	ØNØ68ØØ5	1	
-17	A34C	. AMPLIFIER, driver, clock delay line	ØNØ64Ø16	1	
-18	A34D	. NETWORK, pulse delay, Ø.5 usec	ØNØ71768	1	
-19	A34E, A34F	. NETWORK, pulse delay, Ø.1 usec	ØNØ68ØØ4	2	
-2Ø	A22G, A23G, A24A, A24B, A25A	. FLIP FLOP	ØNØ68Ø17	5	

	G	F	E	D	C	B	A
35		8	12	8	3	3	
34	7	4	4	9	1	2	3
33	3	4	4	4	5	3	3
32	3	4	4	6	7	7	8
31	3	6	6	6	8	4	4
30	8	6	6	6	8	8	7
29	3	3	6	3	3	3	4
28	7	3	3	3	4	18	8
27	3	3	3	3	6	18	8
26	3	3	3	3	6	18	3
25	9	7	7	7	9	3	3
24	3	6	6	6	6	7	10
23	4	6	3	3	9	4	4
22	4	4	7	3	3	4	4
21	4	4	4	3	6	6	7
20	4	6	4	7	4	4	4
19	4	4	4	7	4	4	7
18	13	3	6	3		3	3
17	4	4	7	3	4	4	3
16	4	4	3	3	4	4	9
15	8	4	4	7	4	4	8
14	8	4	3	3	4	4	3
13	4	9	8	3	4	4	10
12	4	3	10	8	4	4	7
11	4	7	8	9	4	3	8
10	4	3	3	3	4	3	9
9	4	9	3	8	4	7	8
8	10	8	3	3	3	3	3
7	7	7	3	4	11	7	12
6	8	3	13	14	9	3	7
5	9	7	7	15	3	3	3
4	3	4	9	3	3	3	3
3	13	3	3	3	7	3	3
2		17	8	8	4	7	
1	16	16	16	16	16	16	16

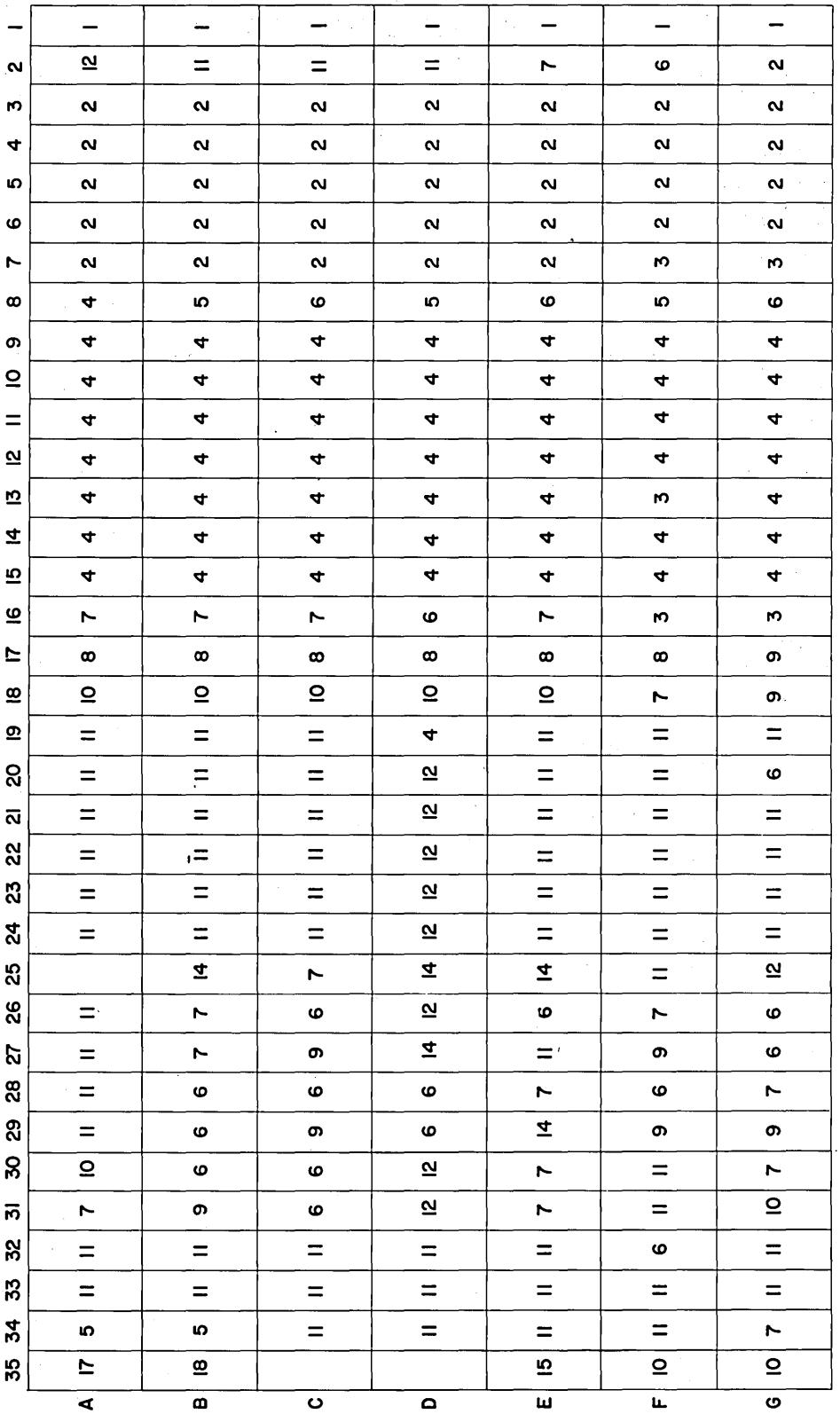
Figure 7-15. Printed Circuit Module Location A2A1

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-15-		PRINTED-CIRCUIT MODULE LOCATION, chassis A2A1	No Number	NP	
-1	A34C	. INVERTER, input amplifier	ØNØ64Ø13	1	
-2	A34B	. SWITCH, positive and negative	ØNØ64Ø19	1	
-3	A3A, A3B, A3D, A3E, A3F, A4A thru A4D, A4G, A5A, A5B, A5C, A6B, A6F, A7E, A8A thru A8E, A9E, A1ØB, A1ØD, A1ØE, A1ØF, A11B, A12F, A13D, A14A, A14D, A14E, A16D, A16E, A17A, A17D, A18A, A18B, A18D, A18F, A21D, A22C, A22D, A23D, A23E, A24G, A25A, A25B, A26A, A26D thru A26G, A27D thru A27G, A28D, A28E, A28F, A29B, A29C, A29D, A29F, A29G, A31G, A32G, A33A, A33B, A33G, A35B, A35C	. INVERTER, AND 3-3-2	ØNØ64Ø11	75	
-4	A2C, A4F, A7D, A9C, A9G, A1ØC, A1ØG, A11C, A11G, A12B, A12C, A12G, A13B, A13C, A13G, A14B, A14C, A14F, A15B, A15C, A15F, A16B, A16C, A16F, A16G, A17B, A17C, A17F, A17G, A19B, A19C, A19E, A19F, A19G, A2ØA, A2ØB, A2ØC, A2ØE, A2ØG, A21E, A21F, A21G, A22A, A22B, A22F, A22G, A23A, A23B, A23G, A28C, A29A, A31A, A31B, A32E, A32F, A33D, A33E, A33F, A34E, A34F	. FLIP FLOP, AND OR 33-3	ØNØ64ØØ8	59	
-5	A33C	. OSCILLATOR, pulse delay, low speed variable	ØNØ64ØØØ	1	
-6	A18E, A2ØF, A21B, A21C, A23F, A24C, A24D, A24E, A24F, A26C, A27C, A29E, A3ØD, A3ØE, A3ØF, A31D, A31E, A31F, A32D	. AMPLIFIER, driver, clock and logic 2-3	ØNØ68Ø23	19	

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-15-7	A2B, A3C, A5E, A5F, A6A, A7B, A7F, A7G, A9B, A11F, A12A, A15D, A17E, A19A, A19D, A20D, A21A, A22E, A24B, A25D, A25E, A25F, A28G, A30A, A32B, A32C, A34G	. INVERTER, 1-1-1-1-1	0N0640120	27	
-8	A2D, A2E, A6G, A8F, A9A, A9D, A11A, A11E, A12D, A13E, A14G, A15A, A15E, A15G, A27A, A28A, A30B, A30C, A30G, A31C, A32A, A35D, A35F	. INVERTER, AND OR 22-23	0N0640100	23	
-9	A4E, A5G, A6C, A9F, A10A, A11D, A13F, A16A, A23C, A25C, A25G, A34D	. INVERTER, AND 5-4	0N071761	12	
-10	A8G, A12E, A13A, A24A	. INVERTER, AND 3-6	0N071762	4	
-11	A7C	. AMPLIFIER, driver, clock delay line	0N064016	1	
-12	A7A, A35E	. INVERTER, AND OR 22222	0N064009	2	
-13	A3G, A6E, A18G	. INVERTER, AND 1-8	0N071764	3	
-14	A6D	. NETWORK, pulse delay, 0.3 usec, 10 section	0N064024	1	
-15	A5D	. AMPLIFIER, driver, clock timing	0N064015	1	
-16	A1A thru A1G	. CAPACITOR ASSEMBLY, #3	0N071777	7	
-17	A2F	. INVERTER, OR 4-4	0N064023	1	
-18	A26B, A27B, A28B	. FLIP FLOP, 2(2C/21C)	0N071774	3	



	A	B	C	D	E	F	G
1	1	1	1	1	1	1	1
2	12	11	11	11	7	6	2
3	2	2	2	2	2	2	2
4	2	2	2	2	2	2	2
5	2	2	2	2	2	2	2
6	2	2	2	2	2	2	2
7	2	2	2	2	2	3	3
8	4	5	6	5	6	5	6
9	4	4	4	4	4	4	4
10	4	4	4	4	4	4	4
11	4	4	4	4	4	4	4
12	4	4	4	4	4	4	4
13	4	4	4	4	4	3	4
14	4	4	4	4	4	4	4
15	4	4	4	4	4	4	4
16	7	7	7	6	7	3	3
17	8	8	8	8	8	8	9
18	10	10	10	10	10	7	9
19	11	11	11	4	11	11	11
20	11	11	11	12	11	11	6
21	11	11	11	12	11	11	11
22	11	11	11	12	11	11	11
23	11	11	11	12	11	11	11
24	11	11	11	12	11	11	11
25		14	7	14	14	11	12
26	11	7	6	12	6	7	6
27	11	7	9	14	11	9	6
28	11	6	6	6	7	6	7
29	11	6	9	6	14	9	9
30	10	6	6	12	7	11	7
31	7	9	6	12	7	11	10
32	11	11	11	11	11	6	11
33	11	11	11	11	11	11	11
34	5	5	11	11	11	11	7
35	17	18			15	10	10

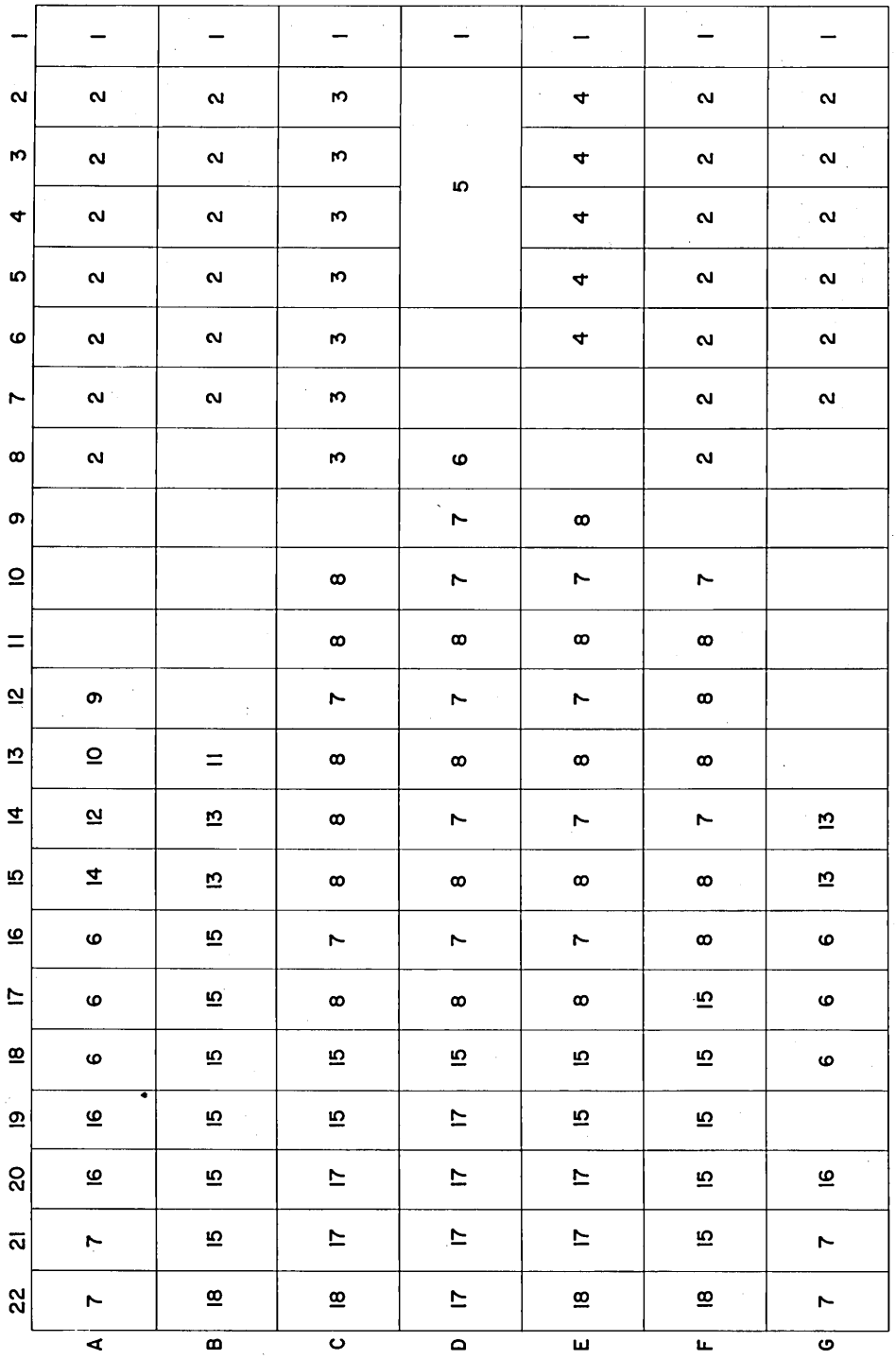
Figure 7-16. Printed Circuit Module Location A2A2

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-16-		PRINTED-CIRCUIT MODULE LOCATION, chassis A2A2	No Number	NP	
-1	A1A thru A1G	. CAPACITOR ASSEMBLY, #3	ØNØ71777	7	
-2	A2G, A3A thru A3G, A4A thru A4G, A5A thru A5G, A6A thru A6G, A7A thru A7E	. AMPLIFIER, driver, 6 volt line	ØNØ68Ø31	34	
-3	A7F, A7G, A13F, A16F, A16G	. INVERTER, AND OR 22222	ØNØ64ØØ9	5	
-4	A8A, A9A thru A9G, A1ØA thru A1ØG, A11A thru A11G, A12A thru A12G, A13A thru A13E, A13G, A14A thru A14G, A15A thru A15G, A19D	. INVERTER-INPUT AMPLIFIER, -6 v	ØNØ64Ø26	51	
-5	A8B, A8D, A8F, A34A, A34B	. FLIP FLOP, 2(2C/21C)	ØNØ71774	5	
-6	A2F, A8C, A8E, A8G, A16D, A2ØG, A26C, A26E, A26G, A27G, A28B, A28C, A28D, A28F, A29B, A29D, A3ØB, A3ØC, A31C, A32F	. INVERTER, AND 3-3-2	ØNØ64Ø11	2Ø	
-7	A2E, A16A, A16B, A16C, A16E, A18F, A25C, A26B, A26F, A27B, A28E, A28G, A3ØE, A3ØG, A31A, A31E, A34G	. INVERTER, 1-1-1-1-1	ØNØ64Ø12	17	
-8	A17A thru A17F	. INVERTER, AND 1-8	ØNØ71764	6	
-9	A17G, A18G, A27C, A27F, A29C, A29F, A29G, A31B	. INVERTER, AND 5-4	ØNØ71761	8	
-1Ø	A18A thru A18E, A3ØA, A35F, A35G	. INVERTER, AND 3-6	ØNØ71762	8	
-11	A2B, A2C, A2D, A19A, A19B, A19C, A19E, A19F, A19G, A2ØA, A2ØB, A2ØC, A2ØE, A2ØF, A21A, A21B, A21C, A21E, A21F, A21G, A22A, A22B, A22C, A22E, A22F, A22G, A23A, A23B, A23C, A23E, A23F, A23G, A24A, A24B, A24C, A24E, A24F, A24G, A25F, A26A, A27A, A27E, A28A, A29A, A3ØF, A31F, A31G,	. FLIP FLOP, AND OR 33-3	ØNØ64ØØ8	64	

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-16-11 (Cont.)	A32A thru A32E, A32G, A33A thru A33G, A34C thru A34F				
-12	A2A, A2Ø0D, A21D, A22D, A23D, A24D, A25G, A26D, A3Ø0D, A31D	AMPLIFIER, driver	ØNØ68Ø23	1Ø	



	A	B	C	D	E	F	G
1	1	1	1	1	1	1	1
2	2	2	3	5	4	2	2
3	2	2	3		4	2	2
4	2	2	3		4	2	2
5	2	2	3		4	2	2
6	2	2	3		4	2	2
7	2	2	3			2	2
8	2		3	6		2	
9				7	8		
10			8	7	7	7	
11			8	8	8	8	
12	9		7	7	7	8	
13	10	11	8	8	8	8	
14	12	13	8	7	7	7	13
15	14	13	8	8	8	8	13
16	6	15	7	7	7	8	6
17	6	15	8	8	8	15	6
18	6	15	15	15	15	15	6
19	16	15	15	17	15	15	
20	16	15	17	17	17	15	16
21	7	15	17	17	17	15	7
22	7	18	18	17	18	18	7

Figure 7-17. Printed Circuit Module Location A3A2/A4A2

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-17-		PRINTED-CIRCUIT MODULE LOCATION, chassis A3A2/A4A2	No Number	NP	
-1	A1A thru A1G	. CAPACITOR ASSEMBLY, #3	ØNØ71777	7	
-2	A2A, A2B, A2F, A2G, A3A, A3B, A3F, A3G, A4A, A4B, A4F, A4G, A5A, A5B, A5F, A5G, A6A, A6B, A6F, A6G, A7A, A7B, A7F, A7G, A8A, A8F	. AMPLIFIER, sense, matched input	ØNØ68ØØ1	26	
-3	A2C, A3C, A4C, A5C, A6C, A7C, A8C	. INVERTER, AND 5-4	ØNØ71761	7	
-4	A2E, A3E, A4E, A5E, A6E	. AMPLIFIER, driver, positive and negative	ØNØ68ØØ8	5	
-5		. BOOTSTRAP ASSEMBLY (used on A3A2)	ØNØ682Ø9	1	
		. BOOTSTRAP ASSEMBLY (used on A4A2)	ØNØ6821Ø	1	
-6	A8D, A16A, A16G, A17A, A17G, A18A, A18G	. INVERTER, 1-1-1-1-1	ØNØ64Ø12	7	
-7	A9D, A1ØD, A1ØE, A1ØF, A12C, A12D, A12E, A14D, A14E, A14F, A16C, A16D, A16E, A21A, A21G, A22A, A22G	. AMPLIFIER, current diverter, memory	ØNØ68Ø33	17	
-8	A9E, A1ØC, A11C thru A11F, A12F, A13C thru A13F, A14C, A15C thru A15F, A16F, A17C, A17D, A17E	. SWITCH, Inhibit	ØNØ64Ø22	2Ø	
-9	A12A	. SENSOR, voltage, +15, -15	ØNØ68ØØ2	1	
-1Ø	A13A	. SENSOR, voltage, -4.5 and positive switch	ØNØ68ØØ6	1	
-11	A13B	. AMPLIFIER, driver, clock and logic 2-3	ØNØ68Ø23	1	
-12	A14A	. AMPLIFIER, regulator, ±10v	ØNØ68ØØ7	1	
-13	A14B, A14G, A15B, A15G	. INVERTER, OR 4-4	ØNØ64Ø23	4	
-14	A15A	. CAPACITOR ASSEMBLY	ØNØ68Ø29	1	
-15	A16B, A17B, A17F, A18B thru A18F, A19B, A19C, A19E, A19F, A2ØB, A2ØF, A21B, A21F	. SWITCH, positive and negative	ØNØ64Ø19	16	
-16	A19A, A2ØA, A2ØG	. NETWORK TRANSFORMER, current probe	ØNØ68ØØ3	3	
-17	A19D, A2ØC, A2ØD, A2ØE, A21C, A21D, A21E, A22D	. SWITCH, negative	ØNØ64Ø18	8	
-18	A22B, A22C, A22E, A22F	. SWITCH, read/write	ØNØ64Ø21	4	

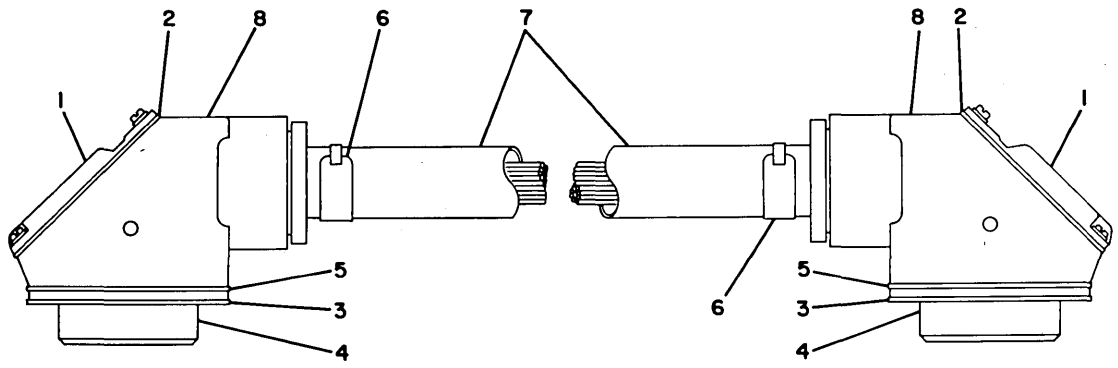


Figure 7-18. Electrical Special Purpose Cable Assembly

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-18-		CABLE ASSEMBLY, special purpose, electrical, 50 ft. lg	ØN116657-2	1	
-1		. COVER, electrical connector	ØN1163Ø8	2	
-2		. SEAL, male, connector to panel	ØNØ67315	2	
		(ATTACHING PARTS, for indexes 1 and 2)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.5 in. lg (DOD no. ØN123137-5)	Coml	8	
		---*---			
-3		. GASKET, electrical connector	ØN1163Ø7	2	
-4	P1, P2	. CONNECTOR, receptacle, electrical, female, 50 contact (71468) (DOD no. ØN123166)	DPD45ØØ-52Ø7	2	
-5		. SEAL, male, connector to panel	ØNØ67315	2	
		(ATTACHING PARTS, for indexes 4 and 5)			
		. SCREW, flat hd, 6-32UNC-2A by Ø.5 in. lg (DOD no. ØN123125-4)	Coml	8	
		---*---			
-6		. BAND, marker, blank, alum, 4.5 in. lg (DOD no. ØN123Ø45-1)	Coml	2	
-7		. CONDUIT ASSEMBLY, metal flexible	ØN116314-4	1	
-8		. SHELL, electrical connector	ØN1163Ø6	2	

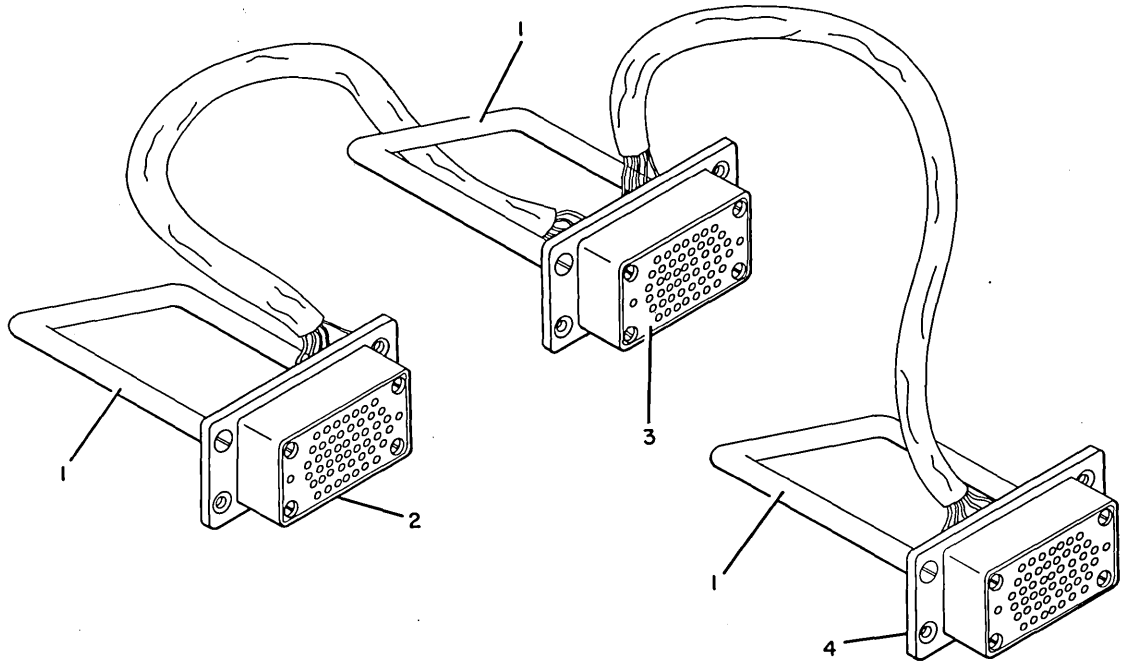


Figure 7-19. Test Cable Assembly

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-19-		CABLE ASSEMBLY, test #1	ØNØ68198	1	
		CABLE ASSEMBLY, test #2	ØNØ68199	1	
		CABLE ASSEMBLY, test #3	ØNØ682ØØ	1	
		CABLE ASSEMBLY, test #4	ØNØ682Ø1	1	
		CABLE ASSEMBLY, test #5	ØNØ6826Ø	1	
-1		. HANDLE (used on ØNØ68198 and ØNØ6826Ø)	ØNØ682Ø5	1	
		. HANDLE (used on ØNØ68199, ØNØ682ØØ, and ØNØ682Ø1)	ØNØ682Ø5	3	
		(ATTACHING PARTS)			
		. SCREW, flat hd, 6-32UNC-2A by Ø.312 in. lg (used on ØNØ68198 and ØNØ6826Ø) (DOD no. ØN123125-1)	Coml	2	
		. SCREW, flat hd, 6-32UNC-2A by Ø.312 in. lg (used on ØNØ68199, ØNØ682ØØ, and ØNØ682Ø1) (DOD no. ØN123125-1)	Coml	6	
		---*---			
-2	P1	. CONNECTOR, receptacle, electrical (71468) (DOD no. ØN123166)	DPD45ØØ-52Ø7	1	
-3	P2	. CONNECTOR, receptacle, electrical (71468) (DOD no. ØN123166) (used on ØNØ68199, ØNØ682ØØ, and ØNØ682Ø1)	DPD45ØØ-52Ø7	1	
-4	P3	. CONNECTOR, receptacle, electrical (71768) (used on ØNØ68199, ØNØ682ØØ, and ØNØ682Ø1) (DOD no. ØN123166)	DPD45ØØ-52Ø7	1	

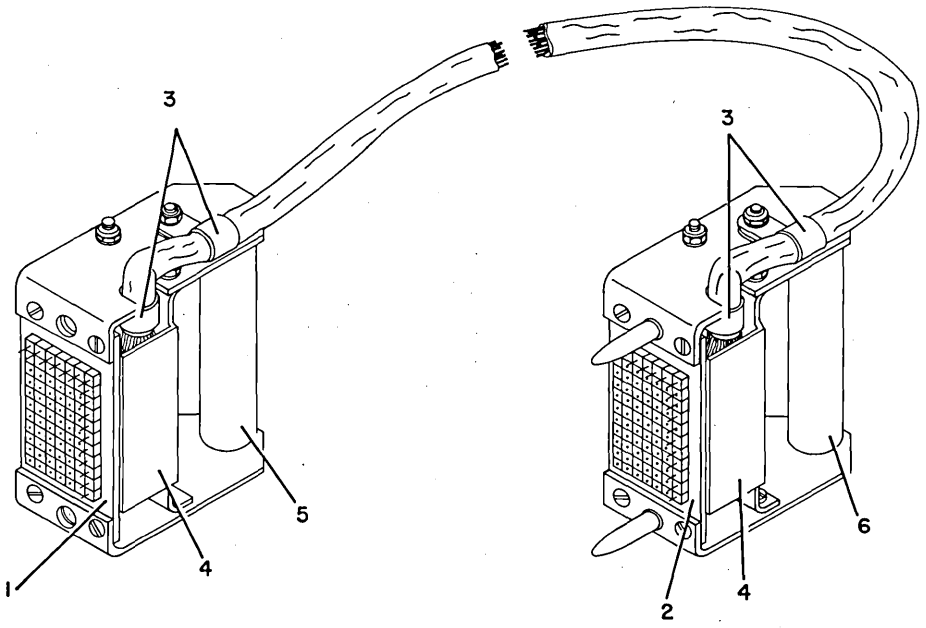


Figure 7-20. Cable Extender

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-2Ø-		CABLE EXTENDER	ØNØ68262	2	
-1	P1	. CONNECTOR, receptacle, elect (91886) (DOD no. ØN12323Ø-1)	361468Ø	1	
		(ATTACHING PARTS)			
		. SCREW, flat hd, 6-32UNC-2A by Ø.375 in. lg (DOD no. ØN123125-2)	Coml	4	
		---*---			
-2	P2	. CONNECTOR, receptacle, elect (91886) (DOD no. ØN123228-1)	3614679	1	
		(ATTACHING PARTS)			
		. SCREW, flat hd, 6-32UNC-2A by Ø.5 in. lg (DOD no. ØN123125-4)	Coml	4	
		. WASHER, flat, no. 6	MS15795-8Ø5	4	
		. NUT, self-locking	MS21Ø44-CØ6	4	
		---*---			
-3		. CLAMP, loop	ØN122981-8	4	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.5 in. lg (DOD no. ØN123137-4)	Coml	4	
		. WASHER, flat, no. 6	MS15795-8Ø5	4	
		. NUT, self-locking, hex	MS21Ø44-CØ6	4	
		---*---			
-4		. RETAINER	ØNØ68277	2	
		(ATTACHING PARTS)			
		. SCREW, pan hd, 6-32UNC-2A by Ø.438 in. lg (DOD no. ØN123137-5)	Coml	8	
		. WASHER, flat, no. 6	MS15795-8Ø5	8	
		. NUT, self-locking, hex	MS21Ø44-CØ6	8	
		---*---			
-5		. HANDLE	ØNØ68264	1	
-6		. HANDLE	ØNØ68278	1	

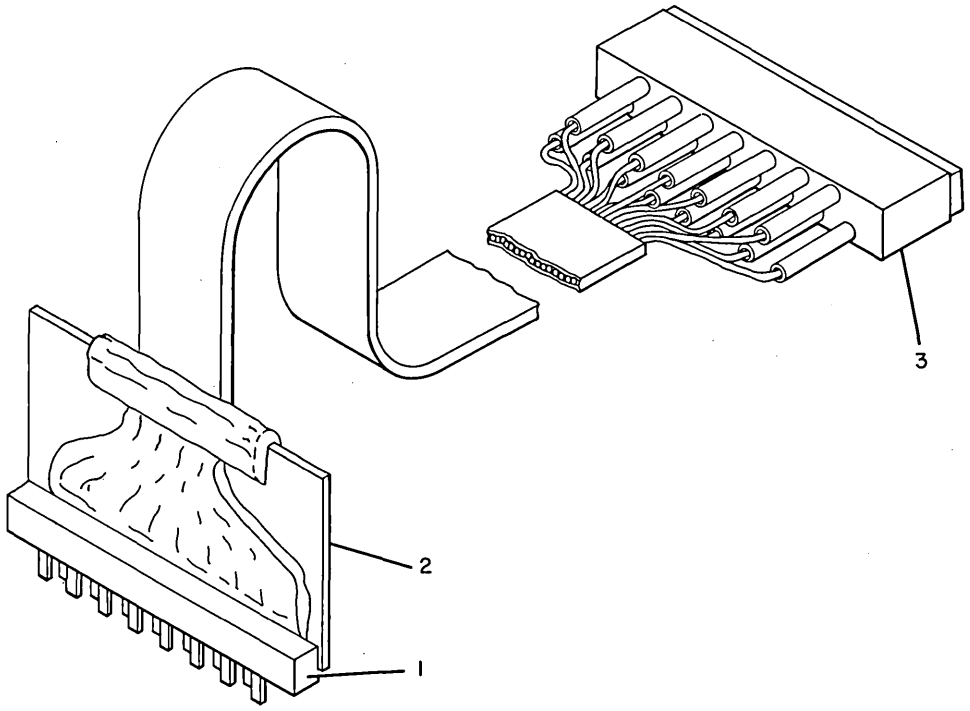


Figure 7-21. Printed Circuit Module Extender

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-21-		PRINTED CIRCUIT MODULE EXTENDER	ØNØ68146	1	
-1		. CONNECTOR, receptacle, electrical (16512) (DOD no. ØN123180-1)	A-2333-Ø9	1	
-2		. BOARD, detail and printed wiring (9Ø536)	245304-ØØ	1	
-3		. CONNECTOR, receptacle, electrical (Ø266Ø) (DOD no. ØN123179-1)	143-825	1	

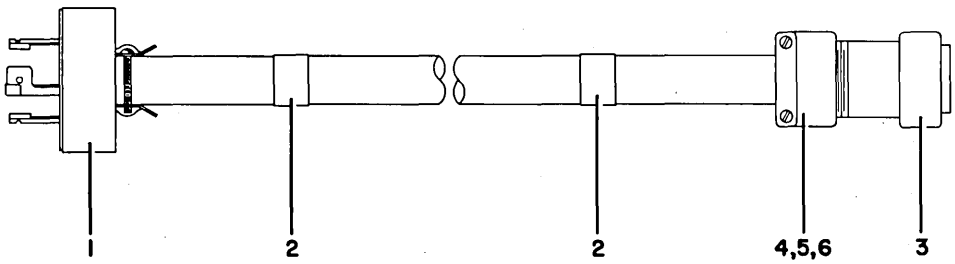


Figure 7-22. Cable Assembly

GROUP ASSEMBLY PARTS LIST

FIG. AND INDEX NO.	REF. DESIGN.	DESCRIPTION	PART NO.	UNITS PER ASSY.	USABLE ON CODE
7-22-		CABLE ASSEMBLY, 20 ft. lg	ØN116647	1	
-1	P1	. CONNECTOR, plug, electrical (74545)	7411	1	
-2		. BAND, marker (DOD no. ØN123Ø45-1)	Coml	2	
-3	P2	. CONNECTOR, plug, electrical	MS31Ø6A2Ø-15SW	1	
-4		. ADAPTER, cable to connector	MS3Ø57-12A	1	
-5		. BUSHING, electrical conductor	MS39Ø56-5	1	
-6		. BUSHING, electrical conductor	MS39Ø56-6	1	

NUMERICAL INDEX

PART NO.	FIG. AND INDEX NO.	QTY PER ART	SOURCE CODE	REPAIR CODE
AN935-B8L	7-2-51	3		
	7-4-2Ø			
AN936-B616B	7-2-54	2		
AO-185668	7-9-3	2		
A17437	7-11-38	2		
A17438	7-11-2Ø	1		
A-2333-Ø9	7-21-1	1		
A2345-1Ø	7-5-61	644		
	7-6-47			
BAND MARKER	7-3-	6		
	7-19-			
	7-22-2			
B8-15	7-12-	2		
CH53BIMF1Ø5K	7-12-4	2		
CL25BH221UP3	7-1Ø-6	8		
	7-11-11			
CPØ9A1KC1Ø4K3	7-4-8	2		
CS-1Ø1	7-1-	1Ø		
CZ24BKF1Ø3	7-4-5	16		
DDM-5ØS	7-9-1	24		
DPD45ØØ-52Ø7	7-18-4	4		
	7-19-2			
	7-19-3			
	7-19-4			
DPD5Ø-34PIGF32A115	7-2-1Ø	9		
FHL17G	7-11-7	18		
FHL18G2-1	7-2-16	25		
	7-3-18			
	7-11-6			
FS31Ø4	7-4-1	1		
FØ2A25ØV3AS	7-2-15	5		
	7-11-1Ø			
FØ2B125V2AS	7-11-2	13		
FØ2B25ØV1AS	7-11-4	5		
FØ3A25ØV1ØAS	7-2-14	14		
	7-3-17			
	7-11-8			
FØ3A25ØV8AS	7-2-13	9		
	7-3-16			
	7-11-9			
FØ3B125V3AS	7-11-3	4		
F03B32V8AS	7-11-1	4		
HKU	7-2-17	8		
	7-3-19			
	7-11-5			
HP-2N	7-5-32	6		
L79NKM-62	7-2-	4		
L79NM-26	7-4-	2		
MBS-S-1838A-9	7-7-13	18		
	7-8-11			
MS15795-8Ø2	7-2-	14		
	7-3-			
	7-4-			
	7-5-			
	7-6-			
MS15795-8Ø3	7-1-	35		
	7-2-			
	7-4-			
	7-9-			
	7-12-			
MS15795-8Ø5	7-1-	252		
	7-2-			
	7-3-			
	7-4-			
	7-5-			
	7-5-5			
	7-6-			
	7-7-			
	7-8-			
	7-11-			
	7-2Ø-			
MS15795-8Ø7	7-1-	65		
	7-2-			
	7-3-			
	7-5-			
	7-6-			
	7-8-			
	7-11-			
	7-12-			
MS15795-8Ø8	7-2-	255		
	7-3-			
	7-5-			
	7-11-			
	7-12-			
MS15795-81Ø	7-5-	8		
	7-6-			
	7-11-			
MS17325-1	7-4-27	1		
MS1783Ø-4F	7-5-29	4		
	7-6-14			
MS21Ø44-CØ4	7-1-	74		

PART NO.	FIG. AND INDEX NO.	QTY PER ART	SOURCE CODE	REPAIR CODE
	7-2-			
	7-8-			
	7-9-			
	7-12-			
MS21Ø44-CØ6	7-1-	128		
	7-2-			
	7-3-			
	7-5-			
	7-6-			
	7-7-			
	7-8-			
	7-11-			
	7-12-			
	7-2Ø-			
MS21Ø44-CØ8	7-2-	24		
	7-3-			
	7-11-			
	7-12-			
MS21Ø44-C3	7-2-	36		
	7-3-			
MS25Ø36-2	7-6-25	2		
MS25Ø36-49	7-2-48	1		
MS25Ø36-5Ø	7-6-27	1		
MS25Ø36-53	7-4-17	2		
MS25Ø36-54	7-6-28	1		
MS25Ø43-2ØC	7-2-34	1		
MS25271-A1	7-11-18	2		
MS3Ø57-12A	7-22-4	1		
MS3Ø57-2ØA	7-3-33	2		
MS31Ø2A2Ø-15PW	7-2-35	1		
MS31Ø2A32-6P	7-11-23	1		
MS31Ø2A32-6PW	7-11-24	1		
MS31Ø6A2Ø-15SW	7-22-3	1		
MS31Ø6A32-6S	7-3-31	1		
MS31Ø6A32-6SW	7-3-32	1		
MS35Ø59-21	7-4-29	1		
MS353Ø7-3Ø5	7-5-12	6		
MS35338-134	7-5-	6		
	7-6-			
MS35338-135	7-4-	26		
	7-1Ø-			
	7-11-			
MS35338-136	7-5-	16		
	7-6-			
	7-11-			
	7-12-			
MS35338-137	7-1-	14		
	7-9-			
MS35338-138	7-2-	32		
	7-3-			
MS35338-139	7-5-	4		
	7-6-			
MS35338-141	7-2-57	2		
MS35489-46	7-6-39	5		
MS35649-224	7-6-	4Ø		
	7-1Ø-			
MS35649-249	7-5-	4		
MS35649-264	7-12-7	1		
MS39Ø56-5	7-22-5	1		
MS39Ø56-6	7-22-6	1		
MS39Ø56-7	7-3-34	2		
MS51Ø23-49	7-5-18	4		
	7-6-2			
MS51957-14	7-4-	8		
MS51957-17	7-1-	4		
MS51957-34	7-5-55	1Ø4		
	7-6-45			
MS51958-65	7-3-	52		
MS51958-67	7-3-	26		
MS51958-68	7-3-	2Ø		
MS51959-25	7-4-	3		
MS91528-1N2B	7-8-17	1		
M221F115Ø4Ø541	7-2-3	2		
	7-3-1			
M221L136Ø4Ø541	7-2-4	2		
	7-3-2			
NUT	7-2-52	6		
	7-2-58			
	7-4-21			
RCØ7GF1Ø4J	7-11-12	3		
RC32GF1ØØJ	7-4-1Ø	5		
RC32GF6R8J	7-1Ø-5	4		
RC32GF681J	7-4-11	5		
RC42GF15ØJ	7-1Ø-4	14		
RE651ØRØ	7-1Ø-1	4		
RE6515RØ	7-1Ø-2	13		
RE6542R2	7-1Ø-3	2		
RF-6Ø-NC-115-6Ø	7-4-3	1		
RY4XX2B3L32	7-4-6	1		
R1Ø9Ø	7-5-41	6		
	7-9-1Ø			
SC-628	7-2-1	1		

NUMERICAL INDEX

PART NO.	FIG. AND INDEX NO.	QTY PER ART	SOURCE CODE	REPAIR CODE
SCREW Ø.25-2ØXØ.5	7-5- 7-6- 7-11-	9		
SCREW Ø.25-28XØ.875	7-2- 7-3-	24		
SCREW Ø.312-18XØ.5	7-1-	8		
SCREW Ø.312-18X1	7-1-	8		
SCREW Ø.375-16X2	7-2-	1		
SCREW 1Ø-32XØ.375	7-9-	12		
SCREW 1Ø-32XØ.438	7-2- 7-3- 7-6-	16		
SCREW 1Ø-32XØ.5	7-2- 7-3-	8		
SCREW 1Ø-32XØ.625	7-1- 7-2- 7-3- 7-5- 7-6- 7-11-	8Ø		
SCREW 1Ø-32XØ.75	7-2- 7-3- 7-6-	96		
SCREW 1Ø-32XØ.875	7-11-	2Ø		
SCREW 1Ø-32X1	7-3-	8		
SCREW 1Ø-32X1.125	7-2-	8		
SCREW 1Ø-32X1.25	7-2- 7-3-	32		
SCREW 2-56XØ.25	7-2- 7-3-	8		
SCREW 2-56XØ.375	7-4- 7-1Ø-	4Ø		
SCREW 2-56XØ.438	7-5-	4		
SCREW 2-56XØ.5	7-6-	2		
SCREW 4-4ØXØ.25	7-1Ø- 7-11-	22		
SCREW 4-4ØXØ.375	7-4-	7		
SCREW 4-4ØXØ.438	7-9-	52		
SCREW 4-4ØXØ.562	7-2-	4		
SCREW 4-4ØXØ.688	7-12-	6		
SCREW 6-32XØ.312	7-3- 7-7- 7-8- 7-19-	52		
SCREW 6-32XØ.375	7-1- 7-2- 7-3- 7-4- 7-5- 7-5-4 7-6- 7-2Ø-	62		
SCREW 6-32XØ.438	7-5-	28		
SCREW 6-32XØ.5	7-1- 7-2- 7-3- 7-6- 7-9- 7-11- 7-18-	117		
SCREW 6-32XØ.562	7-2-	4		
SCREW 6-32XØ.625	7-1- 7-2- 7-4- 7-5-	6Ø		
SCREW 6-32XØ.75	7-11- 7-2Ø-	2Ø		
SCREW 6-32XØ.875	7-11-	6		
SCREW 6-32X1.125	7-11-	1Ø		
SCREW 6-32X1.5	7-12-	2		
SCREW 8-32XØ.25	7-5-	2		
SCREW 8-32XØ.312	7-1- 7-6-	13		
SCREW 8-32XØ.375	7-1-12Ø	24		
SCREW 8-32XØ.438	7-5- 7-6-	53		
SCREW 8-32XØ.5	7-1- 7-2- 7-3- 7-5- 7-6- 7-9- 7-11-	5Ø		
SCREW 8-32XØ.625	7-3- 7-5- 7-6- 7-11-	79		
SCREW 8-32XØ.75	7-2-47	1		

PART NO.	FIG. AND INDEX NO.	QTY PER ART	SOURCE CODE	REPAIR CODE
SCREW 8-32XØ.875	7-4-16	1		
SCREW 8-32X1	7-2-	2Ø		
SCREW 8-32X1.25	7-1-22 7-2-	32		
SCREW 8-32X1.5	7-12-	2		
SP416Ø	7-6-3Ø	1		
SP4167	7-6-29	1		
SS-48151	7-9-6	1Ø		
SS-48152	7-9-5	2		
ST1-6ØØØ-1633	7-7-3 7-8-3	254		
S38Ø7	7-11-15	1		
S3898	7-11-36	1		
S4111B	7-11-37	1		
TS1Ø3PØ3	7-4-4	1		
WASHER, FLAT, NO. 8	7-2-5Ø 7-4-19	4		
WASHER, LOCK, NO. 6	7-6-41	16		
WASHER, LOCK, NO. 8	7-2-49 7-4-18 7-5-51 7-6-	26		
WASHER, NO. Ø.375	7-2-56	3		
WASHER, NO. 2	7-1Ø-	38		
ØNØ64ØØØ	7-15-5	1		
ØNØ64ØØ8	7-13-9 7-14-14 7-15-4	91		
ØNØ64ØØ9	7-13-8 7-14-6 7-15-12 7-16-3	45		
ØNØ64Ø1Ø	7-13-5 7-14-8 7-15-8	92		
ØNØ64Ø11	7-13-6 7-14-9 7-15-3 7-16-6	121		
ØNØ64Ø12	7-13-7 7-14-3 7-15-7 7-16-7 7-17-6	81		
ØNØ64Ø13	7-15-1	1		
ØNØ64Ø15	7-15-15	1		
ØNØ64Ø16	7-14-17 7-15-11	2		
ØNØ64Ø19	7-15-2 7-17-15	17		
ØNØ64Ø21	7-17-18	4		
ØNØ64Ø22	7-17-8	2Ø		
ØNØ64Ø23	7-15-17 7-16-12	11		
ØNØ64Ø24	7-15-14	1		
ØNØ64Ø26	7-16-4	51		
ØNØ67ØØ3	7-4-3Ø	1		
ØNØ67ØØ5	7-2-9	9		
ØNØ67ØØ6	7-2- 7-3-	AR		
ØNØ67ØØ7	7-2-	AR		
ØNØ67ØØ8	7-12-	6		
ØNØ67Ø11	7-12-5	2		
ØNØ67Ø13	7-11-	8		
ØNØ67Ø14	7-11-21	3		
ØNØ67Ø18	7-5-7 7-6-8	2		
ØNØ67Ø27	7-5-59	8		
ØNØ67Ø33	7-5-1	1		
ØNØ67Ø48-1	7-5-63	1		
ØNØ67Ø48-2	7-5-63	1		
ØNØ67Ø5Ø	7-5-62	8		
ØNØ67Ø51-1	7-5-	1		
ØNØ67Ø51-2	7-5-	1		
ØNØ67Ø52	7-5-33	1		
ØNØ67Ø54	7-5-31	1		
ØNØ67Ø55	7-5-23	1		
ØNØ67Ø56	7-5-16	1		
ØNØ67Ø58	7-2-27	1		
ØNØ67Ø59-2	7-2-	2		
ØNØ67Ø62	7-1-	8		
ØNØ67Ø64	7-5-27 7-6-12	8		
ØNØ67Ø65	7-5-6Ø	1		
ØNØ67Ø66	7-5-52	8		
ØNØ67Ø74	7-5-3 7-6-2Ø	2		
ØNØ67115	7-2- 7-3-	AR		
ØNØ67124	7-2-	AR		

NUMERICAL INDEX

PART NO.	FIG. AND INDEX NO.	QTY PER ART	SOURCE CODE	REPAIR CODE
	7-3-			
ØNØ67125	7-2-	AR		
	7-3-			
ØNØ67126	7-2-	AR		
	7-3-			
ØNØ67128	7-2-21	AR		
	7-3-23			
ØNØ67136	7-5-17	1		
ØNØ67138	7-2-22	AR		
	7-3-24			
ØNØ67139	7-2-23	AR		
	7-3-25			
ØNØ672Ø2	7-5-38	1		
ØNØ672Ø3	7-2-2Ø	6		
	7-3-22			
ØNØ67249	7-5-28	8		
	7-6-13			
ØNØ67315	7-18-2	2		
	7-18-5			
ØNØ67324	7-11-22	2		
ØNØ67322	7-2-11	9		
ØNØ67325	7-5-25	1		
ØNØ67332	7-5-5Ø	32		
	7-6-4Ø			
ØNØ67333	7-1-	3		
	7-5-6			
	7-6-			
ØNØ67517	7-14-11	13		
ØNØ6765Ø	7-1Ø-2	1		
ØNØ67739	7-2-8	9		
ØNØ68ØØ1	7-17-2	26		
ØNØ68ØØ2	7-17-9	1		
ØNØ68ØØ3	7-17-17	3		
ØNØ68ØØ4	7-14-19	2		
ØNØ68ØØ5	7-1-	2		
	7-14-16			
ØNØ68ØØ6	7-17-1Ø	1		
ØNØ68ØØ7	7-17-12	1		
ØNØ68ØØ8	7-17-4	5		
ØNØ68Ø17	7-13-14	12		
	7-14-2Ø			
ØNØ68Ø19	7-14-5	6		
ØNØ68Ø21	7-13-13	1		
ØNØ68Ø23	7-13-4	55		
	7-14-13			
	7-15-6			
	7-17-11			
ØNØ68Ø29	7-17-14	1		
ØNØ68Ø31	7-16-2	34		
ØNØ68Ø33	7-17-7	17		
ØNØ681Ø2	7-2-12	9		
ØNØ681Ø4	7-5-42	AR		
ØNØ681Ø5	7-5-2	1		
ØNØ681Ø9-2	7-3-44	2		
ØNØ6811Ø	7-11-34	2		
ØNØ68112	7-11-31	2		
ØNØ68117	7-5-26	4		
	7-6-11			
ØNØ68119	7-5-24	1		
ØNØ68122	7-6-46	8		
ØNØ68124	7-11-32	1		
ØNØ68125	7-11-33	1		
ØNØ68132	7-2-36	1		
ØNØ68133-2	7-1-5	1		
ØNØ68136	7-2-45	4		
	7-3-9			
ØNØ68145	7-5-37	2		
	7-6-17			
ØNØ68146	7-21	2		
ØNØ68147	7-4-	1		
ØNØ68148	7-6-23	1		
ØNØ68149	7-12-8	1		
ØNØ68152	7-2-33	1		
ØNØ68153	7-8-15	2		
ØNØ6816Ø	7-6-38	2		
ØNØ68165-2	7-6-	1		
ØNØ68166	7-6-	1		
ØNØ68167	7-6-49	1		
ØNØ68168	7-6-48	8		
ØNØ68169	7-6-5Ø	1		
ØNØ6817Ø	7-6-21	1		
ØNØ68171	7-6-22	1		
ØNØ68172	7-6-15	1		
ØNØ68173	7-6-16	1		
ØNØ68174	7-6-1Ø	1		
ØNØ68178	7-6-	1		
ØNØ68179	7-6-18	1		
ØNØ6818Ø-2	7-3-	2		
ØNØ68181	7-3-3Ø	1		
ØNØ68182	7-9-14	2		
ØNØ68183	7-9-4	2		
ØNØ68184	7-6-42	8		

PART NO.	FIG. AND INDEX NO.	QTY PER ART	SOURCE CODE	REPAIR CODE
ØNØ68192	7-1-2	3		
	7-5-3			
	7-6-2Ø			
ØNØ68194	7-5-4Ø	1		
ØNØ68194-2	7-6-37	1		
ØNØ68197	7-5-39	2		
	7-6-36			
ØNØ68198	7-19-	1		
ØNØ68199	7-19-	1		
ØNØ682Ø0	7-19-	1		
ØNØ682Ø1	7-19-	1		
ØNØ682Ø3	7-5-	2		
	7-6-			
ØNØ682Ø4	7-2-2	1		
ØNØ682Ø5	7-19-1	4		
ØNØ682Ø6	7-5-	2		
	7-6-			
ØNØ682Ø9	7-17-5	1		
ØNØ6821Ø	7-17-5	1		
ØNØ68211	7-11-17	2		
ØNØ68212	7-2-43	1		
ØNØ68213	7-2-44	3		
ØNØ68218-2	7-1-	1		
ØNØ68219-2	7-1-3	1		
ØNØ6822Ø	7-3-42	2		
ØNØ68221	7-11-28	AR		
ØNØ68228-2	7-2-	1		
ØNØ68229	7-6-1	4		
ØNØ6823Ø-2	7-2-38	1		
ØNØ68238-2	7-1-4	1		
ØNØ68239	7-11-16	1		
ØNØ68247	7-4-12	1		
ØNØ68251	7-1-1	2		
ØNØ68255-1	7-7-9	1		
ØNØ68255-2	7-7-1Ø	1		
ØNØ68256	7-7-16	2		
ØNØ68257	7-7-14	2		
ØNØ68258-2	7-8-21	1		
ØNØ6826Ø	7-18-	1		
ØNØ68261	7-8-13	2		
ØNØ68263	7-8-16	1		
ØNØ68268	7-8-12	2		
ØNØ6827Ø	7-7-2	2		
	7-8-1			
ØNØ68271	7-7-1	1		
ØNØ68272	7-8-2	1		
ØNØ68273	7-7-17	2		
ØNØ68279	7-7-15	2		
ØNØ68281	7-5-56	56		
ØNØ7176Ø	7-13-2	92		
	7-14-12			
ØNØ71761	7-13-3	37		
	7-14-7			
	7-15-9			
	7-16-9			
	7-17-3			
ØNØ71762	7-13-1Ø	16		
	7-14-15			
	7-15-1Ø			
	7-16-1Ø			
ØNØ71764	7-13-11	15		
	7-14-1Ø			
	7-15-13			
	7-16-8			
ØNØ71768	7-14-18	1		
ØNØ71774	7-13-12	21		
	7-14-4			
	7-15-18			
	7-16-5			
ØNØ71777	7-13-1	28		
	7-14-1			
	7-15-16			
	7-16-1			
ØNØ71779	7-14-2	2		
ØN1163Ø6	7-18-8	2		
ØN1163Ø7	7-18-3	2		
ØN1163Ø8	7-18-1	2		
ØN116314-4	7-18-7	1		
ØN116448-2	7-2-5	1		
ØN116448-3	7-3-3	1		
ØN116463-1	7-1-19	4		
ØN116625	7-2-26	2		
	7-3-29			
ØN116626	7-5-19	4		
	7-6-3			
ØN116627	7-5-21	2		
	7-6-5			
ØN116645	7-22-	1		
ØN116647	7-22-	1		
ØN116657-2	7-18-	1		
ØN116661	7-5-11	1		
ØN116671	7-5-9	5		

NUMERICAL INDEX

PART NO.	FIG. AND INDEX NO.	QTY PER ART	SOURCE CODE	REPAIR CODE
	7-6-6			
ØN116800	7-1-	1		
ØN116801-1	7-1-11	1		
ØN116801-2	7-1-12	1		
ØN116802-1	7-1-13	1		
ØN116803-1	7-5-	1		
ØN116803-2	7-5-	1		
ØN116804-1	7-5-64	1		
ØN116804-2	7-5-64	1		
ØN116805	7-2-	1		
ØN116806	7-5-10	1		
ØN116807-1	7-1-31	1		
ØN116807-2	7-1-33	2		
ØN116807-3	7-1-32	1		
ØN116808	7-6-19	1		
ØN116810	7-5-10	1		
ØN116811	7-11-14	1		
ØN116812	7-1-8	1		
ØN116813-1	7-5-	1		
ØN116813-2	7-5-	1		
ØN116814	7-6-7	1		
ØN116815	7-6-7	1		
ØN116816	7-1-9	1		
ØN116817	7-4-33	1		
ØN116818	7-4-32	1		
ØN116819	7-1-6	1		
ØN116820	7-4-22	1		
ØN116821	7-4-30	1		
ØN116823-1	7-2-46	1		
ØN116823-2	7-3-40	1		
ØN116824-1	7-3-41	1		
ØN116824-2	7-2-46	1		
ØN116825	7-11-39	1		
ØN116826	7-1-16	1		
ØN116828	7-3-10	1		
ØN116829	7-11-25	1		
ØN116830	7-3-47	1		
ØN116831	7-3-46	1		
ØN116832	7-3-4	1		
ØN116833	7-3-43	1		
ØN116836	7-7-19	1		
ØN116837	7-8-23	1		
ØN116838	7-8-23	1		
ØN116839	7-7-18	1		
ØN116840	7-1-21	8		
ØN116841-1	7-1-18	4		
ØN116842	7-5-49	1		
ØN116843	7-1-17	2		
ØN116844	7-12-10	1		
ØN116845	7-3-8	1		
ØN116846	7-4-	1		
ØN116847	7-4-7	1		
ØN116848-1	7-2-19	2		
	7-3-21			
ØN116848-2	7-2-18	2		
	7-3-20			
ØN116850-1	7-1-27	8		
ØN116850-2	7-1-28	10		
ØN116851-1	7-2-29	8		
	7-3-12			
ØN116851-4	7-2-28	10		
	7-3-11			
ØN116852-1	7-2-30	AR		
	7-3-13			
ØN116852-2	7-2-31	AR		
	7-3-14			
ØN116852-3	7-2-32	AR		
	7-3-15			
ØN116853-1	7-1-26	2		
ØN116854	7-1-23	8		
ØN116856	7-1-29	1		
ØN116857-2	7-1-15	1		
ØN116858-2	7-4-31	1		
ØN116859	7-1-24	8		
ØN116861	7-3-38	1		
ØN116862	7-9-13	2		
ØN116863-1	7-2-39	1		
ØN116863-2	7-2-40	1		
ØN123195-24	7-8-	76		
ØN123319-6	7-5-8	AR		
	7-6-9			
ØN123319-10	7-1-10	AR		
ØN123319-11	7-1-7	AR		
ØN123319-17	7-2-42	AR		
	7-3-9			
ØN123363-15	7-3-45	AR		
ØN123363-34	7-2-41	AR		
Ø6-Ø32Ø2-TO BE EST	7-3-7	1		
1NØ56S1Ø5UA	7-8-18	1		
1N1186	7-5-11	30		
	7-6-26			
	7-11-30			
1N284RB	7-5-14	3		

PART NO.	FIG. AND INDEX NO.	QTY PER ART	SOURCE CODE	REPAIR CODE
	7-6-31			
1N4086	7-4-5	1		
1112-1	7-7-5	149		
1112-2	7-7-6	122		
	7-7-11			
	7-8-6			
	7-8-9			
1120-12-CPDD	7-7-7	172		
	7-7-12			
	7-8-7			
	7-8-10			
13AT401-T2	7-8-20	1		
13AT403-T2	7-4-23	6		
	7-8-19			
143-825	7-21-3	1		
15S11-1AC-15S1-7-1AC	7-4-	2		
15R1-1AC-15R10-1AC	7-4-	2		
1826	7-4-24	6		
2AC6	7-3-36	1		
20JX31	7-2-37	3		
224S-1-102(M)	7-9-7	2		
224S-1-150(M)	7-9-8	8		
245304-00	7-21-2	1		
2510-2	7-4-2	1		
26TB12	7-10-1	2		
26TB8	7-4-14	1		
322055	7-2-55	1		
344	7-7-4	254		
	7-8-4			
350235-B	7-2-6	4		
	7-3-6			
350235-T	7-2-7	4		
	7-3-5			
361Ø049-4	7-2-25	1512		
3614679	7-3-25	4		
3614680	7-20-1	3		
3614791-4-361Ø01ØW	7-3-28	193		
	7-5-36			
3614792-4-361Ø013	7-3-27	77		
	7-6-34			
3614798-2-361Ø01ØW	7-5-45	337		
	7-6-35			
3614875	7-2-24	8		
3617351	7-5-43	1		
3650-1-05	7-4-9	26		
	7-10-7			
	7-11-13			
350266-L	7-11-27	1		
350266-R	7-11-26	1		
37TB-11	7-11-29	2		
40829	7-5-54	28		
47309	7-6-44	28		
5C11A9	7-5-34	42		
5191761-12A-529ØØØ9	7-9-12	368		
5191884-12B-529ØØØ9	7-9-11	368		
603-1/4	7-5-20	4		
	7-6-4			
62-99-193-10	7-1-25	16		
654DS	7-12-3	2		
7411	7-22-1	1		
79LH1660-26	7-2-	8		
	7-3-			
79LH1660-40	7-4-	10		
79Ø1489-ØØ	7-1-30	4		
8L2-FF	7-5-22	1		
8L3-FF	7-9-2	2		
8038-1G13	7-5-15	3		
	7-5-15			
	7-6-32			
81-041Ø-0111-203	7-4-23	4		
81-041Ø-0112-203	7-4-24	4		
8869-K4	7-9-9	2		
9Ø8-1166-1634-526	7-7-	177		

REFERENCE DESIGNATOR INDEX

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A1	7-1-11	ØN1168Ø1-Ø1
A1A1	7-5	ØN1168Ø3-Ø1
A1A1A1A	7-13-1	ØNØ71777
thru		
A1A1A1G	7-13-1	ØNØ71777
A1A1A1ØA	7-13-6	ØN064Ø11
A1A1A1ØB	7-13-6	ØNØ64Ø11
A1A1A1ØC	7-13-8	ØNØ64Ø09
A1A1A1ØD	7-13-4	ØNØ68Ø23
A1A1A1ØE	7-13-8	ØNØ64Ø09
A1A1A1ØF	7-13-6	ØNØ64Ø11
A1A1A1ØG	7-13-6	ØNØ64Ø11
A1A1A11A	7-13-8	ØNØ64Ø09
A1A1A11B	7-13-8	ØNØ64Ø09
A1A1A11C	7-13-8	ØNØ64Ø09
A1A1A11D	7-13-7	ØNØ64Ø12
A1A1A11E	7-13-8	ØNØ64Ø09
A1A1A11F	7-13-8	ØNØ64Ø09
A1A1A11G	7-13-8	ØNØ64Ø09
A1A1A12A	7-13-8	ØNØ64Ø09
A1A1A12B	7-13-8	ØNØ64Ø09
A1A1A12C	7-13-4	ØNØ68Ø23
A1A1A12D	7-13-4	ØNØ68Ø23
A1A1A12E	7-13-4	ØNØ68Ø23
A1A1A12F	7-13-8	ØNØ64Ø09
A1A1A12G	7-13-8	ØNØ64Ø09
A1A1A13B	7-13-7	ØNØ64Ø12
A1A1A13D	7-13-4	ØNØ68Ø23
A1A1A13F	7-13-7	ØNØ64Ø12
A1A1A13G	7-13-4	ØNØ68Ø23
A1A1A14A	7-13-2	ØNØ7176Ø
thru		
A1A1A14G	7-13-2	ØNØ7176Ø
A1A1A15A	7-13-8	ØNØ64Ø09
thru		
A1A1A15G	7-13-8	ØNØ64Ø09
A1A1A16B	7-13-5	ØNØ64Ø1Ø
A1A1A16C	7-13-4	ØNØ68Ø23
A1A1A16D	7-13-4	ØNØ68Ø23
A1A1A16E	7-13-4	ØNØ68Ø23
A1A1A16F	7-13-5	ØNØ64Ø1Ø
A1A1A16G	7-13-9	ØNØ64Ø08
A1A1A17A	7-13-2	ØNØ7176Ø
thru		
A1A1A17G	7-13-2	ØNØ7176Ø
A1A1A18A	7-13-2	ØNØ7176Ø
thru		
A1A1A18G	7-13-2	ØNØ7176Ø
A1A1A19A	7-13-5	ØNØ64Ø1Ø
A1A1A19B	7-13-7	ØNØ64Ø12
A1A1A19C	7-13-5	ØNØ64Ø1Ø
A1A1A19D	7-13-4	ØNØ68Ø23
A1A1A19E	7-13-5	ØNØ64Ø1Ø
A1A1A19F	7-13-7	ØNØ64Ø12
A1A1A19G	7-13-5	ØNØ64Ø1Ø
A1A1A2ØA	7-13-5	ØNØ64Ø1Ø
thru		
A1A1A2ØG	7-13-5	ØNØ64Ø1Ø
A1A1A21A	7-13-7	ØNØ64Ø12
thru		
A1A1A21D	7-13-7	ØNØ64Ø12
A1A1A21E	7-13-4	ØNØ68Ø23
A1A1A21F	7-13-7	ØNØ64Ø12
A1A1A21G	7-13-7	ØNØ64Ø12
A1A1A22A	7-13-5	ØNØ64Ø1Ø
thru		
A1A1A22G	7-13-5	ØNØ64Ø1Ø
A1A1A23A	7-13-5	ØNØ64Ø1Ø
thru		
A1A1A23G	7-13-5	ØNØ64Ø1Ø
A1A1A24A	7-13-7	ØNØ64Ø12
A1A1A24B	7-13-1Ø	ØNØ71762
A1A1A24C	7-13-4	ØNØ68Ø23
A1A1A24D	7-13-4	ØNØ68Ø23
A1A1A24E	7-13-4	ØNØ68Ø23
A1A1A24F	7-13-1Ø	ØNØ71762
A1A1A24G	7-13-5	ØNØ64Ø1Ø
A1A1A25A	7-13-2	ØNØ7176Ø
thru		
A1A1A25G	7-13-2	ØNØ7176Ø
A1A1A26A	7-13-2	ØNØ7176Ø
thru		
A1A1A26G	7-13-2	ØNØ7176Ø
A1A1A27A	7-13-2	ØNØ7176Ø
thru		
A1A1A27G	7-13-2	ØNØ7176Ø
A1A1A28A	7-13-2	ØNØ7176Ø
thru		
A1A1A28G	7-13-2	ØNØ7176Ø
A1A1A29A	7-13-7	ØNØ64Ø12
A1A1A29B	7-13-11	ØNØ71764
A1A1A29C	7-13-4	ØNØ68Ø23
A1A1A29D	7-13-4	ØNØ68Ø23
A1A1A29E	7-13-4	ØNØ68Ø23
A1A1A29F	7-13-11	ØNØ71764
A1A1A29G	7-13-5	ØNØ64Ø1Ø
A1A1A3ØA	7-13-2	ØNØ7176Ø
thru		
A1A1A3ØG	7-13-2	ØNØ7176Ø
A1A1A31A	7-13-2	ØNØ7176Ø
thru		
A1A1A31G	7-13-2	ØNØ7176Ø
A1A1A32A	7-13-5	ØNØ64Ø1Ø
A1A1A32B	7-13-5	ØNØ64Ø1Ø
A1A1A32C	7-13-4	ØNØ68Ø23
A1A1A32D	7-13-4	ØNØ68Ø23
A1A1A32E	7-13-4	ØNØ68Ø23
A1A1A32F	7-13-5	ØNØ64Ø1Ø
A1A1A33A	7-13-8	ØNØ64Ø09
A1A1A33B	7-13-8	ØNØ64Ø09
A1A1A33C	7-13-7	ØNØ64Ø12
A1A1A33D	7-13-5	ØNØ64Ø1Ø
A1A1A33E	7-13-5	ØNØ64Ø1Ø
A1A1A33G	7-13-14	ØNØ68Ø17
A1A1A34A	7-13-12	ØNØ71774
thru		
A1A1A34G	7-13-12	ØNØ71774
A1A1A35A	7-13-14	ØNØ68Ø17
thru		
A1A1A35D	7-13-14	ØNØ68Ø17
A1A1A35E	7-13-13	ØNØ68Ø21
A1A1A35F	7-13-14	ØNØ68Ø17
A1A1A35G	7-13-14	ØNØ68Ø17
A1A1A4A	7-13-2	ØNØ7176Ø
thru		
A1A1A4G	7-13-2	ØNØ7176Ø
A1A1A5A	7-13-2	ØNØ7176Ø
thru		
A1A1A5G	7-13-2	ØNØ7176Ø
A1A1A6A	7-13-5	ØNØ64Ø1Ø
A1A1A6B	7-13-4	ØNØ68Ø23
thru		
A1A1A6E	7-13-4	ØNØ68Ø23
A1A1A6F	7-13-3	ØNØ71761
A1A1A6G	7-13-3	ØNØ71761
A1A1A7A	7-13-2	ØNØ7176Ø
thru		
A1A1A7G	7-13-2	ØNØ7176Ø
A1A1A8A	7-13-2	ØNØ7176Ø
thru		
A1A1A8G	7-13-2	ØNØ7176Ø
A1A1A9A	7-13-6	ØNØ64Ø11
A1A1A9B	7-13-6	ØNØ64Ø11
A1A1A9C	7-13-7	ØNØ64Ø12
A1A1A9D	7-13-4	ØNØ68Ø23
A1A1A9E	7-13-4	ØNØ68Ø23
A1A1A9F	7-13-6	ØNØ64Ø11
A1A1A9G	7-13-6	ØNØ64Ø11
A1A1C1	7-5-34	5C11A9
thru		
A1A1C42	7-5-34	5C11A9
A1A1J1A	7-5-61	A2345-1Ø
thru		
A1A1J1G	7-5-61	A2345-1Ø
A1A1J1ØA	7-5-61	A2345-1Ø
thru		
A1A1J1ØG	7-5-61	A2345-1Ø
A1A1J11A	7-5-61	A2345-1Ø
thru		
A1A1J11G	7-5-61	A2345-1Ø
A1A1J12A	7-5-61	A2345-1Ø
thru		
A1A1J12G	7-5-61	A2345-1Ø
A1A1J13A	7-5-61	A2345-1Ø
thru		
A1A1J13G	7-5-61	A2345-1Ø
A1A1J14A	7-5-61	A2345-1Ø
thru		
A1A1J14G	7-5-61	A2345-1Ø
A1A1J15A	7-5-61	A2345-1Ø
thru		
A1A1J15G	7-5-61	A2345-1Ø
A1A1J16A	7-5-61	A2345-1Ø
thru		
A1A1J16G	7-5-61	A2345-1Ø
A1A1J17A	7-5-61	A2345-1Ø
thru		
A1A1J17G	7-5-61	A2345-1Ø
A1A1J18A	7-5-61	A2345-1Ø
thru		
A1A1J18G	7-5-61	A2345-1Ø
A1A1J19A	7-5-61	A2345-1Ø
thru		
A1A1J19G	7-5-61	A2345-1Ø

REFERENCE DESIGNATOR INDEX

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A1A1J2A	7-5-61	A2345-1Ø
thru		
A1A1J2G	7-5-61	A2345-1Ø
A1A1J2ØA	7-5-61	A2345-1Ø
thru		
A1A1J2ØG	7-5-61	A2345-1Ø
A1A1J21A	7-5-61	A2345-1Ø
thru		
A1A1J21G	7-5-61	A2345-1Ø
A1A1J22A	7-5-61	A2345-1Ø
thru		
A1A1A22G	7-5-61	A2345-1Ø
A1A1A23A	7-5-61	A2345-1Ø
thru		
A1A1A23G	7-5-61	A2345-1Ø
A1A1A24A	7-5-61	A2345-1Ø
thru		
A1A1A24G	7-5-61	A2345-1Ø
A1A1A25A	7-5-61	A2345-1Ø
thru		
A1A1A25G	7-5-61	A2345-1Ø
A1A1A26A	7-5-61	A2345-1Ø
thru		
A1A1A26G	7-5-61	A2345-1Ø
A1A1J27A	7-5-61	A2345-1Ø
thru		
A1A1J27G	7-5-61	A2345-1Ø
A1A1J28A	7-5-61	A2345-1Ø
thru		
A1A1J28G	7-5-61	A2345-1Ø
A1A1J29A	7-5-61	A2345-1Ø
thru		
A1A1J29G	7-5-61	A2345-1Ø
A1A1J3A	7-5-61	A2345-1Ø
thru		
A1A1J3G	7-5-61	A2345-1Ø
A1A1J3ØA	7-5-61	A2345-1Ø
thru		
A1A1J3ØG	7-5-61	A2345-1Ø
A1A1J31A	7-5-61	A2345-1Ø
thru		
A1A1J31G	7-5-61	A2345-1Ø
A1A1J32A	7-5-61	A2345-1Ø
thru		
A1A1J32G	7-5-61	A2345-1Ø
A1A1J33A	7-5-61	A2345-1Ø
thru		
A1A1J33G	7-5-61	A2345-1Ø
A1A1J34A	7-5-61	A2345-1Ø
thru		
A1A1J34G	7-5-61	A2345-1Ø
A1A1J35A	7-5-61	A2345-1Ø
thru		
A1A1J35G	7-5-61	A2345-1Ø
A1A1J4A	7-5-61	A2345-1Ø
thru		
A1A1J4G	7-5-61	A2345-1Ø
A1A1J5A	7-5-61	A2345-1Ø
thru		
A1A1J5G	7-5-61	A2345-1Ø
A1A1J6A	7-5-61	A2345-1Ø
thru		
A1A1J6G	7-5-61	A2345-1Ø
A1A1J7A	7-5-61	A2345-1Ø
thru		
A1A1J7G	7-5-61	A2345-1Ø
A1A1J8A	7-5-61	A2345-1Ø
thru		
A1A1J8G	7-5-61	A2345-1Ø
A1A1J9A	7-5-61	A2345-1Ø
thru		
A1A1J9G	7-5-61	A2345-1Ø
A1A1P1	7-5-35	3614676
A1A1P2	7-5-35	3614676
A1A1TB1	7-5-43	3617351
A1A1TB2	7-5-44	No Number
A1A2	7-5	ØN116813-1
A1A2A1A	7-14-1	ØNØ71777
thru		
A1A2A1G	7-14-1	ØNØ71777
A1A2A1ØA	7-14-12	ØNØ71760
A1A2A1ØB	7-14-12	ØNØ71760
A1A2A1ØC	7-14-12	ØNØ71760
A1A2A1ØD	7-14-11	ØNØ67517
A1A2A1ØE	7-14-13	ØNØ68023
A1A2A1ØF	7-14-12	ØNØ71760
A1A2A1ØG	7-14-12	ØNØ71760
A1A2A11A	7-14-12	ØNØ71760
A1A2A11B	7-14-12	ØNØ71760
A1A2A11C	7-14-12	ØNØ71760
A1A2A11D	7-14-11	ØNØ67517

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A1A2A11E	7-14-14	ØNØ64ØØ8
A1A2A11F	7-14-12	ØNØ71760
A1A2A11G	7-14-12	ØNØ71760
A1A2A12A	7-14-3	ØNØ64Ø12
A1A2A12B	7-14-8	ØNØ64Ø1Ø
A1A2A12C	7-14-6	ØNØ64ØØ9
thru		
A1A2A12F	7-14-6	ØNØ64ØØ9
A1A2A12G	7-14-11	ØNØ67517
A1A2A13A	7-14-8	ØNØ64Ø1Ø
A1A2A13B	7-14-8	ØNØ64Ø1Ø
A1A2A13C	7-14-8	ØNØ64Ø1Ø
A1A2A13D	7-14-3	ØNØ64Ø12
A1A2A13E	7-14-3	ØNØ64Ø12
A1A2A13F	7-14-8	ØNØ64Ø1Ø
A1A2A13G	7-14-8	ØNØ64Ø1Ø
A1A2A14A	7-14-3	ØNØ64Ø12
A1A2A14B	7-14-3	ØNØ64Ø12
A1A2A14C	7-14-3	ØNØ64Ø12
A1A2A14D	7-14-8	ØNØ64Ø1Ø
A1A2A14E	7-14-8	ØNØ64Ø1Ø
A1A2A14F	7-14-3	ØNØ64Ø12
A1A2A14G	7-14-3	ØNØ64Ø12
A1A2A15A	7-14-8	ØNØ64Ø1Ø
A1A2A15B	7-14-8	ØNØ64Ø1Ø
A1A2A15C	7-14-8	ØNØ64Ø1Ø
A1A2A15D	7-14-15	ØNØ71762
A1A2A15E	7-14-15	ØNØ71762
A1A2A15F	7-14-8	ØNØ64Ø1Ø
A1A2A15G	7-14-8	ØNØ64Ø1Ø
A1A2A16A	7-14-8	ØNØ64Ø1Ø
thru		
A1A2A16D	7-14-8	ØNØ64Ø1Ø
A1A2A16E	7-14-9	ØNØ64Ø11
A1A2A16F	7-14-8	ØNØ64Ø1Ø
A1A2A16G	7-14-8	ØNØ64Ø1Ø
A1A2A17A	7-14-12	ØNØ71760
A1A2A17B	7-14-12	ØNØ71760
A1A2A17C	7-14-12	ØNØ71760
A1A2A17D	7-14-11	ØNØ67517
A1A2A17E	7-14-12	ØNØ71760
A1A2A17F	7-14-12	ØNØ71760
A1A2A17G	7-14-3	ØNØ64Ø12
A1A2A18A	7-14-12	ØNØ71760
A1A2A18B	7-14-12	ØNØ71760
A1A2A18C	7-14-12	ØNØ71760
A1A2A18D	7-14-11	ØNØ67517
A1A2A18E	7-14-12	ØNØ71760
A1A2A18F	7-14-12	ØNØ71760
A1A2A18G	7-14-3	ØNØ64Ø12
A1A2A19A	7-14-12	ØNØ71760
A1A2A19B	7-14-12	ØNØ71760
A1A2A19C	7-14-12	ØNØ71760
A1A2A19D	7-14-11	ØNØ67517
A1A2A19E	7-14-12	ØNØ71760
A1A2A19F	7-14-12	ØNØ71760
A1A2A2A	7-14-2	ØNØ71779
A1A2A2B	7-14-3	ØNØ64Ø12
A1A2A2C	7-14-2	ØNØ71779
A1A2A2D	7-14-4	ØNØ71774
A1A2A2G	7-14-3	ØNØ64Ø12
A1A2A2ØA	7-14-12	ØNØ71760
A1A2A2ØB	7-14-12	ØNØ71760
A1A2A2ØC	7-14-12	ØNØ71760
A1A2A2ØD	7-14-11	ØNØ67517
A1A2A2ØE	7-14-12	ØNØ71760
A1A2A2ØF	7-14-12	ØNØ71760
A1A2A2ØG	7-14-14	ØNØ64ØØ8
A1A2A21A	7-14-7	ØNØ71761
A1A2A21B	7-14-1Ø	ØNØ71764
A1A2A21C	7-14-13	ØNØ68Ø23
A1A2A21D	7-14-11	ØNØ67517
A1A2A21E	7-14-13	ØNØ68Ø23
A1A2A21G	7-14-8	ØNØ64Ø1Ø
A1A2A22A	7-14-12	ØNØ71760
A1A2A22B	7-14-12	ØNØ71760
A1A2A22C	7-14-12	ØNØ71760
A1A2A22D	7-14-11	ØNØ67517
A1A2A22E	7-14-12	ØNØ71760
A1A2A22F	7-14-12	ØNØ71760
A1A2A22G	7-14-2Ø	ØNØ68Ø17
A1A2A23A	7-14-12	ØNØ71760
A1A2A23B	7-14-12	ØNØ71760
A1A2A23C	7-14-12	ØNØ71760
A1A2A23D	7-14-11	ØNØ67517
A1A2A23E	7-14-12	ØNØ71760
A1A2A23F	7-14-12	ØNØ71760
A1A2A23G	7-14-2Ø	ØNØ68Ø17
A1A2A24A	7-14-2Ø	ØNØ68Ø17
A1A2A24B	7-14-2Ø	ØNØ68Ø17
A1A2A24C	7-14-1Ø	ØNØ71764

REFERENCE DESIGNATOR INDEX

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A1A2A24D	7-14-1Ø	ØNØ71764
A1A2A24E	7-14-8	ØNØ64Ø1Ø
A1A2A24F	7-14-9	ØNØ64Ø11
A1A2A25A	7-14-2Ø	ØNØ68Ø17
A1A2A25B	7-14-3	ØNØ64Ø12
A1A2A25C	7-14-8	ØNØ64Ø1Ø
A1A2A25D	7-14-8	ØNØ64Ø1Ø
A1A2A25E	7-14-3	ØNØ64Ø12
A1A2A25F	7-14-3	ØNØ64Ø12
A1A2A25G	7-14-3	ØNØ64Ø12
A1A2A26A thru	7-14-14	ØNØ64ØØ8
A1A2A26E	7-14-14	ØNØ64ØØ8
A1A2A26G	7-14-9	ØNØ64Ø11
A1A2A27A thru	7-14-14	ØNØ64ØØ8
A1A2A27E	7-14-14	ØNØ64ØØ8
A1A2A27F	7-14-7	ØNØ71761
A1A2A27G	7-14-7	ØNØ71761
A1A2A28A	7-14-9	ØNØ64Ø11
A1A2A28C	7-14-7	ØNØ71761
A1A2A28D	7-14-13	ØNØ68Ø23
A1A2A28E	7-14-13	ØNØ68Ø23
A1A2A28F	7-14-3	ØNØ64Ø12
A1A2A28G	7-14-14	ØNØ64ØØ8
A1A2A29A thru	7-14-14	ØNØ64ØØ8
A1A2A29G	7-14-14	ØNØ64ØØ8
A1A2A23A	7-14-5	ØNØ68Ø19
A1A2A3B	7-14-6	ØNØ64ØØ9
A1A2A3C	7-14-7	ØNØ71761
A1A2A3D	7-14-4	ØNØ71774
A1A2A3E	7-14-3	ØNØ64Ø12
A1A2A3ØA thru	7-14-14	ØNØ64ØØ8
A1A2A3ØG	7-14-14	ØNØ64ØØ8
A1A2A31A	7-14-9	ØNØ64Ø11
A1A2A31B	7-14-9	ØNØ64Ø11
A1A2A31C	7-14-13	ØNØ68Ø23
A1A2A31D	7-14-13	ØNØ68Ø23
A1A2A31E	7-14-13	ØNØ68Ø23
A1A2A31F	7-14-3	ØNØ64Ø12
A1A2A32A	7-14-4	ØNØ71774
A1A2A32B	7-14-4	ØNØ71774
A1A2A32C	7-14-14	ØNØ64ØØ8
A1A2A32D	7-14-14	ØNØ64ØØ8
A1A2A32G	7-14-14	ØNØ64ØØ8
A1A2A33A	7-14-4	ØNØ71774
A1A2A33B	7-14-4	ØNØ71774
A1A2A33C	7-14-3	ØNØ64Ø12
A1A2A33D	7-14-9	ØNØ64Ø11
A1A2A33E	7-14-16	ØNØ64ØØ5
A1A2A33G	7-14-14	ØNØ64ØØ8
A1A2A34C	7-14-17	ØNØ64Ø16
A1A2A34D	7-14-18	ØNØ71768
A1A2A34E	7-14-19	ØNØ68ØØ4
A1A2A34F	7-14-19	ØNØ68ØØ4
A1A2A4A	7-14-8	ØNØ64Ø1Ø
A1A2A4B	7-14-8	ØNØ64Ø1Ø
A1A2A4C	7-14-7	ØNØ71761
A1A2A4D	7-14-9	ØNØ64Ø11
A1A2A4E	7-14-7	ØNØ71761
A1A2A4G	7-14-1Ø	ØNØ71764
A1A2A5A thru	7-14-8	ØNØ64Ø1Ø
A1A2A5F	7-14-8	ØNØ64Ø1Ø
A1A2A5G	7-14-7	ØNØ71761
A1A2A6A	7-14-11	ØNØ67517
A1A2A6B	7-14-3	ØNØ64Ø12
A1A2A6C	7-14-3	ØNØ64Ø12
A1A2A6D	7-14-8	ØNØ64Ø1Ø
A1A2A6E	7-14-3	ØNØ64Ø12
A1A2A6F	7-14-3	ØNØ64Ø12
A1A2A6G	7-14-8	ØNØ64Ø1Ø
A1A2A7A thru	7-14-9	ØNØ64Ø11
A1A2A7G	7-14-9	ØNØ64Ø11
A1A2A8A	7-14-6	ØNØ64ØØ9
A1A2A8B	7-14-6	ØNØ64ØØ9
A1A2A8C	7-14-6	ØNØ64ØØ9
A1A2A8D	7-14-9	ØNØ64Ø11
A1A2A8E	7-14-6	ØNØ64ØØ9
A1A2A8F	7-14-6	ØNØ64ØØ9
A1A2A8G	7-14-6	ØNØ64ØØ9
A1A2A9A	7-14-6	ØNØ64ØØ9
A1A2A9B	7-14-6	ØNØ64ØØ9
A1A2A9C	7-14-6	ØNØ64ØØ9
A1A2A9D	7-14-11	ØNØ67517
A1A2A9E	7-14-6	ØNØ64ØØ9
A1A2A9F	7-14-6	ØNØ64ØØ9
A1A2A9G	7-14-6	ØNØ64ØØ9

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A1A2C1 thru	7-5-34	5C11A9
A1A2C42	7-5-34	5C11A9
A1A2J1A thru	7-5-61	A2345-1Ø
A1A2J1G	7-5-61	A2345-1Ø
A1A2J1ØA thru	7-5-61	A2345-1Ø
A1A2J1ØG	7-5-61	A2345-1Ø
A1A2J11A thru	7-5-61	A2345-1Ø
A1A2J11G	7-5-61	A2345-1Ø
A1A2J12A thru	7-5-61	A2345-1Ø
A1A2J12G	7-5-61	A2345-1Ø
A1A2J13A thru	7-5-61	A2345-1Ø
A1A2J13G	7-5-61	A2345-1Ø
A1A2J14A thru	7-5-61	A2345-1Ø
A1A2J14G	7-5-61	A2345-1Ø
A1A2J15A thru	7-5-61	A2345-1Ø
A1A2J15G	7-5-61	A2345-1Ø
A1A2J16A thru	7-5-61	A2345-1Ø
A1A2J16G	7-5-61	A2345-1Ø
A1A2J17A thru	7-5-61	A2345-1Ø
A1A2J17G	7-5-61	A2345-1Ø
A1A2J18A thru	7-5-61	A2345-1Ø
A1A2J18G	7-5-61	A2345-1Ø
A1A2J19A thru	7-5-61	A2345-1Ø
A1A2J19G	7-5-61	A2345-1Ø
A1A2J2A thru	7-5-61	A2345-1Ø
A1A2J2G	7-5-61	A2345-1Ø
A1A2J2ØA thru	7-5-61	A2345-1Ø
A1A2J2ØG	7-5-61	A2345-1Ø
A1A2J21A thru	7-5-61	A2345-1Ø
A1A2J21G	7-5-61	A2345-1Ø
A1A2J22A thru	7-5-61	A2345-1Ø
A1A2J22G	7-5-61	A2345-1Ø
A1A2J23A thru	7-5-61	A2345-1Ø
A1A2J23G	7-5-61	A2345-1Ø
A1A2J24A thru	7-5-61	A2345-1Ø
A1A2J24G	7-5-61	A2345-1Ø
A1A2J25A thru	7-5-61	A2345-1Ø
A1A2J25G	7-5-61	A2345-1Ø
A1A2J26A thru	7-5-61	A2345-1Ø
A1A2J26G	7-5-61	A2345-1Ø
A1A2J27A thru	7-5-61	A2345-1Ø
A1A2J27G	7-5-61	A2345-1Ø
A1A2J28A thru	7-5-61	A2345-1Ø
A1A2J28G	7-5-61	A2345-1Ø
A1A2J29A thru	7-5-61	A2345-1Ø
A1A2J29G	7-5-61	A2345-1Ø
A1A2J3A thru	7-5-61	A2345-1Ø
A1A2J3G	7-5-61	A2345-1Ø
A1A2J3ØA thru	7-5-61	A2345-1Ø
A1A2J3ØG	7-5-61	A2345-1Ø
A1A2J31A thru	7-5-61	A2345-1Ø
A1A2J31G	7-5-61	A2345-1Ø
A1A2J32A thru	7-5-61	A2345-1Ø
A1A2J32G	7-5-61	A2345-1Ø
A1A2J33A thru	7-5-61	A2345-1Ø
A1A2J33G	7-5-61	A2345-1Ø
A1A2J34A thru	7-5-61	A2345-1Ø
A1A2J34G	7-5-61	A2345-1Ø
A1A2J35A thru	7-5-61	A2345-1Ø
A1A2J35G	7-5-61	A2345-1Ø

REFERENCE DESIGNATOR INDEX

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A1A2J4A	7-5-61	A2345-1Ø
thru		
A1A2J4G	7-5-61	A2345-1Ø
A1A2J5A	7-5-61	A2345-1Ø
thru		
A1A2J5G	7-5-61	A2345-1Ø
A1A2J6A	7-5-61	A2345-1Ø
thru		
A1A2J6G	7-5-61	A2345-1Ø
A1A2J7A	7-5-61	A2345-1Ø
thru		
A1A2J7G	7-5-61	A2345-1Ø
A1A2J8A	7-5-61	A2345-1Ø
thru		
A1A2J8G	7-5-61	A2345-1Ø
A1A2J9A	7-5-61	A2345-1Ø
thru		
A1A2J9G	7-5-61	A2345-1Ø
A1A2P1	7-5-35	3614676
A1A2P2	7-5-35	3614676
A1A2S1	7-5-46	8869-K4
A1A2S2	7-5-46	8869-K4
A1A2TB1	7-5-43	3617351
A1A2TB2	7-5-44	No Number
A1A3	7-5-1Ø	ØN1168Ø6
A1A3S1	7-7-13	MBS-S-1838A-9
thru		
A1A3S1Ø	7-7-13	MBS-S-1838A-9
A1A3XDS1A	7-7	9Ø8-1166-1634-526
thru		
A1A3XDS1L	7-7	9Ø8-1166-1634-526
A1A3XDS1ØA	7-7	9Ø8-1166-1634-526
thru		
A1A3XDS1ØL	7-7	9Ø8-1166-1634-526
A1A3XDS11A	7-7	9Ø8-1166-1634-526
thru		
A1A3XDS11L	7-7	9Ø8-1166-1634-526
A1A3XDS12A	7-7	9Ø8-1166-1634-526
thru		
A1A3XDS12E	7-7	9Ø8-1166-1634-526
A1A3XDS12J	7-7	9Ø8-1166-1634-526
A1A3XDS12L	7-7	9Ø8-1166-1634-526
A1A3XDS13A	7-7	9Ø8-1166-1634-526
thru		
A1A3XDS13I	7-7	9Ø8-1166-1634-526
A1A3XDS14A	7-7	9Ø8-1166-1634-526
thru		
A1A3XDS14E	7-7	9Ø8-1166-1634-526
A1A3XDS14L	7-7	9Ø8-1166-1634-526
A1A3XDS15A	7-7	9Ø8-1166-1634-526
thru		
A1A3XDS15I	7-7	9Ø8-1166-1634-526
A1A3XDS16A	7-7	9Ø8-1166-1634-526
thru		
A1A3XDS16E	7-7	9Ø8-1166-1634-526
A1A3XDS16J	7-7	9Ø8-1166-1634-526
A1A3XDS16L	7-7	9Ø8-1166-1634-526
A1A3XDS17A	7-7	9Ø8-1166-1634-526
thru		
A1A3XDS17C	7-7	9Ø8-1166-1634-526
A1A3XDS17I	7-7	9Ø8-1166-1634-526
A1A3XDS2A	7-7	9Ø8-1166-1634-526
thru		
A1A3XDS2L	7-7	9Ø8-1166-1634-526
A1A3XDS3A	7-7	9Ø8-1166-1634-526
thru		
A1A3XDS3L	7-7	9Ø8-1166-1634-526
A1A3XDS4A	7-7	9Ø8-1166-1634-526
thru		
A1A3XDS4L	7-7	9Ø8-1166-1634-526
A1A3XDS5A	7-7	9Ø8-1166-1634-526
thru		
A1A3XDS5L	7-7	9Ø8-1166-1634-526
A1A3XDS6A	7-7	9Ø8-1166-1634-526
thru		
A1A3XDS6L	7-7	9Ø8-1166-1634-526
A1A3XDS7A	7-7	9Ø8-1166-1634-526
thru		
A1A3XDS7L	7-7	9Ø8-1166-1634-526
A1A3XDS8A	7-7	9Ø8-1166-1634-526
thru		
A1A3XDS8L	7-7	9Ø8-1166-1634-526
A1A3XDS9A	7-7	9Ø8-1166-1634-526
thru		
A1A3XDS9E	7-7	9Ø8-1166-1634-526
A1A3XDS9H	7-7	9Ø8-1166-1634-526
thru		
A1A3XDS9L	7-7	9Ø8-1166-1634-526
A1CR1	7-5-13	1N1186
A1CR2	7-5-13	1N1186
A1CR3	7-5-14	1N2804RB

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A1CR4	7-5-13	1N1186
A1CR5	7-5-13	1N1186
A1CR6	7-5-14	1N2804RB
A1XCR3	7-5-15	8038-1G13
A1XCR6	7-5-15	8038-1G13
A2	7-1-12	ØN116801-2
A2A1	7-5	ØN116803-1
A2A1A1A	7-15-16	ØNØ71777
thru		
A2A1A1G	7-15-16	ØNØ71777
A2A1A1ØA	7-15-9	ØNØ71761
A2A1A1ØB	7-15-3	ØNØ64Ø11
A2A1A1ØC	7-15-4	ØNØ64Ø08
A2A1A1ØD	7-15-3	ØNØ64Ø11
A2A1A1ØE	7-15-3	ØNØ64Ø11
A2A1A1ØF	7-15-3	ØNØ64Ø11
A2A1A1ØG	7-15-4	ØNØ64Ø08
A2A1A11A	7-15-8	ØNØ64Ø1Ø
A2A1A11B	7-15-3	ØNØ64Ø11
A2A1A11C	7-15-4	ØNØ64Ø08
A2A1A11D	7-15-9	ØNØ71761
A2A1A11E	7-15-8	ØNØ64Ø1Ø
A2A1A11F	7-15-7	ØNØ64Ø12
A2A1A11G	7-15-4	ØNØ64Ø08
A2A1A12A	7-15-7	ØNØ64Ø12
A2A1A12B	7-15-4	ØNØ64Ø08
A2A1A12C	7-15-4	ØNØ64Ø08
A2A1A12D	7-15-8	ØNØ64Ø1Ø
A2A1A12E	7-15-1Ø	ØNØ71762
A2A1A12F	7-15-3	ØNØ64Ø11
A2A1A12G	7-15-4	ØNØ64Ø08
A2A1A13A	7-15-1Ø	ØNØ71762
A2A1A13B	7-15-4	ØNØ64Ø08
A2A1A13C	7-15-4	ØNØ64Ø08
A2A1A13D	7-15-3	ØNØ64Ø11
A2A1A13E	7-15-8	ØNØ64Ø1Ø
A2A1A13F	7-15-9	ØNØ71761
A2A1A13G	7-15-4	ØNØ64Ø08
A2A1A14A	7-15-3	ØNØ64Ø11
A2A1A14B	7-15-4	ØNØ64Ø08
A2A1A14C	7-15-4	ØNØ64Ø08
A2A1A14D	7-15-3	ØNØ64Ø11
A2A1A14E	7-15-3	ØNØ64Ø11
A2A1A14F	7-15-4	ØNØ64Ø08
A2A1A14G	7-15-4	ØNØ64Ø18
A2A1A15A	7-15-8	ØNØ64Ø1Ø
A2A1A15B	7-15-4	ØNØ64Ø08
A2A1A15C	7-15-4	ØNØ64Ø08
A2A1A15D	7-15-7	ØNØ64Ø12
A2A1A15E	7-15-8	ØNØ64Ø1Ø
A2A1A15F	7-15-4	ØNØ64Ø08
A2A1A15G	7-15-8	ØNØ64Ø1Ø
A2A1A16A	7-15-1Ø	ØNØ71761
A2A1A16B	7-15-4	ØNØ64Ø08
A2A1A16C	7-15-4	ØNØ64Ø08
A2A1A16D	7-15-3	ØNØ64Ø11
A2A1A16E	7-15-3	ØNØ64Ø11
A2A1A16F	7-15-4	ØNØ64Ø08
A2A1A16G	7-15-4	ØNØ64Ø08
A2A1A17A	7-15-3	ØNØ64Ø11
A2A1A17B	7-15-3	ØNØ64Ø08
A2A1A17C	7-15-3	ØNØ64Ø11
A2A1A17D	7-15-3	ØNØ64Ø11
A2A1A17E	7-15-7	ØNØ64Ø12
A2A1A17F	7-15-4	ØNØ64Ø08
A2A1A17G	7-15-4	ØNØ64Ø08
A2A1A18A	7-15-3	ØNØ64Ø11
A2A1A18B	7-15-3	ØNØ64Ø11
A2A1A18D	7-15-3	ØNØ64Ø11
A2A1A18E	7-15-6	ØNØ64Ø23
A2A1A18F	7-15-3	ØNØ64Ø11
A2A1A18G	7-15-13	ØNØ71764
A2A1A19A	7-15-13	ØNØ71764
A2A1A19B	7-15-4	ØNØ64Ø08
A2A1A19C	7-15-4	ØNØ64Ø08
A2A1A19D	7-15-7	ØNØ64Ø12
A2A1A19E	7-15-4	ØNØ64Ø08
A2A1A19F	7-15-4	ØNØ64Ø08
A2A1A19G	7-15-4	ØNØ64Ø08
A2A1A2B	7-15-7	ØNØ64Ø12
A2A1A2C	7-15-8	ØNØ64Ø1Ø
A2A1A2D	7-15-8	ØNØ64Ø1Ø
A2A1A2E	7-15-8	ØNØ64Ø1Ø
A2A1A2F	7-15-17	ØNØ64Ø23
A2A1A2ØA	7-15-4	ØNØ64Ø04
A2A1A2ØB	7-15-4	ØNØ64Ø04
A2A1A2ØC	7-15-4	ØNØ64Ø04
A2A1A2ØD	7-15-7	ØNØ64Ø12
A2A1A2ØE	7-15-4	ØNØ64Ø08
A2A1A2ØF	7-15-6	ØNØ68Ø23
A2A1A2ØG	7-15-4	ØNØ64Ø12

REFERENCE DESIGNATOR INDEX

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A2A1A21A	7-15-7	ØNØ64Ø12
A2A1A21B	7-15-6	ØNØ68Ø23
A2A1A21C	7-15-6	ØNØ68Ø23
A2A1A21D	7-15-3	ØNØ64Ø11
A2A1A21E	7-15-4	ØNØ64Ø08
A2A1A21F	7-15-4	ØNØ64Ø08
A2A1A21G	7-15-4	ØNØ64Ø08
A2A1A22A	7-15-4	ØNØ64Ø08
A2A1A22B	7-15-4	ØNØ64Ø08
A2A1A22C	7-15-3	ØNØ64Ø11
A2A1A22D	7-15-3	ØNØ64Ø11
A2A1A22E	7-15-7	ØNØ64Ø12
A2A1A22F	7-15-4	ØNØ64Ø08
A2A1A22G	7-15-4	ØNØ64Ø08
A2A1A23A	7-15-4	ØNØ64Ø08
A2A1A23B	7-15-4	ØNØ64Ø08
A2A1A23C	7-15-9	ØNØ71761
A2A1A23D	7-15-3	ØNØ64Ø11
A2A1A23E	7-15-3	ØNØ64Ø11
A2A1A23F	7-15-6	ØNØ68Ø23
A2A1A23G	7-15-4	ØNØ64Ø08
A2A1A24A	7-15-1Ø	ØNØ71762
A2A1A24B	7-15-7	ØNØ64Ø12
A2A1A24C	7-15-6	ØNØ68Ø23
A2A1A24D	7-15-6	ØNØ64Ø23
A2A1A24E	7-15-6	ØNØ64Ø23
A2A1A24F	7-15-6	ØNØ64Ø23
A2A1A24G	7-15-3	ØNØ64Ø11
A2A1A25A	7-15-3	ØNØ64Ø11
A2A1A25B	7-15-3	ØNØ64Ø11
A2A1A25C	7-15-9	ØNØ71761
A2A1A25D	7-15-7	ØNØ64Ø12
A2A1A25E	7-15-7	ØNØ64Ø12
A2A1A25F	7-15-7	ØNØ64Ø12
A2A1A25G	7-15-9	ØNØ71761
A2A1A26A	7-15-3	ØNØ64Ø11
A2A1A26B	7-15-18	ØNØ71774
A2A1A26C	7-15-6	ØNØ64Ø23
A2A1A26D thru A2A1A26G	7-15-3	ØNØ64Ø11
A2A1A27A	7-15-8	ØNØ64Ø1Ø
A2A1A27B	7-15-18	ØNØ71774
A2A1A27C	7-15-6	ØNØ68Ø23
A2A1A27D thru A2A1A28A	7-15-3	ØNØ64Ø11
A2A1A28B	7-15-18	ØNØ71774
A2A1A28C	7-15-4	ØNØ64Ø08
A2A1A28D	7-15-3	ØNØ64Ø11
A2A1A28E	7-15-3	ØNØ64Ø11
A2A1A28F	7-15-3	ØNØ64Ø11
A2A1A28G	7-15-7	ØNØ64Ø12
A2A1A29A	7-15-4	ØNØ64Ø08
A2A1A29B	7-15-3	ØNØ64Ø11
A2A1A29C	7-15-3	ØNØ64Ø11
A2A1A29D	7-15-3	ØNØ64Ø11
A2A1A29E	7-15-6	ØNØ68Ø23
A2A1A29F	7-15-3	ØNØ64Ø11
A2A1A29G	7-15-3	ØNØ64Ø11
A2A1A3A	7-15-3	ØNØ64Ø11
A2A1A3B	7-15-3	ØNØ64Ø11
A2A1A3C	7-15-7	ØNØ64Ø12
A2A1A3D	7-15-3	ØNØ64Ø11
A2A1A3E	7-15-3	ØNØ64Ø11
A2A1A3F	7-15-3	ØNØ64Ø11
A2A1A3G	7-15-13	ØNØ71764
A2A1A3ØA	7-15-7	ØNØ64Ø12
A2A1A3ØB	7-15-8	ØNØ64Ø1Ø
A2A1A3ØC	7-15-8	ØNØ64Ø1Ø
A2A1A3ØD	7-15-6	ØNØ68Ø23
A2A1A3ØE	7-15-6	ØNØ68Ø23
A2A1A3ØF	7-15-6	ØNØ68Ø23
A2A1A3ØG	7-15-8	ØNØ64Ø1Ø
A2A1A31A	7-15-4	ØNØ64Ø08
A2A1A31B	7-15-4	ØNØ64Ø08
A2A1A31C	7-15-8	ØNØ64Ø1Ø
A2A1A31D	7-15-6	ØNØ68Ø23
A2A1A31E	7-15-6	ØNØ68Ø23
A2A1A31F	7-15-6	ØNØ68Ø23
A2A1A31G	7-15-3	ØNØ64Ø11
A2A1A32A	7-15-8	ØNØ64Ø1Ø
A2A1A32B	7-15-7	ØNØ64Ø12
A2A1A32C	7-15-7	ØNØ64Ø12
A2A1A32D	7-15-6	ØNØ68Ø23
A2A1A32E	7-15-4	ØNØ64Ø08
A2A1A32F	7-15-4	ØNØ64Ø08
A2A1A32G	7-15-3	ØNØ64Ø11
A2A1A33A	7-15-3	ØNØ64Ø11
A2A1A33B	7-15-3	ØNØ64Ø11
A2A1A33C	7-15-5	ØNØ64ØØØ
A2A1A33D	7-15-4	ØNØ64ØØ8
A2A1A33E	7-15-4	ØNØ64Ø08
A2A1A33F	7-15-4	ØNØ64Ø08
A2A1A33G	7-15-3	ØNØ64Ø11
A2A1A34B	7-15-2	ØNØ64Ø19
A2A1A34C	7-15-1	ØNØ64Ø13
A2A1A34D	7-15-9	ØNØ71761
A2A1A34E	7-15-4	ØNØ64Ø08
A2A1A34F	7-15-4	ØNØ64Ø08
A2A1A34G	7-15-7	ØNØ64Ø12
A2A1A35D	7-15-8	ØNØ64Ø1Ø
A2A1A35E	7-15-12	ØNØ64Ø09
A2A1A35F	7-15-8	ØNØ64Ø1Ø
A2A1A4A thru A2A1A4D	7-15-3	ØNØ64Ø11
A2A1A4E	7-15-9	ØNØ71761
A2A1A4F	7-15-4	ØNØ64Ø08
A2A1A4G	7-15-3	ØNØ64Ø11
A2A1A5A	7-15-3	ØNØ64Ø11
A2A1A5B	7-15-3	ØNØ64Ø11
A2A1A5C	7-15-3	ØNØ64Ø11
A2A1A5D	7-15-15	ØNØ64Ø15
A2A1A5E	7-15-7	ØNØ64Ø12
A2A1A5F	7-15-7	ØNØ64Ø12
A2A1A5G	7-15-9	ØNØ71761
A2A1A6A	7-15-7	ØNØ64Ø12
A2A1A6B	7-15-3	ØNØ64Ø11
A2A1A6C	7-15-1Ø	ØNØ71761
A2A1A6D	7-15-14	ØNØ64Ø24
A2A1A6E	7-15-13	ØNØ71764
A2A1A6F	7-15-3	ØNØ64Ø11
A2A1A6G	7-15-8	ØNØ64Ø1Ø
A2A1A7A	7-15-12	ØNØ64Ø09
A2A1A7B	7-15-7	ØNØ64Ø12
A2A1A7C	7-15-11	ØNØ64Ø16
A2A1A7D	7-15-4	ØNØ64Ø08
A2A1A7E	7-15-3	ØNØ64Ø11
A2A1A7G	7-15-7	ØNØ64Ø12
A2A1A8A thru A2A1A8E	7-15-3	ØNØ64Ø11
A2A1A8F	7-15-8	ØNØ64Ø1Ø
A2A1A8G	7-15-1Ø	ØNØ71762
A2A1A9A	7-15-8	ØNØ64Ø1Ø
A2A1A9B	7-15-7	ØNØ64Ø12
A2A1A9C	7-15-4	ØNØ64Ø08
A2A1A9D	7-15-8	ØNØ64Ø1Ø
A2A1A9E	7-15-3	ØNØ64Ø11
A2A1A9F	7-15-9	ØNØ71761
A2A1A9G	7-15-4	ØNØ64Ø08
A2A1C1 thru A2A1C42	7-5-34	5C11A9
A2A1J1A thru A2A1J1G	7-5-61	A2345-1Ø
A2A1J1ØA thru A2A1J1ØG	7-5-61	A2345-1Ø
A2A1J11A thru A2A1J11G	7-5-61	A2345-1Ø
A2A1J12A thru A2A1J12G	7-5-61	A2345-1Ø
A2A1J13A thru A2A1J13G	7-5-61	A2345-1Ø
A2A1J14A thru A2A1J14G	7-5-61	A2345-1Ø
A2A1J15A thru A2A1J15G	7-5-61	A2345-1Ø
A2A1J16A thru A2A1J16G	7-5-61	A2345-1Ø
A2A1J17A thru A2A1J17G	7-5-61	A2345-1Ø
A2A1J18A thru A2A1J18G	7-5-61	A2345-1Ø
A2A1J19A thru A2A1J19G	7-5-61	A2345-1Ø
A2A1J2A thru A2A1J2G	7-5-61	A2345-1Ø

REFERENCE DESIGNATOR INDEX

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A2A1J2ØA	7-5-61	A2345-1Ø
thru		
A2A1J2ØG	7-5-61	A2345-1Ø
A2A1J21A	7-5-61	A2345-1Ø
thru		
A2A1J21G	7-5-61	A2345-1Ø
A2A1J22A	7-5-61	A2345-1Ø
thru		
A2A1J22G	7-5-61	A2345-1Ø
A2A1J23A	7-5-61	A2345-1Ø
thru		
A2A1J23G	7-5-61	A2345-1Ø
A2A1J24A	7-5-61	A2345-1Ø
thru		
A2A1J24G	7-5-61	A2345-1Ø
A2A1J25A	7-5-61	A2345-1Ø
thru		
A2A1J25G	7-5-61	A2345-1Ø
A2A1J26A	7-5-61	A2345-1Ø
thru		
A2A1J26G	7-5-61	A2345-1Ø
A2A1J27A	7-5-61	A2345-1Ø
thru		
A2A1J27G	7-5-61	A2345-1Ø
A2A1J28A	7-5-61	A2345-1Ø
thru		
A2A1J28G	7-5-61	A2345-1Ø
A2A1J29A	7-5-61	A2345-1Ø
thru		
A2A1J29G	7-5-61	A2345-1Ø
A2A1J3A	7-5-61	A2345-1Ø
thru		
A2A1J3G	7-5-61	A2345-1Ø
A2A1J3ØA	7-5-61	A2345-1Ø
thru		
A2A1J3ØG	7-5-61	A2345-1Ø
A2A1J31A	7-5-61	A2345-1Ø
thru		
A2A1J31G	7-5-61	A2345-1Ø
A2A1J32A	7-5-61	A2345-1Ø
thru		
A2A1J32G	7-5-61	A2345-1Ø
A2A1J33A	7-5-61	A2345-1Ø
thru		
A2A1J33G	7-5-61	A2345-1Ø
A2A1J34A	7-5-61	A2345-1Ø
thru		
A2A1J34G	7-5-61	A2345-1Ø
A2A1J35A	7-5-61	A2345-1Ø
thru		
A2A1J35G	7-5-61	A2345-1Ø
A2A1J4A	7-5-61	A2345-1Ø
thru		
A2A1J4G	7-5-61	A2345-1Ø
A2A1J5A	7-5-61	A2345-1Ø
thru		
A2A1J5G	7-5-61	A2345-1Ø
A2A1J6A	7-5-61	A2345-1Ø
thru		
A2A1J6G	7-5-61	A2345-1Ø
A2A1J7A	7-5-61	A2345-1Ø
thru		
A2A1J7G	7-5-61	A2345-1Ø
A2A1J8A	7-5-61	A2345-1Ø
thru		
A2A1J8G	7-5-61	A2345-1Ø
A2A1J9A	7-5-61	A2345-1Ø
thru		
A2A1J9G	7-5-61	A2345-1Ø
A2A1P1	7-5-35	3614676
A2A1P2	7-5-35	3614676
A2A1TB1	7-5-43	3617351
A2A1TB2	7-5-44	No Number
A2A2	7-5	ØN116813-2
A2A2A1A	7-16-1	ØNØ71777
thru		
A2A2A1G	7-16-1	ØNØ71777
A2A2A1ØA	7-16-4	ØNØ64Ø26
thru		
A2A2A1ØG	7-16-4	ØNØ64Ø26
A2A2A11A	7-16-4	ØNØ64Ø26
thru		
A2A2A11G	7-16-4	ØNØ64Ø26
A2A2A12A	7-16-4	ØNØ64Ø26
thru		
A2A2A12G	7-16-4	ØNØ64Ø26
A2A2A13A	7-16-4	ØNØ64Ø26
thru		
A2A2A13E	7-16-4	ØNØ64Ø26
A2A2A13F	7-16-5	ØNØ64ØØ9
A2A2A13G	7-16-4	ØNØ64Ø26

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A2A2A14A	7-16-4	ØNØ64Ø26
thru		
A2A2A14G	7-16-4	ØNØ64Ø26
A2A2A15A	7-16-4	ØNØ64Ø26
thru		
A2A2A15G	7-16-4	ØNØ64Ø26
A2A2A16A	7-16-7	ØNØ64Ø12
A2A2A16B	7-16-7	ØNØ64Ø12
A2A2A16C	7-16-7	ØNØ64Ø12
A2A2A16D	7-16-6	ØNØ64Ø11
A2A2A16E	7-16-7	ØNØ64Ø12
A2A2A16F	7-16-3	ØNØ64ØØ9
A2A2A16G	7-16-3	ØNØ64ØØ9
A2A2A17A	7-16-8	ØNØ71764
thru		
A2A2A17F	7-16-8	ØNØ71764
A2A2A17G	7-16-9	ØNØ71761
A2A2A18A	7-16-1Ø	ØNØ71762
thru		
A2A2A18E	7-16-1Ø	ØNØ71762
A2A2A18F	7-16-7	ØNØ64Ø12
A2A2A18G	7-16-9	ØNØ71761
A2A2A19A	7-16-11	ØNØ64ØØ8
A2A2A19B	7-16-11	ØNØ64ØØ8
A2A2A19C	7-16-11	ØNØ64ØØ8
A2A2A19D	7-16-4	ØNØ64Ø26
A2A2A19E	7-16-11	ØNØ64ØØ8
A2A2A19F	7-16-11	ØNØ64ØØ8
A2A2A2A	7-16-12	ØNØ68Ø23
A2A2A2B	7-16-11	ØNØ64ØØ8
A2A2A2C	7-16-11	ØNØ64ØØ8
A2A2A2D	7-16-11	ØNØ64ØØ8
A2A2A2E	7-16-7	ØNØ64Ø12
A2A2A2F	7-16-6	ØNØ64Ø11
A2A2A2ØA	7-16-11	ØNØ64ØØ8
A2A2A2ØB	7-16-11	ØNØ64ØØ8
A2A2A2ØC	7-16-11	ØNØ64ØØ8
A2A2A2ØD	7-16-12	ØNØ68Ø23
A2A2A2ØE	7-16-11	ØNØ64ØØ8
A2A2A2ØF	7-16-11	ØNØ64ØØ8
A2A2A2ØG	7-16-6	ØNØ64Ø11
A2A2A21A	7-16-11	ØNØ64ØØ8
A2A2A21B	7-16-11	ØNØ64ØØ8
A2A2A21C	7-16-11	ØNØ64ØØ8
A2A2A21D	7-16-12	ØNØ68Ø23
A2A2A21E	7-16-11	ØNØ64ØØ8
A2A2A21F	7-16-11	ØNØ64ØØ8
A2A2A21G	7-16-11	ØNØ64ØØ8
A2A2A22A	7-16-11	ØNØ64ØØ8
A2A2A22B	7-16-11	ØNØ64ØØ8
A2A2A22C	7-16-11	ØNØ64ØØ8
A2A2A22D	7-16-12	ØNØ64Ø23
A2A2A22E	7-16-11	ØNØ64ØØ8
A2A2A22F	7-16-11	ØNØ64ØØ8
A2A2A22G	7-16-11	ØNØ64ØØ8
A2A2A23A	7-16-11	ØNØ64ØØ8
A2A2A23B	7-16-11	ØNØ64ØØ8
A2A2A23C	7-16-11	ØNØ64ØØ8
A2A2A23D	7-16-12	ØNØ64Ø23
A2A2A23E	7-16-11	ØNØ64ØØ8
A2A2A23F	7-16-11	ØNØ64ØØ8
A2A2A23G	7-16-11	ØNØ64ØØ8
A2A2A24A	7-16-11	ØNØ64ØØ8
A2A2A24B	7-16-11	ØNØ64ØØ8
A2A2A24C	7-16-11	ØNØ64ØØ8
A2A2A24D	7-16-12	ØNØ68Ø23
A2A2A24E	7-16-11	ØNØ64ØØ8
A2A2A24F	7-16-11	ØNØ64ØØ8
A2A2A24G	7-16-11	ØNØ64ØØ8
A2A2A25A	7-16-16	ØNØ64Ø33
A2A2A25B	7-16-14	ØNØ64Ø1Ø
A2A2A25C	7-16-7	ØNØ64Ø12
A2A2A25D	7-16-14	ØNØ64Ø1Ø
A2A2A25E	7-16-14	ØNØ64Ø1Ø
A2A2A25F	7-16-11	ØNØ64ØØ8
A2A2A25G	7-16-12	ØNØ68Ø23
A2A2A26A	7-16-11	ØNØ64ØØ8
A2A2A26B	7-16-7	ØNØ64Ø12
A2A2A26C	7-16-6	ØNØ64Ø11
A2A2A26D	7-16-12	ØNØ68Ø23
A2A2A26F	7-16-7	ØNØ64Ø12
A2A2A26G	7-16-6	ØNØ64Ø11
A2A2A27A	7-16-11	ØNØ64ØØ8
A2A2A27B	7-16-7	ØNØ64Ø12
A2A2A27C	7-16-9	ØNØ71761
A2A2A27D	7-16-14	ØNØ64Ø1Ø
A2A2A27E	7-16-11	ØNØ64ØØ8
A2A2A27F	7-16-9	ØNØ71761
A2A2A27G	7-16-6	ØNØ64Ø11
A2A2A28A	7-16-11	ØNØ64ØØ8
A2A2A28B	7-16-6	ØNØ64Ø11

REFERENCE DESIGNATOR INDEX

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A2A2A28C	7-16-6	ØNØ64Ø11
A2A2A28D	7-16-6	ØNØ64Ø11
A2A2A28E	7-16-7	ØNØ64Ø12
A2A2A28F	7-16-6	ØNØ64Ø11
A2A2A28G	7-16-7	ØNØ64Ø12
A2A2A29A	7-16-11	ØNØ64ØØ8
A2A2A29B	7-16-6	ØNØ64Ø11
A2A2A29C	7-16-9	ØNØ71761
A2A2A29D	7-16-6	ØNØ64Ø11
A2A2A29E	7-16-14	ØNØ64Ø1Ø
A2A2A29F	7-16-9	ØNØ71761
A2A2A29G	7-16-9	ØNØ71761
A2A2A3A	7-16-2	ØNØ68Ø31
thru		
A2A2A3G	7-16-2	ØNØ68Ø31
A2A2A3ØA	7-16-1Ø	ØNØ71762
A2A2A3ØB	7-16-6	ØNØ64Ø11
A2A2A3ØC	7-16-6	ØNØ64Ø11
A2A2A3ØD	7-16-12	ØNØ68Ø23
A2A2A3ØE	7-16-7	ØNØ64Ø12
A2A2A3ØF	7-16-11	ØNØ64ØØ8
A2A2A3ØG	7-16-7	ØNØ64Ø12
A2A2A31A	7-16-7	ØNØ64Ø12
A2A2A31B	7-16-9	ØNØ71761
A2A2A31C	7-16-6	ØNØ64Ø11
A2A2A31D	7-16-12	ØNØ68Ø23
A2A2A31E	7-16-7	ØNØ64Ø12
A2A2A31F	7-16-11	ØNØ64ØØ8
A2A2A31G	7-16-11	ØNØ64ØØ8
A2A2A32A	7-16-11	ØNØ64ØØ8
thru		
A2A2A32E	7-16-11	ØNØ64ØØ8
A2A2A32F	7-16-6	ØNØ64Ø11
A2A2A32G	7-16-11	ØNØ64ØØ8
A2A2A33A	7-16-11	ØNØ64ØØ8
thru		
A2A2A33G	7-16-11	ØNØ64ØØ8
A2A2A34A	7-16-5	ØNØ71774
A2A2A34B	7-16-5	ØNØ71774
A2A2A34C	7-16-11	ØNØ64ØØ8
thru		
A2A2A34F	7-16-11	ØNØ64ØØ8
A2A2A34G	7-16-7	ØNØ64Ø12
A2A2A35A	7-16-17	ØN116348
A2A2A35B	7-16-18	ØN116349
A2A2A35E	7-16-15	ØNØ68Ø21
A2A2A35F	7-16-1Ø	ØNØ71762
A2A2A35G	7-16-1Ø	ØNØ71762
A2A2A4A	7-16-2	ØNØ68Ø31
thru		
A2A2A4G	7-16-2	ØNØ68Ø31
A2A2A5A	7-16-2	ØNØ68Ø31
thru		
A2A2A5G	7-16-2	ØNØ68Ø31
A2A2A6A	7-16-2	ØNØ68Ø31
thru		
A2A2A6G	7-16-2	ØNØ68Ø31
A2A2A7A	7-16-2	ØNØ68Ø31
thru		
A2A2A7E	7-16-2	ØNØ68Ø31
A2A2A7F	7-16-3	ØNØ64ØØ9
A2A2A7G	7-16-3	ØNØ64ØØ9
A2A2A8A	7-16-4	ØNØ64Ø26
A2A2A8B	7-16-5	ØNØ71774
A2A2A8C	7-16-6	ØNØ64Ø11
A2A2A8D	7-16-5	ØNØ71774
A2A2A8E	7-16-6	ØNØ64Ø11
A2A2A8F	7-16-5	ØNØ71774
A2A2A9A	7-16-4	ØNØ64Ø26
thru		
A2A2A9G	7-16-4	ØNØ64Ø26
A2A2C1	7-5-34	5C11A
thru		
A2A2C42	7-5-34	5C11A
A2A2J1A	7-5-61	A2345-1Ø
thru		
A2A2J1G	7-5-61	A2345-1Ø
A2A2J1ØA	7-5-61	A2345-1Ø
thru		
A2A2J1ØG	7-5-61	A2345-1Ø
A2A2J11A	7-5-61	A2345-1Ø
thru		
A2A2J11G	7-5-61	A2345-1Ø
A2A2J12A	7-5-61	A2345-1Ø
thru		
A2A2J12G	7-5-61	A2345-1Ø
A2A2J13A	7-5-61	A2345-1Ø
thru		
A2A2J13G	7-5-61	A2345-1Ø
A2A2J14A	7-5-61	A2345-1Ø
thru		
A2A2J14G	7-5-61	A2345-1Ø

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A2A2J15A	7-5-61	A2345-1Ø
thru		
A2A2J15G	7-5-61	A2345-1Ø
A2A2J16A	7-5-61	A2345-1Ø
thru		
A2A2J16G	7-5-61	A2345-1Ø
A2A2J17A	7-5-61	A2345-1Ø
thru		
A2A2J17G	7-5-61	A2345-1Ø
A2A2J18A	7-5-61	A2345-1Ø
thru		
A2A2J18G	7-5-61	A2345-1Ø
A2A2J19A	7-5-61	A2345-1Ø
thru		
A2A2J19G	7-5-61	A2345-1Ø
A2A2J2A	7-5-61	A2345-1Ø
thru		
A2A2J2G	7-5-61	A2345-1Ø
A2A2J2ØA	7-5-61	A2345-1Ø
thru		
A2A2J2ØG	7-5-61	A2345-1Ø
A2A2J21A	7-5-61	A2345-1Ø
thru		
A2A2J21G	7-5-61	A2345-1Ø
A2A2J22A		
thru		
A2A2J22G	7-5-61	A2345-1Ø
A2A2J23A	7-5-61	A2345-1Ø
thru		
A2A2J23G	7-5-61	A2345-1Ø
A2A2J24A	7-5-61	A2345-1Ø
thru		
A2A2J24G	7-5-61	A2345-1Ø
A2A2J25A	7-5-61	A2345-1Ø
thru		
A2A2J25G	7-5-61	A2345-1Ø
A2A2J26A	7-5-61	A2345-1Ø
thru		
A2A2J26G	7-5-61	A2345-1Ø
A2A2J27A	7-5-61	A2345-1Ø
thru		
A2A2J27G	7-5-61	A2345-1Ø
A2A2J28A	7-5-61	A2345-1Ø
thru		
A2A2J28G	7-5-61	A2345-1Ø
A2A2J29A	7-5-61	A2345-1Ø
thru		
A2A2J29G	7-5-61	A2345-1Ø
A2A2J3A	7-5-61	A2345-1Ø
thru		
A2A2J3G	7-5-61	A2345-1Ø
A2A2J3ØA	7-5-61	A2345-1Ø
thru		
A2A2J3ØG	7-5-61	A2345-1Ø
A2A2J31A	7-5-61	A2345-1Ø
thru		
A2A2J31G	7-5-61	A2345-1Ø
A2A2J32A	7-5-61	A2345-1Ø
thru		
A2A2J32G	7-5-61	A2345-1Ø
A2A2J33A	7-5-61	A2345-1Ø
thru		
A2A2J33G	7-5-61	A2345-1Ø
A2A2J34A	7-5-61	A2345-1Ø
thru		
A2A2J34G	7-5-61	A2345-1Ø
A2A2J35A	7-5-61	A2345-1Ø
thru		
A2A2J35G	7-5-61	A2345-1Ø
A2A2J4A	7-5-61	A2345-1Ø
thru		
A2A2J4G	7-5-61	A2345-1Ø
A2A2J5A	7-5-61	A2345-1Ø
thru		
A2A2J5G	7-5-61	A2345-1Ø
A2A2J6A	7-5-61	A2345-1Ø
thru		
A2A2J6G	7-5-61	A2345-1Ø
A2A2J7A	7-5-61	A2345-1Ø
thru		
A2A2J7G	7-5-61	A2345-1Ø
A2A2J8A	7-5-61	A2345-1Ø
thru		
A2A2J8G	7-5-61	A2345-1Ø
A2A2J9A	7-5-61	A2345-1Ø
thru		
A2A2J9G	7-5-61	A2345-1Ø
A2A2P1	7-5-35	3614676
A2A2P2	7-5-35	3614676
A2A2S1	7-5-48	8869-K4
A2A2TB1	7-5-43	3617351
A2A2TB2	7-5-44	No Number

REFERENCE DESIGNATOR INDEX

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A2A3	7-5-1Ø	ØN11681Ø
A2A3R1	7-8-18	1NØ56S1Ø5UA
A2A3S1	7-8-11	MBS-5-1836A9
thru		
A2A3S8	7-8-11	MBS-5-1836A9
A2A3S9	7-8-19	13AT4Ø3-T2
thru		
A2A3S13	7-8-19	13AT4Ø3-T2
A2A3S14	7-8-2Ø	13AT4Ø1-T2
A2A3XDS1B	7-8	ØN123195-24
thru		
A2A3XDS1I	7-8	ØN123195-24
A2A3XDS1ØB	7-8	ØN123195-24
thru		
A2A3XDS1ØE	7-8	ØN123195-24
A2A3XDS11B	7-8	ØN123195-24
A2A3XDS12B	7-8	ØN123195-24
A2A3XDS12C	7-8	ØN123195-24
A2A3XDS12F	7-8	ØN123195-24
thru		
A2A3XDS121	7-8	ØN123195-24
A2A3XDS2C	7-8	ØN123195-24
thru		
A2A3XDS2F	7-8	ØN123195-24
A2A3XDS2H	7-8	ØN123195-24
A2A3XDS2I	7-8	ØN123195-24
A2A3XDS3B	7-8	ØN123195-24
A2A3XDS3C	7-8	ØN123195-24
A2A3XDS3E	7-8	ØN123195-24
A2A3XDS3G	7-8	ØN123195-24
A2A3XDS3H	7-8	ØN123195-24
A2A3XDS4C	7-8	ØN123195-24
thru		
A2A3XDS4F	7-8	ØN123195-24
A2A3XDS4H	7-8	ØN123195-24
A2A3XDS4I	7-8	ØN123195-24
A2A3XDS5B	7-8	ØN123195-24
A2A3XDS5C	7-8	ØN123195-24
A2A3XDS5E	7-8	ØN123195-24
A2A3XDS5G	7-8	ØN123195-24
A2A3XDS5H	7-8	ØN123195-24
A2A3XDS5I	7-8	ØN123195-24
A2A3XDS6B	7-8	ØN123195-24
thru		
A2A3XDS6D	7-8	ØN123195-24
A2A3XDS6F	7-8	ØN123195-24
A2A3XDS6G	7-8	ØN123195-24
A2A3XDS7B	7-8	ØN123195-24
thru		
A2A3XDS7D	7-8	ØN123195-24
A2A3XDS7F	7-8	ØN123195-24
A2A3XDS7G	7-8	ØN123195-24
A2A3XDS7I	7-8	ØN123195-24
A2A3XDS8C	7-8	ØN123195-24
thru		
A2A3XDS8E	7-8	ØN123195-24
A2A3XDS8H	7-8	ØN123195-24
A2A3XDS8I	7-8	ØN123195-24
A2A3XDS9A	7-8	ØN123195-24
thru		
A2A3XDS9I	7-8	ØN123195-24
A2CR1	7-5-13	1N1186
A2CR2	7-5-13	1N1186
A2CR3	7-5-14	1N28Ø4RB
A2CR4	7-5-13	1N1186
A2CR5	7-5-13	1N1186
A2CR6	7-5-14	1N28Ø4RB
A2XCR3	7-5-15	8Ø38-1G13
A2XCR6	7-5-15	8Ø38-1G13
A3	7-1-13	ØN1168Ø2-1
A3A1	7-6	ØNØ68178
A3A2	7-6	ØNØ68165-2
A3A2A1	7-6	ØNØ68166
A3A2A1A	7-17-1	ØN171777
thru		
A3A2A1G	7-17-1	ØN171777
A3A2A1J1A	7-6-47	A2345-1Ø
thru		
A3A2A1J1G	7-6-47	A2345-1Ø
A3A2A1J1ØA	7-6-47	A2345-1Ø
thru		
A3A2A1J1ØG	7-6-47	A2345-1Ø
A3A2A1J11A	7-6-47	A2345-1Ø
thru		
A3A2A1J11G	7-6-47	A2345-1Ø
A3A2A1J12A	7-6-47	A2345-1Ø
thru		
A3A2A1J12G	7-6-47	A2345-1Ø
A3A2A1J13A	7-6-47	A2345-1Ø
thru		
A3A2A1J13G	7-6-47	A2345-1Ø

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A3A2A1J14A	7-6-47	A2345-1Ø
thru		
A3A2A1J14G	7-6-47	A2345-1Ø
A3A2A1J15A	7-6-47	A2345-1Ø
thru		
A3A2A1J15G	7-6-47	A2345-1Ø
A3A2A1J16A	7-6-47	A2345-1Ø
thru		
A3A2A1J16G	7-6-47	A2345-1Ø
A3A2A1J17A	7-6-47	A2345-1Ø
thru		
A3A2A1J17G	7-6-47	A2345-1Ø
A3A2A1J18A	7-6-47	A2345-1Ø
thru		
A3A2A1J18G	7-6-47	A2345-1Ø
A3A2A1J19A	7-6-47	A2345-1Ø
thru		
A3A2A1J19G	7-6-47	A2345-1Ø
A3A2A1J2A	7-6-47	A2345-1Ø
thru		
A3A2A1J2G	7-6-47	A2345-1Ø
A3A2A1J2ØA	7-6-47	A2345-1Ø
thru		
A3A2A1J2ØG	7-6-47	A2345-1Ø
A3A2A1J21A	7-6-47	A2345-1Ø
thru		
A3A2A1J21G	7-6-47	A2345-1Ø
A3A2A1J22A	7-6-47	A2345-1Ø
thru		
A3A2A1J22G	7-6-47	A2345-1Ø
A3A2A1J3A	7-6-47	A2345-1Ø
thru		
A3A2A1J3G	7-6-47	A2345-1Ø
A3A2A1J4A	7-6-47	A2345-1Ø
thru		
A3A2A1J4G	7-6-47	A2345-1Ø
A3A2A1J5A	7-6-47	A2345-1Ø
thru		
A3A2A1J5G	7-6-47	A2345-1Ø
A3A2A1J6A	7-6-47	A2345-1Ø
thru		
A3A2A1J6G	7-6-47	A2345-1Ø
A3A2A1J7A	7-6-47	A2345-1Ø
thru		
A3A2A1J7G	7-6-47	A2345-1Ø
A3A2A1J8A	7-6-47	A2345-1Ø
thru		
A3A2A1J8G	7-6-47	A2345-1Ø
A3A2A1J9A	7-6-47	A2345-1Ø
thru		
A3A2A1J9G	7-6-47	A2345-1Ø
A3A2A1ØC	7-17-8	ØNØ64Ø22
A3A2A1ØD	7-17-7	ØNØ68Ø33
A3A2A1ØE	7-17-7	ØNØ68Ø33
A3A2A1ØF	7-17-7	ØNØ68Ø33
A3A2A11C	7-17-8	ØNØ64Ø22
thru		
A3A2A11F	7-17-8	ØNØ64Ø22
A3A2A12A	7-17-9	ØNØ68ØØ2
A3A2A12C	7-17-7	ØNØ68Ø33
A3A2A12D	7-17-7	ØNØ68Ø33
A3A2A12E	7-17-7	ØNØ68Ø33
A3A2A12F	7-17-8	ØNØ64Ø22
A3A2A13A	7-17-1Ø	ØNØ68ØØ6
A3A2A13B	7-17-11	ØNØ68Ø23
A3A2A13C	7-17-8	ØNØ64Ø22
thru		
A3A2A13F	7-17-8	ØNØ64Ø22
A3A2A14A	7-17-12	ØNØ68Ø07
A3A2A14B	7-17-13	ØNØ64Ø23
A3A2A14C	7-17-8	ØNØ64Ø22
A3A2A14D	7-17-7	ØNØ68Ø33
A3A2A14E	7-17-7	ØNØ68Ø33
A3A2A14F	7-17-7	ØNØ68Ø33
A3A2A14G	7-17-13	ØNØ64Ø23
A3A2A15A	7-17-14	ØNØ68Ø29
A3A2A15B	7-17-13	ØNØ64Ø23
A3A2A15C	7-17-8	ØNØ64Ø22
thru		
A3A2A15F	7-17-8	ØNØ64Ø22
A3A2A15G	7-17-13	ØNØ64Ø23
A3A2A16A	7-17-6	ØNØ64Ø12
A3A2A16B	7-17-15	ØNØ64Ø19
A3A2A16C	7-17-7	ØNØ68Ø33
A3A2A16D	7-17-7	ØNØ68Ø33
A3A2A16E	7-17-7	ØNØ68Ø33
A3A2A16F	7-17-8	ØNØ64Ø22
A3A2A16G	7-17-6	ØNØ64Ø12
A3A2A17A	7-17-6	ØNØ64Ø12
A3A2A17B	7-17-15	ØNØ64Ø19
A3A2A17C	7-17-8	ØNØ64Ø22

REFERENCE DESIGNATOR INDEX

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A3A2A17D	7-17-8	ØNØ64Ø22
A3A2A17E	7-17-8	ØNØ64Ø22
A3A2A17F	7-17-15	ØNØ64Ø19
A3A2A17G	7-17-6	ØNØ64Ø12
A3A2A18A	7-17-6	ØNØ64Ø12
A3A2A18B	7-17-15	ØNØ64Ø19
thru		
A3A2A18F	7-17-15	ØNØ64Ø19
A3A2A18G	7-17-6	ØNØ64Ø12
A3A2A19A	7-17-16	ØNØ68Ø3
A3A2A19B	7-17-15	ØNØ64Ø19
A3A2A19C	7-17-15	ØNØ64Ø19
A3A2A19D	7-17-17	ØNØ64Ø18
A3A2A19E	7-17-15	ØNØ64Ø19
A3A2A19F	7-17-15	ØNØ64Ø19
A3A2A2	7-6-23	ØNØ68148
A3A2A2A	7-17-2	ØNØ68ØØ1
A3A2A2B	7-17-2	ØNØ68ØØ1
A3A2A2C	7-17-3	ØNØ71761
A3A2A2C1	7-1Ø-6	CL25BH221UP3
thru		
A3A2A2C4	7-1Ø-6	CL25BH221UP3
A3A2A2E	7-17-4	ØNØ68ØØ8
A3A2A2F	7-17-2	ØNØ68ØØ1
A3A2A2G	7-17-2	ØNØ68ØØ1
A3A2A2R1	7-1Ø-1	RE651ØRØ
A3A2A2R2	7-1Ø-1	RE651ØRØ
A3A2A2R4	7-1Ø-4	RC42GF15ØJ
thru		
A3A2A2R17	7-1Ø-4	RC42GF15ØJ
A3A2A2R18	7-1Ø-2	RE6515RØ
thru		
A3A2A2R27	7-1Ø-2	RE6515RØ
A3A2A2R28	7-1Ø-3	RE6542R2
A3A2A2R29	7-1Ø-3	RE6542R2
A3A2A2R3Ø	7-1Ø-2	RE6515RØ
thru		
A3A2A2R32	7-1Ø-2	RE6515RØ
A3A2A2R37	7-1Ø-1	RE651ØRØ
A3A2A2R38	7-1Ø-1	RE651ØRØ
A3A2A2R39	7-1Ø-5	RC32GF6R8J
thru		
A3A2A2R42	7-1Ø-5	RC32GF6R8J
A3A2A2ØA	7-17-16	ØNØ68Ø3
A3A2A2ØB	7-17-15	ØNØ64Ø19
A3A2A2ØC	7-17-17	ØNØ64Ø18
A3A2A2ØD	7-17-17	ØNØ64Ø18
A3A2A2ØE	7-17-17	ØNØ64Ø18
A3A2A2ØF	7-17-15	ØNØ64Ø19
A3A2A2ØG	7-17-16	ØNØ68Ø3
A3A2A21A	7-17-7	ØNØ68Ø33
A3A2A21B	7-17-15	ØNØ64Ø19
A3A2A21C	7-17-17	ØNØ64Ø18
A3A2A21D	7-17-17	ØNØ64Ø18
A3A2A21E	7-17-17	ØNØ64Ø18
A3A2A21F	7-17-15	ØNØ64Ø19
A3A2A21G	7-17-7	ØNØ68Ø33
A3A2A22A	7-17-7	ØNØ68Ø33
A3A2A22B	7-17-18	ØNØ64Ø21
A3A2A22C	7-17-18	ØNØ64Ø21
A3A2A22D	7-17-17	ØNØ64Ø18
A3A2A22E	7-17-18	ØNØ64Ø21
A3A2A22F	7-17-18	ØNØ64Ø21
A3A2A22G	7-17-7	ØNØ68Ø33
A3A2A3A	7-17-2	ØNØ68ØØ1
A3A2A3B	7-17-2	ØNØ68ØØ1
A3A2A3C	7-17-3	ØNØ71761
A3A2A2E	7-17-4	ØNØ68ØØ8
A3A2A3F	7-17-2	ØNØ68ØØ1
A3A2A3G	7-17-2	ØNØ68ØØ1
A3A2A4A	7-17-2	ØNØ68ØØ1
A3A2A4B	7-17-2	ØNØ68ØØ1
A3A2A4C	7-17-3	ØNØ71761
A3A2A4E	7-17-4	ØNØ68ØØ8
A3A2A4F	7-17-2	ØNØ68ØØ1
A3A2A4G	7-17-2	ØNØ68ØØ1
A3A2A5A	7-17-2	ØNØ68ØØ1
A3A2A5B	7-17-2	ØNØ68ØØ1
A3A2A5C	7-17-3	ØNØ71761
A3A2A5E	7-17-4	ØNØ68ØØ8
A3A2A5F	7-17-2	ØNØ68ØØ1
A3A2A5G	7-17-2	ØNØ68ØØ1
A3A2A6A	7-17-2	ØNØ68ØØ1
A3A2A6B	7-17-2	ØNØ68ØØ1
A3A2A6C	7-17-3	ØNØ71761
A3A2A6E	7-17-4	ØNØ68ØØ8
A3A2A6F	7-17-2	ØNØ68ØØ1
A3A2A6G	7-17-2	ØNØ68ØØ1
A3A2A7A	7-17-2	ØNØ68ØØ1
A3A2A7B	7-17-2	ØNØ68ØØ1
A3A2A7C	7-17-3	ØNØ71761
A3A2A7F	7-17-2	ØNØ68ØØ1

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A3A2A7G	7-17-2	ØNØ68ØØ1
A3A2A8A	7-17-2	ØNØ68ØØ1
A3A2A8C	7-17-3	ØNØ71761
A3A2A8D	7-17-6	ØNØ64Ø12
A3A2A8F	7-17-2	ØNØ68ØØ1
A3A2A9D	7-17-6	ØNØ64Ø12
A3A2A9E	7-17-8	ØNØ64Ø22
A3A2CR1	7-6-31	1N2804RB
A3A2CR2	7-6-26	1N1186
A3A2CR3	7-6-26	1N1186
A3A2C1	7-6-24	5C11A9
thru		
A3A2C42	7-6-24	5C11A9
A3A2P1	7-6-33	361468Ø
A3A2P2	7-6-33	361468Ø
A3A2Q1	7-6-3Ø	SP4166
A3A2Q2	7-6-29	SP4167
A3A2XCR1	7-6-32	8Ø38-1G13
A3A2Ø	7-6-1	ØNØ68229
A3A21	7-6-1	ØNØ68229
A3A22	7-6-1	ØNØ68229
A3A23	7-6-1	ØNØ68229
A3A4	7-6-1Ø	ØNØ66174
A3A4B1	7-9-3	AØ-185668
A3A4J2Ø1	7-9-1	DDM-5ØS
thru		
A3A4J2Ø3	7-9-1	DDM-5ØS
A3A4J211	7-9-1	DDM-5ØS
thru		
A3A4J213	7-9-1	DDM-5ØS
A3A4J221	7-9-1	DDM-5ØS
thru		
A3A4J223	7-9-1	DDM-5ØS
A3A4J231	7-9-1	DDM-5ØS
thru		
A3A4J233	7-9-1	DDM-5ØS
A3A4R2Ø	7-9-8	224S-1-15Ø(M)
thru		
A3A4R23	7-9-8	224S-1-15Ø(M)
A3A4R24	7-9-7	224S-1-1Ø2(M)
A3A4S2	7-9-9	8869-K4
A4	7-1-14	ØN116Ø2-2
A4A1	7-6	ØNØ68178
A4A2	7-6	ØNØ68165-2
A4A2A1A	7-17-1	ØNØ71777
thru		
A4A2A1G	7-17-1	ØNØ71777
A4A2A1J1A	7-6-47	A2345-1Ø
thru		
A4A2A1J1G	7-6-47	A2345-1Ø
A4A2A1J1ØA	7-6-47	A2345-1Ø
thru		
A4A2A1J1ØG	7-6-47	A2345-1Ø
A4A2A1J11A	7-6-47	A2345-1Ø
thru		
A4A2A1J11G	7-6-47	A2345-1Ø
A4A2A1J12A	7-6-47	A2345-1Ø
thru		
A4A2A1J12G	7-6-47	A2345-1Ø
A4A2A1J13A	7-6-47	A2345-1Ø
thru		
A4A2A1J13G	7-6-47	A2345-1Ø
A4A2A1J14A	7-6-47	A2345-1Ø
thru		
A4A2A1J14G	7-6-47	A2345-1Ø
A4A2A1J15A	7-6-47	A2345-1Ø
thru		
A4A2A1J15G	7-6-47	A2345-1Ø
A4A2A1J16A	7-6-47	A2345-1Ø
thru		
A4A2A1J16G	7-6-47	A2345-1Ø
A4A2A1J17A	7-6-47	A2345-1Ø
thru		
A4A2A1J17G	7-6-47	A2345-1Ø
A4A2A1J18A	7-6-47	A2345-1Ø
thru		
A4A2A1J18G	7-6-47	A2345-1Ø
A4A2A1J19A	7-6-47	A2345-1Ø
thru		
A4A2A1J19G	7-6-47	A2345-1Ø
A4A2A1J2A	7-6-47	A2345-1Ø
thru		
A4A2A1J2G	7-6-47	A2345-1Ø
A4A2A1J2ØA	7-6-47	A2345-1Ø
thru		
A4A2A1J2ØG	7-6-47	A2345-1Ø
A4A2A1J21A	7-6-47	A2345-1Ø
thru		
A4A2A1J21G	7-6-47	A2345-1Ø
A4A2A1J22A	7-6-47	A2345-1Ø
thru		
A4A2A1J22G	7-6-47	A2345-1Ø

REFERENCE DESIGNATOR INDEX

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A4A2A1J3A	7-6-47	A2345-1Ø
thru		
A4A2A1J4A	7-6-47	A2345-1Ø
thru		
A4A2A1J4G	7-6-47	A2345-1Ø
A4A2A1J5A	7-6-47	A2345-1Ø
thru		
A4A2A1J5G	7-6-47	A2345-1Ø
A4A2A1J6A	7-6-47	A2345-1Ø
thru		
A4A2A1J6G	7-6-47	A2345-1Ø
A4A2A1J7A	7-6-47	A2345-1Ø
thru		
A4A2A1J7G	7-6-47	A2345-1Ø
A4A2A1J8A	7-6-47	A2345-1Ø
thru		A2345-1Ø
A4A2A1J8G	7-6-47	A2345-1Ø
A4A2A1J9A	7-6-47	A2345-1Ø
thru		
A4A2A1J9G	7-6-47	A2345-1Ø
A4A2A1ØC	7-17-8	ØNØ64Ø22
A4A2A1ØD	7-17-7	ØNØ68Ø33
A4A2A1ØE	7-17-7	ØNØ68Ø33
A4A2A1ØF	7-17-7	ØNØ68Ø03
A4A2A11C	7-17-8	ØNØ64Ø02
thru		
A4A2A11F	7-17-8	ØNØ64Ø22
A4A2A12A	7-17-9	ØNØ68Ø02
A4A2A12C	7-17-7	ØNØ68Ø33
A4A2A12D	7-17-7	ØNØ68Ø33
A4A2A12E	7-17-7	ØNØ68Ø33
A4A2A12F	7-17-8	ØNØ64Ø02
A4A2A13A	7-17-1Ø	ØNØ68Ø06
A4A2A13B	7-17-11	ØNØ68Ø23
A4A2A13C	7-17-8	ØNØ64Ø22
thru		
A4A2A13F	7-17-8	ØNØ64Ø22
A4A2A14A	7-17-12	ØNØ68Ø07
A4A2A14B	7-17-13	ØNØ64Ø23
A4A2A14C	7-17-8	ØNØ64Ø02
A4A2A14D	7-17-7	ØNØ68Ø33
A4A2A14E	7-17-7	ØNØ68Ø33
A4A2A14F	7-17-7	ØNØ68Ø33
A4A2A14G	7-17-13	ØNØ64Ø23
A4A2A15A	7-17-14	ØNØ64Ø29
A4A2A15B	7-17-13	ØNØ64Ø23
A4A2A15C	7-17-8	ØNØ64Ø22
thru		
A4A2A15F	7-17-8	ØNØ64Ø22
A4A2A15G	7-17-13	ØNØ64Ø23
A4A2A16A	7-17-6	ØNØ64Ø12
A4A2A16B	7-17-15	ØNØ64Ø19
A4A2A16C	7-17-7	ØNØ68Ø33
A4A2A16D	7-17-7	ØNØ68Ø33
A4A2A16E	7-17-7	ØNØ68Ø33
A4A2A16F	7-17-8	ØNØ64Ø22
A4A2A16G	7-17-6	ØNØ64Ø12
A4A2A17A	7-17-6	ØNØ64Ø12
A4A2A17B	7-17-15	ØNØ64Ø19
A4A2A17C	7-17-8	ØNØ64Ø22
A4A2A17D	7-17-6	ØNØ64Ø22
A4A2A17E	7-17-8	ØNØ64Ø22
A4A2A17F	7-17-15	ØNØ64Ø19
A4A2A17G	7-17-6	ØNØ64Ø12
A4A2A18A	7-17-6	ØNØ64Ø12
A4A2A18B	7-17-15	ØNØ64Ø19
thru		
A4A2A18F	7-17-15	ØNØ64Ø19
A4A2A18G	7-17-6	ØNØ64Ø12
A4A2A19A	7-17-16	ØNØ68Ø03
A4A2A19B	7-17-15	ØNØ64Ø19
A4A2A19C	7-17-15	ØNØ64Ø19
A4A2A19D	7-17-17	ØNØ64Ø18
A4A2A19E	7-17-15	ØNØ64Ø19
A4A2A19F	7-17-15	ØNØ64Ø19
A4A2A2	7-6-23	ØNØ68148
A4A2A2A	7-17-2	ØNØ68Ø01
A4A2A2B	7-17-2	ØNØ68Ø01
A4A2A2C	7-17-3	ØNØ71761
A4A2A2C1	7-1Ø-6	CL25BH221UP3
thru		
A4A2A2C4	7-1Ø-6	CL25BH221UP3
A4A2A2E	7-17-4	ØNØ68ØØ8
A4A2A2F	7-17-2	ØNØ68Ø01
A4A2A2G	7-17-2	ØNØ68Ø01
A4A2A2R1	7-1Ø-1	RE6510RØ
A4A2A2R2	7-1Ø-1	RE6510RØ
A4A2A2R4	7-1Ø-4	RC42GF15ØJ
thru		
A4A2A2R17	7-1Ø-4	RC42GF15ØJ
A4A2A2R18	7-1Ø-2	RE6515RØ
thru		
A4A2A2R27	7-1Ø-2	RE6515RØ

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
A4A2A2R28	7-1Ø-3	RE6542R2
A4A2A2R29	7-1Ø-3	RE6542R2
A4A2A2R3Ø	7-1Ø-2	RE6515RØ
thru		
A4A2A2R32	7-1Ø-2	RE6515RØ
A4A2A2R37	7-1Ø-1	RE6510RØ
A4A2A2R38	7-1Ø-1	RE6510RØ
A4A2A2R39	7-1Ø-5	RC32GF6R8J
thru		
A4A2A2R42	7-1Ø-5	RC32GF6R8J
A4A2A2ØA	7-17-16	ØNØ68Ø03
A4A2A2ØB	7-17-15	ØNØ64Ø19
A4A2A2ØC	7-17-17	ØNØ64Ø18
A4A2A2ØD	7-17-17	ØNØ64Ø18
A4A2A2ØE	7-17-17	ØNØ64Ø18
A4A2A2ØF	7-17-15	ØNØ64Ø19
A4A2A2ØG	7-17-16	ØNØ68Ø03
A4A2A21A	7-17-7	ØNØ68Ø33
A4A2A21B	7-17-15	ØNØ64Ø19
A4A2A21C	7-15-17	ØNØ64Ø18
A4A2A21D	7-17-17	ØNØ64Ø18
A4A2A21E	7-17-17	ØNØ64Ø18
A4A2A21F	7-17-15	ØNØ64Ø19
A4A2A21G	7-17-7	ØNØ68Ø33
A4A2A22A	7-17-7	ØNØ68Ø33
A4A2A22B	7-17-18	ØNØ64Ø21
A4A2A22C	7-17-18	ØNØ64Ø21
A4A2A22D	7-17-17	ØNØ64Ø18
A4A2A22E	7-17-18	ØNØ64Ø21
A4A2A22F	7-17-18	ØNØ64Ø21
A4A2A22G	7-17-7	ØNØ68Ø33
A4A2A3A	7-17-2	ØNØ68Ø01
A4A2A3B	7-17-2	ØNØ68Ø01
A4A2A3C	7-17-3	ØNØ71761
A4A2A3E	7-17-4	ØNØ68ØØ8
A4A2A3F	7-15-2	ØNØ68Ø01
A4A2A3G	7-17-2	ØNØ68Ø01
A4A2A4A	7-17-2	ØNØ68Ø01
A4A2A4B	7-17-2	ØNØ68Ø01
A4A2A4C	7-17-3	ØNØ71761
A4A2A4E	7-17-4	ØNØ68ØØ8
A4A2A4F	7-17-2	ØNØ68Ø01
A4A2A4G	7-17-2	ØNØ68Ø01
A4A2A5A	7-17-2	ØNØ68Ø01
A4A2A5B	7-17-2	ØNØ68Ø01
A4A2A5C	7-17-3	ØNØ71761
A4A2A5E	7-17-4	ØNØ68ØØ8
A4A2A5F	7-17-2	ØNØ68Ø01
A4A2A5G	7-17-2	ØNØ68Ø01
A4A2A6A	7-17-2	ØNØ68Ø01
A4A2A6B	7-17-2	ØNØ68Ø01
A4A2A6C	7-17-3	ØNØ71761
A4A2A6E	7-17-4	ØNØ68ØØ8
A4A2A6F	7-17-2	ØNØ68Ø01
A4A2A6G	7-17-2	ØNØ68Ø01
A4A2A7A	7-17-2	ØNØ68Ø01
A4A2A7B	7-17-2	ØNØ68Ø01
A4A2A7C	7-17-3	ØNØ71761
A4A2A7F	7-17-2	ØNØ68Ø01
A4A2A7G	7-17-2	ØNØ68Ø01
A4A2A8A	7-17-2	ØNØ68Ø01
A4A2A8C	7-17-3	ØNØ71761
A4A2A8D	7-17-6	ØNØ64Ø12
A4A2A8F	7-17-2	ØNØ68Ø01
A4A2A9D	7-17-7	ØNØ68Ø33
A4A2A9E	7-17-8	ØNØ64Ø22
A4A2CR1	7-6-31	1N28Ø4RB
A4A2CR2	7-6-26	1N1186
A4A2CR3	7-6-26	1N1186
A4A2C1	7-6-24	5C11A9
thru		
A4A2C42	7-6-24	5C11A9
A4A2P1	7-6-33	361468Ø
A4A2P2	7-6-33	361468Ø
A4A2Q1	7-6-3Ø	SP4166
A4A2Q2	7-6-29	SP4167
A4A2XCR1	7-6-32	8Ø38-1G13
A4A2Ø	7-6-1	ØNØ68229
A4A21	7-6-1	ØNØ68229
A4A22	7-6-1	ØNØ68229
A4A23	7-6-1	ØNØ68229
A4A4	7-6-1Ø	ØNØ68174
A4A4B1	7-9-3	AØ-185668
A4A4J2Ø1	7-9-1	DDM-5ØS
thru		
A4A4J2Ø3	7-9-1	DDM-5ØS
A4A4J211	7-9-1	DDM-5ØS
thru		
A4A4J213	7-9-1	DDM-5ØS
A4A4J221	7-9-1	DDM-5ØS
thru	7-9-1	
A4A4J223	7-9-1	DDM-5ØS
A4A4J231	7-9-1	DDM-5ØS

REFERENCE DESIGNATOR INDEX

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
thru		
A4A4J233	7-9-1	DDM-5ØS
A4A4R2Ø	7-9-8	224S-1-15ØM
thru		
A4A4R23	7-9-8	224S-1-15ØM
A4A4R24	7-9-7	224S-1-1Ø2(M)
A4A4S2	7-9-9	8869-K4
A5	7-1-9	ØN116816
A5A1	7-4	ØNØ68147
A5A1R1	7-4-1Ø	RC32GF1ØØJ
A5A1R2	7-4-11	RC32GF681J
A5A1R3	7-4-11	RC32GF681J
A5A1R4	7-4-1Ø	RC32GF1ØØJ
A5A1R5	7-4-1Ø	RC32GF1ØØJ
A5A1R6	7-4-11	RC32GF681J
A5A1R7	7-4-11	RC32GF681J
A5A1R8	7-4-1Ø	RC32GF1ØØJ
A5A1R9	7-4-1Ø	RC32GF1ØØJ
A5A1R1Ø	7-4-11	RC32GF681J
A5A2	7-4	ØN116846
A5A2CR1	7-4-5	1N4Ø86
A5A2K1	7-4-1	FS31Ø4
A5A2K2	7-4-3	RF-6Ø-NC-115-6Ø
A5A2K3	7-4-6	RY4XX2B3L32
A5A2XK1	7-4-4	TS1Ø3PØ3
A5C1	7-4-8	CPØ9A1KC1Ø4K3
A5C2	7-4-8	CPØ9A1KC1Ø4K3
A5C3	7-4-15	CZ24BKF1Ø3
thru		
A5C11	7-4-15	CZ24BKF1Ø3
A5C13	7-4-15	CZ24BKF1Ø3
thru		
A5C19	7-4-15	CZ24BKF1Ø3
A5DS1	7-4-25	1826
thru		
A5DS6	7-4-25	1826
A5E1	7-4-16	SCREW
A5LS1	7-2-1	SC-628
A5M1	7-4-27	MS17325-1
A5S1	7-4-28	13AT4Ø3-T2
A5S2	7-4-29	MS35Ø59-21
A5S4	7-4-26	13AT4Ø1-T2
A5S5	7-4-26	13AT4Ø1-T2
A5TB1	7-4-14	26TB8
A5TB2	7-4-13	26TB12
A5XDS1	7-4-24	81-Ø11Ø-Ø112-2Ø3
A5XDS2	7-4-23	81-Ø41Ø-Ø111-2Ø3
thru		
A5XDS5	7-4-23	81-Ø41Ø-Ø111-2Ø3
A5SDS6	7-4-24	81-Ø41Ø-Ø112-2Ø3
A6	7-1-17	ØN116843
A6B1	7-12-3	654DS
A6B2	7-12-3	654DS
A6C1	7-12-4	CH53BIMF1Ø5K
A6C2	7-12-4	CH53BIMF1Ø5K
A6TB1	7-12-2	26TB12
A7	7-1-17	ØN116843
A7B1	7-12-3	654DS
A7B2	7-12-3	654DS
A7C1	7-12-4	CH53BIMF1Ø5K
A7C2	7-12-4	CH53BIMF1Ø5K
A7TB1	7-12-2	26TB12
A12	7-2	ØNØ68228-2
A12A1	7-2	ØNØ67Ø59-2
A12A1F1	7-2-13	FØ3A25ØV8AS
A12A1F2	7-2-14	FØ3A25ØV1ØAS
A12A1F3	7-2-15	FØ2A25ØV3AS
A12A1F4	7-2-13	FØ3A25ØV8AS
A12A1F5	7-2-14	FØ3A25ØV1ØAS
A12A1F6	7-2-15	FØ2A25ØV3AS
A12A1J1	7-2-24	3614875
thru		
A12A1J4	7-2-24	3614875
A12A1XF1	7-2-17	HKU
A12A1XF2	7-2-16	FHL18G2-1
A12A1XF3	7-2-16	FHL18G2-1
A12A1XF4	7-2-17	HKU
A12A1XF5	7-2-16	FHL18G2-1
A12A1XF6	7-2-16	FHL18G2-1
A12A2	7-2	ØNØ67Ø59-2
A12A2F1	7-2-13	FØ3A25ØV8AS
A12A2F2	7-2-14	FØ3A25ØV1ØAS
A12A2F3	7-2-15	FØ2A25ØV3AS
A12A2F4	7-2-13	FØ3A25ØV8AS
A12A2F5	7-2-14	FØ3A25ØV1ØAS
A12A2F6	7-2-15	FØ2A25ØV3AS
A12A2J1	7-2-24	3614875
thru		
A12A2J4	7-2-24	3614875
A12A2XF1	7-2-17	HKU
A12A2XF2	7-2-16	FHL18G2-1
A12A2XF3	7-2-16	FHL18G2-1
A12A2XF4	7-2-17	HKU
A12A2XF5	7-2-16	FHL18G2-1
A12A2XF6	7-2-16	FHL18G2-1
A12A3	7-3	ØNØ6818Ø-2
A12A3F1	7-3-16	FØ3A25ØV8AS
A12A3F2	7-3-17	FØ3A25ØV1ØAS
A12A3F3	7-3-17	FØ3A25ØV1ØAS
A12A3F4	7-3-16	FØ3A25ØV8AS
A12A3F5	7-3-17	FØ3A25ØV1ØAS
A12A3F6	7-3-17	FØ3A25ØV1ØAS
A12A3J1	7-3-26	3614679
thru		
A12A3J4	7-3-26	3614679
A12A3XF1	7-3-19	HKU
A12A3XF2	7-3-18	FHL18G2-1
A12A3XF3	7-3-18	FHL18G2-1
A12A3XF4	7-3-19	HKU
A12A3XF5	7-3-18	FHL18G-1
A12A3XF6	7-3-18	FHL18G-1
A12A4	7-3	ØNØ6818Ø-2
A12A4F1	7-3-16	FØ3A25ØV8AS
A12A4F2	7-3-17	FØ3A25ØV1ØAS
A12A4F3	7-3-17	FØ3A25ØV1ØAS
A12A4F4	7-3-16	FØ3A25ØV8AS
A12A4F5	7-3-17	FØ3A25ØV1ØAS
A12A4F6	7-3-17	FØ3A25ØV1ØAS
A12A4J1	7-3-26	3614679
thru		
A12A4J4	7-3-26	3614679
A12A4XF1	7-3-19	HKU
A12A4XF2	7-3-18	FH618G-1
A12A4XF3	7-3-18	FH618G-1
A12A4XF4	7-3-19	HKU
A12A4XF5	7-8-18	FHL18G-1
A12A4XF6	7-8-18	FHL18G-1
A12J2	7-2-1Ø	DPD5Ø-34PIGF-32A115
thru		
A12J1Ø	7-2-1Ø	DPD5Ø-34PIGF-32A115
FL1	7-2-37	2ØJX31
FL2	7-2-37	2ØJX31
FL3	7-2-37	2ØJX31
J1	7-2-35	MS3102A20-15PW
PS1	7-1-16	ØN116826
PS1CR1	7-11-3Ø	1N1186
thru		
PS1CR24	7-11-3Ø	1N1186
PS1C1	7-11-11	CL26BH221UP3
thru		
PS1C4	7-11-11	CL26BH221UP3
PS1F1	7-11-4	FØ2B25ØV1AS
thru		
PS1F3	7-11-4	FØ2B25ØV1AS
PS1F4	7-11-3	FØ3B125V3AS
thru		
PS1F6	7-11-3	FØ3B125V3AS
PS1F7	7-11-2	FØ2B125V2AS
thru		
PS1F15	7-11-2	FØ2B125V2AS
PS1F16	7-11-1	FØ3B32V8AS
PS1F17	7-11-1	FØ3B32V8AS
PS1F18	7-11-1	FØ3B32V8AS
PS1J1	7-11-23	MS31Ø2A32-6P
PS1J2	7-11-24	MS31Ø2A32-6PW
PS1K1	7-11-18	MS25271-A1
PS1K2	7-11-18	MS25271-A1
PS1L1	7-11-15	S38Ø7
PS1L2	7-11-36	S3898
PS1R1	7-11-12	RCØ7GF1Ø4J
thru		
PS1R3	7-11-12	RCØ7GF1Ø4J
PS1TB1	7-11-29	37TB-11
PS1TB2	7-11-29	37TB-11
PS1T1	7-11-20	A17438
PS1T2	7-11-38	A17437
PS1T3	7-11-38	A17437
PS1T4	7-11-37	S4111B
PS1W1	7-11-21	ØNØ67Ø14
PS1W2	7-11-34	ØNØ6811Ø
PS1W3	7-11-34	ØNØ6811Ø
PS1W4	7-11-21	ØNØ67Ø14
PS1W5	7-11-21	ØNØ67Ø14
PS1W6	7-11-31	ØNØ68112
PS1W7	7-11-31	ØNØ68112
PS1XF1	7-11-5	HKU
PS1XF2	7-11-5	HKU
PS1XF3	7-11-5	HKU
PS1XF4	7-11-6	FHL18G2-1
thru		
PS1XF12	7-11-6	FHL18G2-1
PS1XF13	7-11-7	FHL17G
thru		
PS1XF18	7-11-7	FHL17G
P1	7-18-4	DPD45ØØ-52Ø7
P1	7-19-2	DPD45ØØ-52Ø7

REFERENCE DESIGNATOR INDEX

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER
P1	7-22-1	7411
P1	7-20-1	3614680
P2	7-18-4	DPD4500-5207
P2	7-19-3	DPD4500-5207
P2	7-20-2	3614679
P2	7-22-3	MS3106A20-15SW
P3	7-19-4	DPD4500-5207
S1	7-3-37	2AC6
S2	7-3-1	M221F1150405 41
S3	7-3-2	M221L1360405 41
S4	7-2-3	M221F1150405 41
S5	7-2-4	M221L1360405 41
W1	7-2-43	ØNØ68212
W2	7-2-44	ØNØ68213
W3	7-2-44	ØNØ68213
W4	7-2-44	ØNØ68213

REFERENCE DESIGNATION	FIG. AND INDEX NO.	PART NUMBER

APPENDIX A

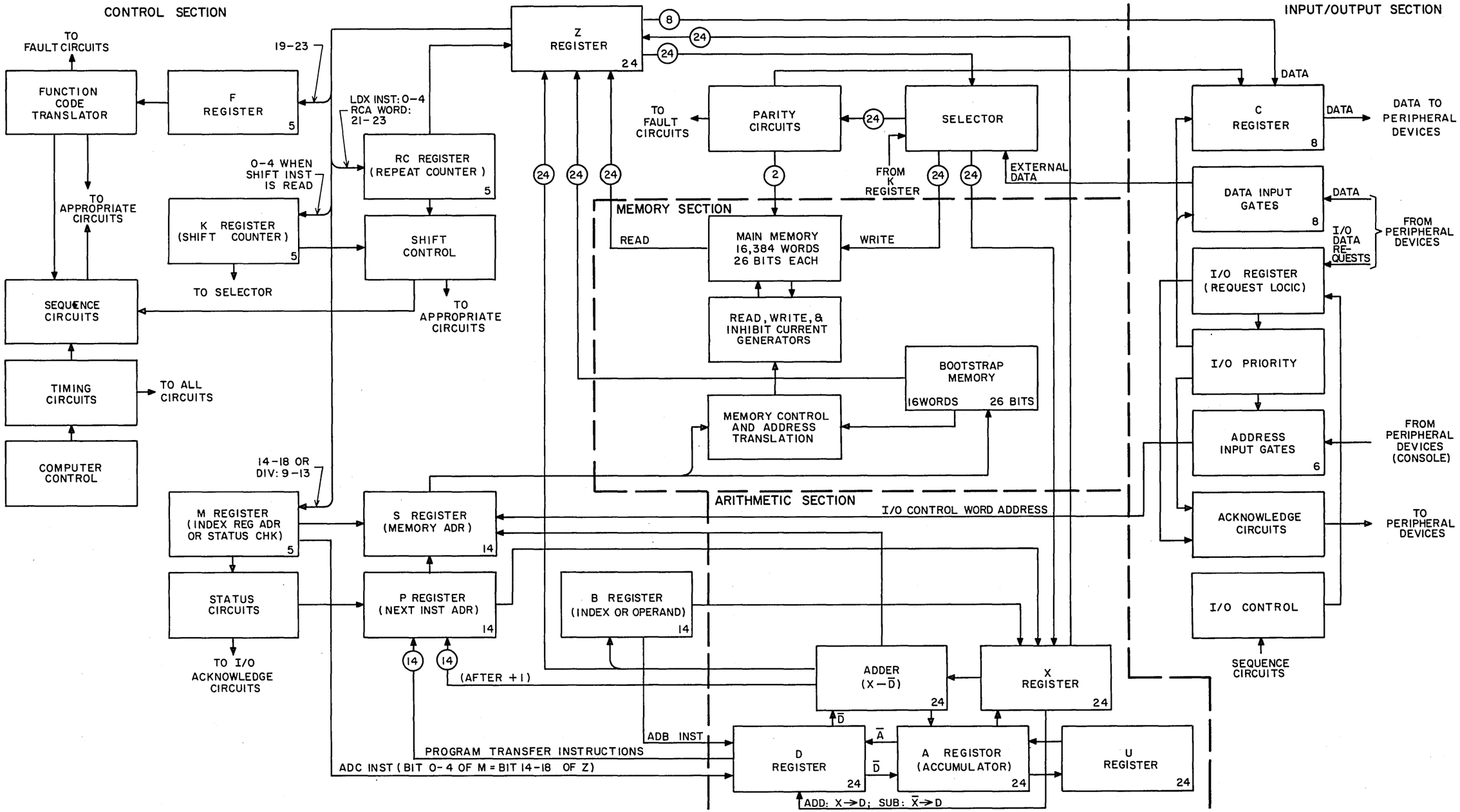


Figure A-1. CP-818A/U Computer, Block Diagram

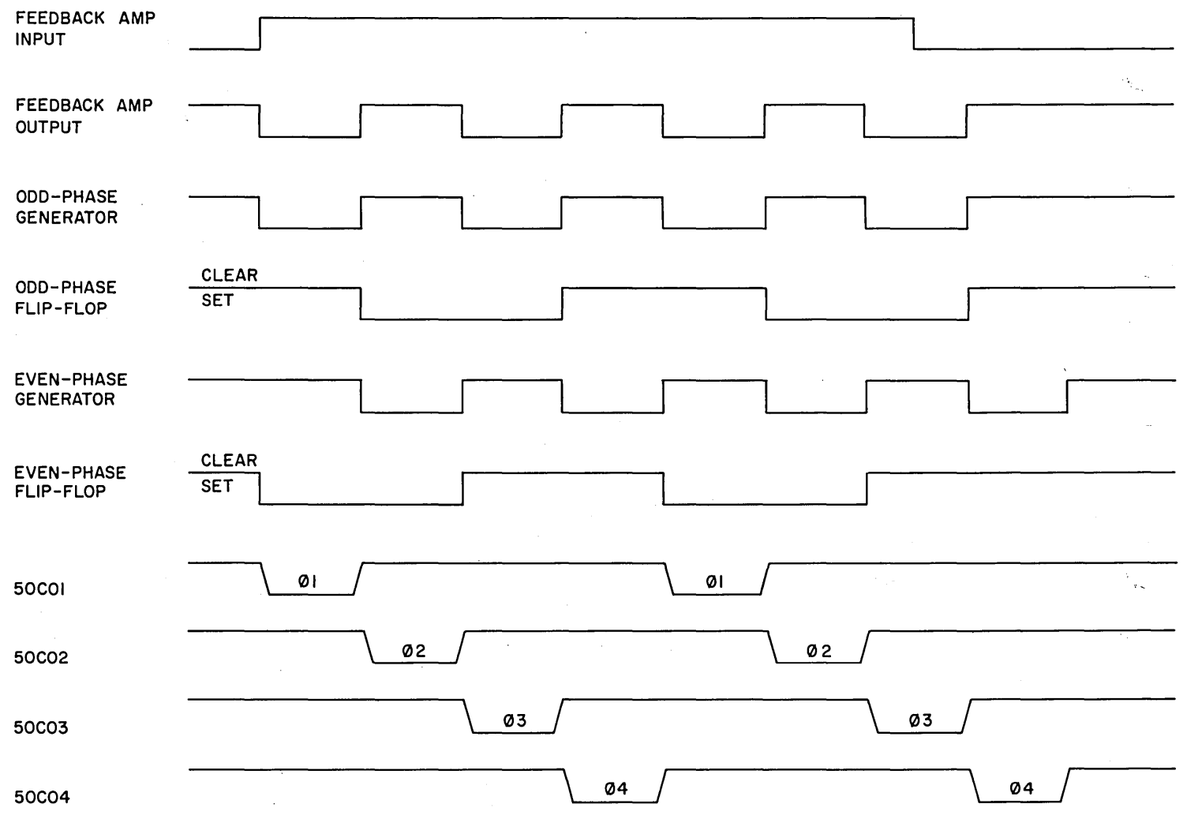


Figure A-2. Master Clock Timing Diagram

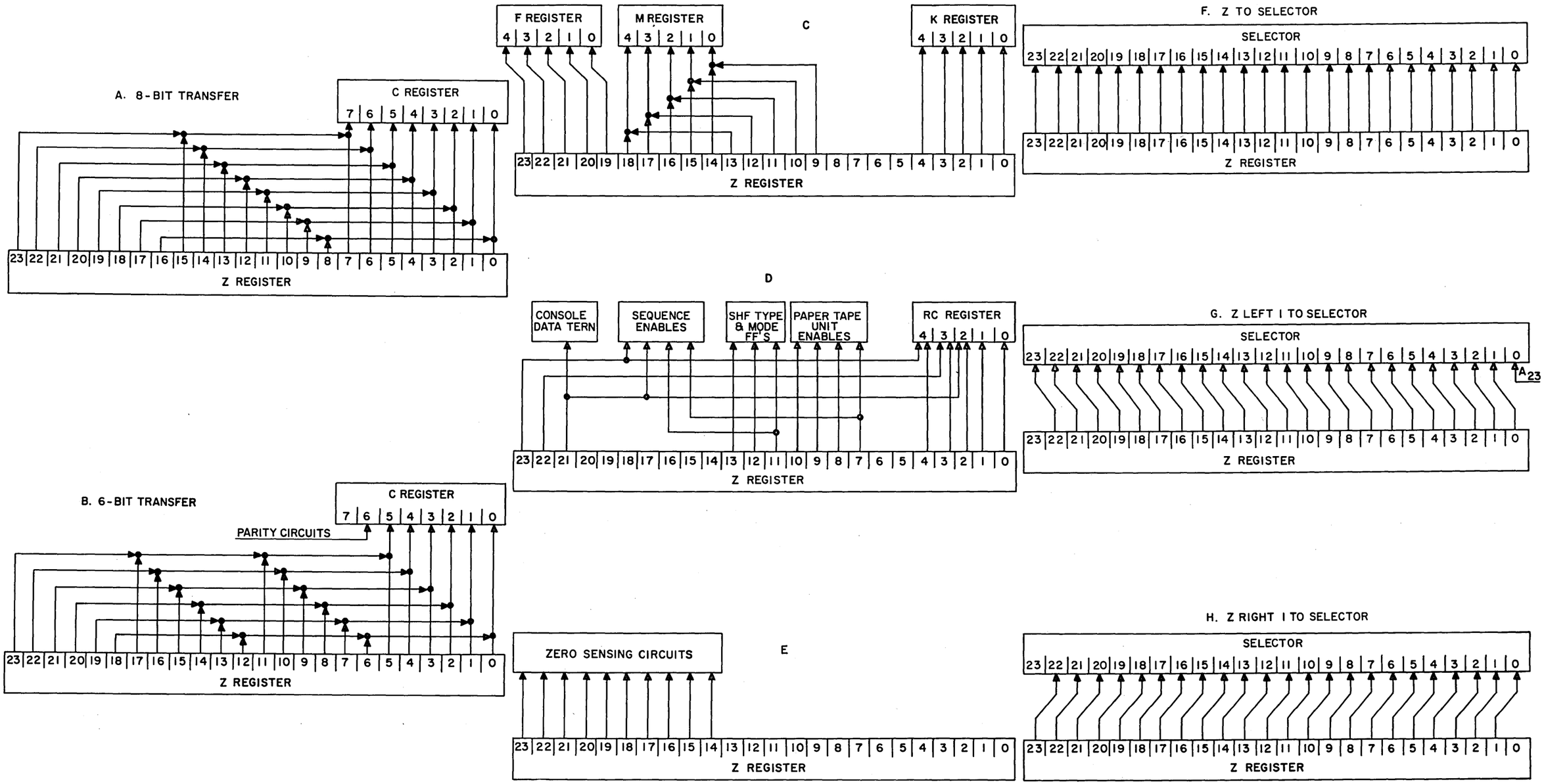
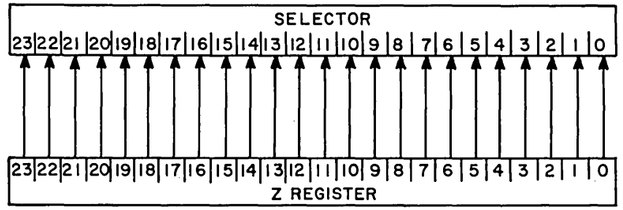
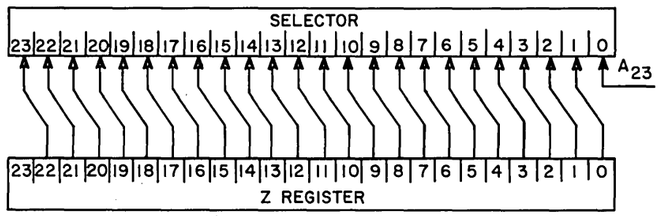


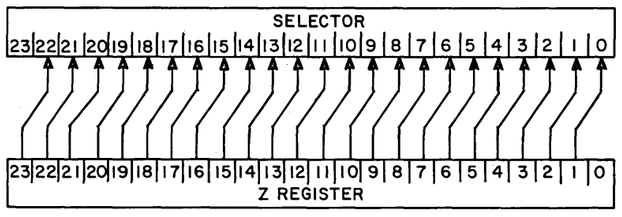
Figure A-3. Z-Register Outputs



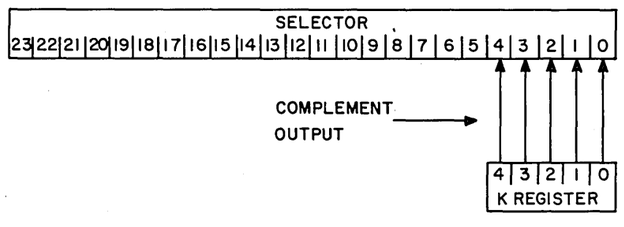
A. Z TO SELECTOR (INTERNAL DATA)



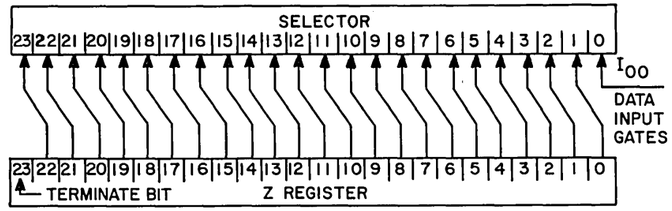
B. Z LEFT 1 TO SELECTOR (TYPE IX_2 SHIFT INSTRUCTION)



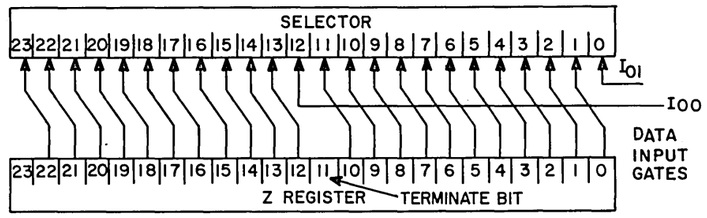
C. Z RIGHT 1 TO SELECTOR (TYPE IX_2 SHIFT INSTRUCTION)



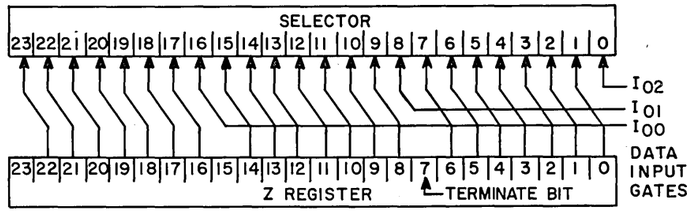
D. K TO SELECTOR



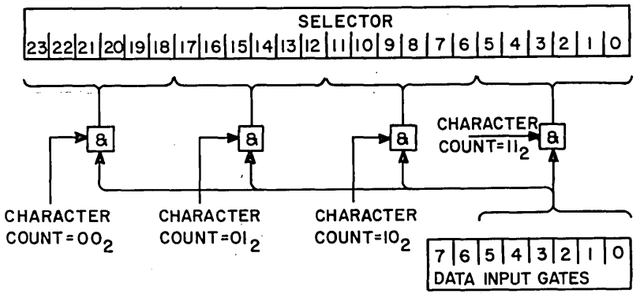
E. CONSOLE DATA INPUT MODE 1($X_{23-22}=00_2$) 1 BIT IN



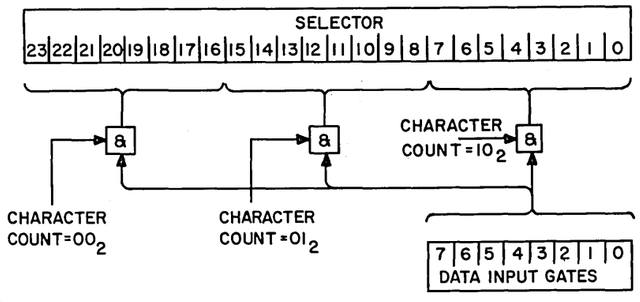
F. CONSOLE DATA INPUT MODE 2 ($X_{23-22}=01_2$) 2 BITS IN



G. CONSOLE DATA INPUT MODE 3($X_{23-22}=10_2$) 3 BITS IN



H. EXTERNAL INPUT DATA 6 BIT MODE



I. EXTERNAL INPUT DATA – 8 BIT MODE

Figure A-4. Selector Inputs

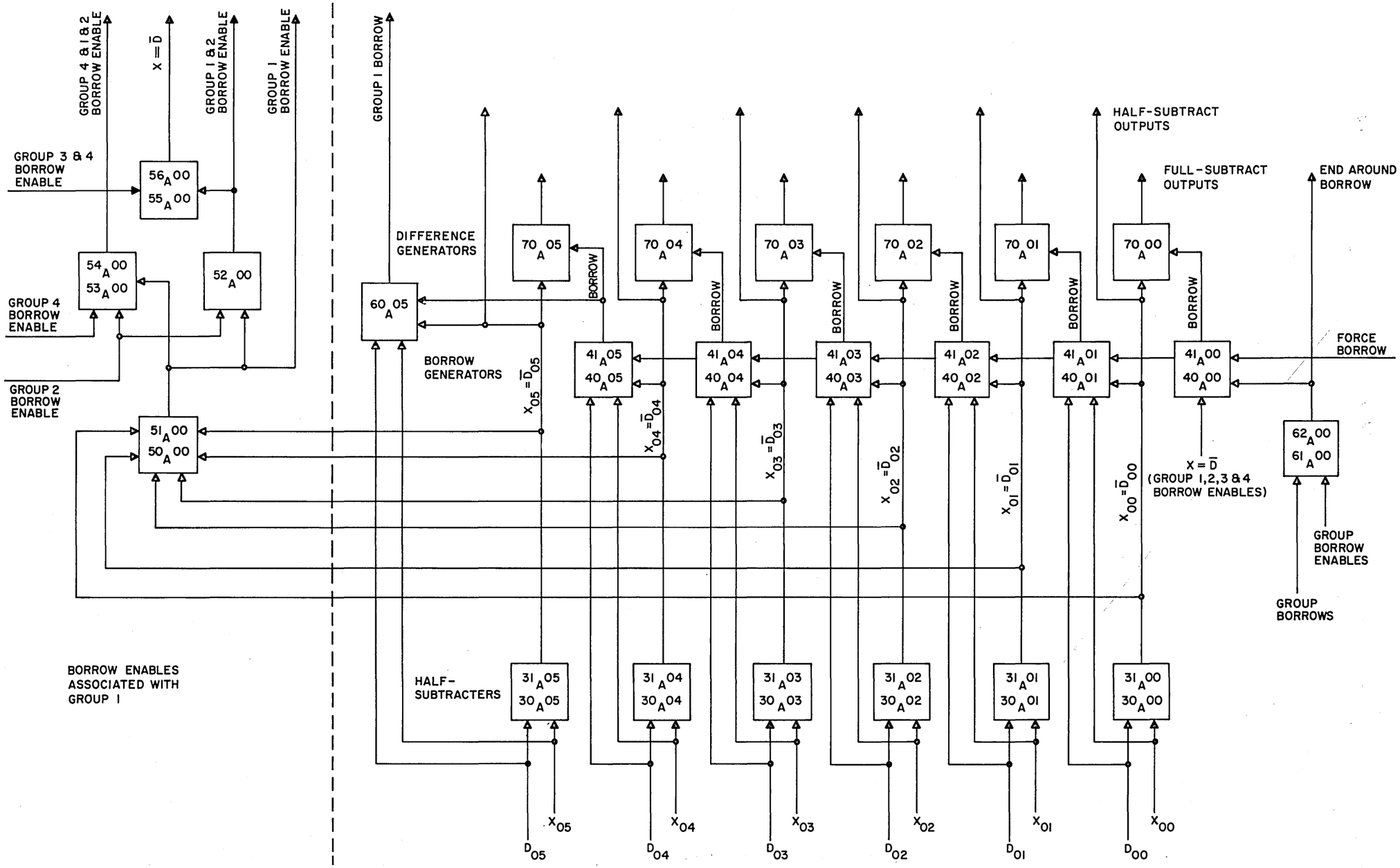


Figure A-5. Adder Group I, Simplified Diagram

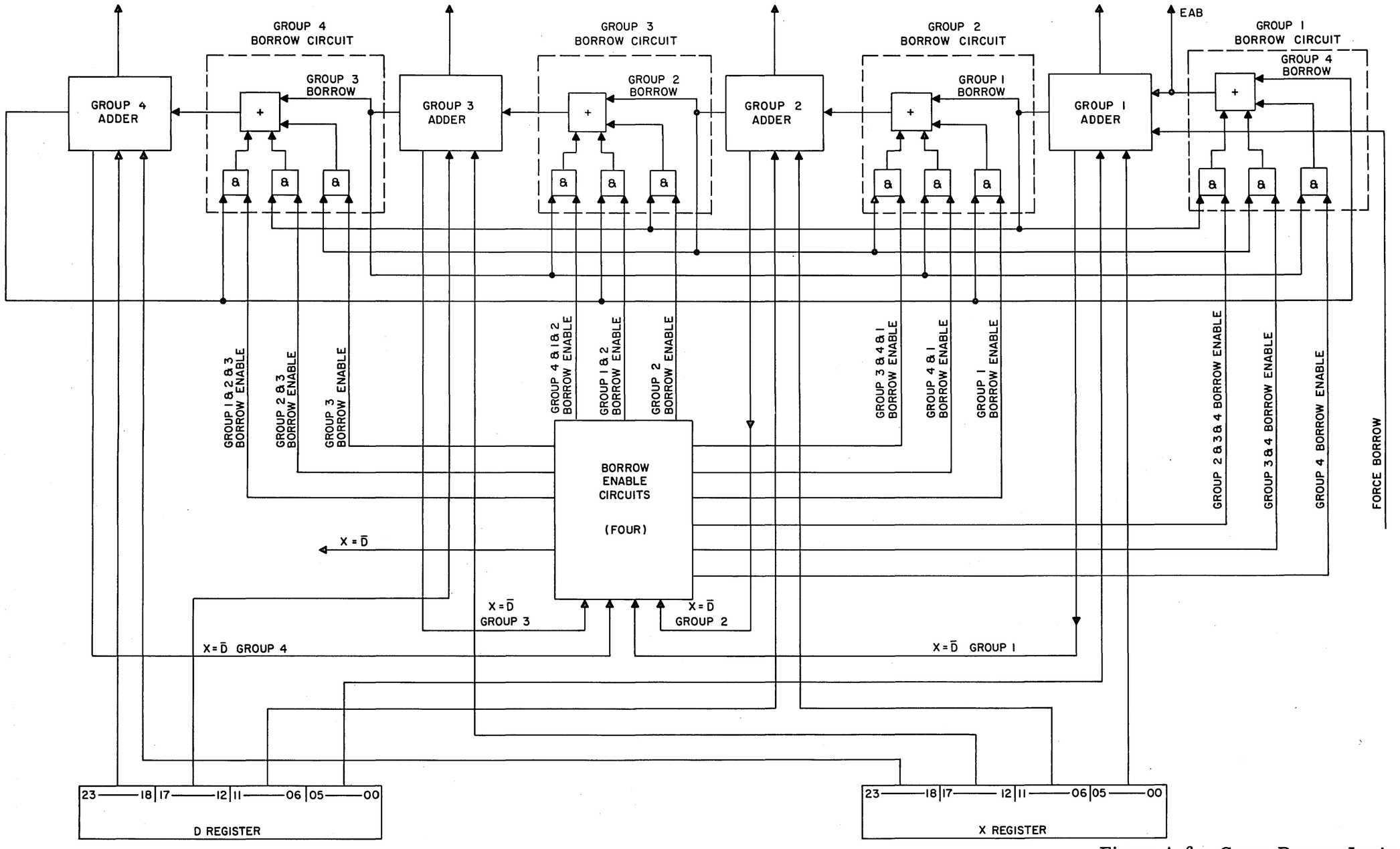


Figure A-6. Group Borrow Logic

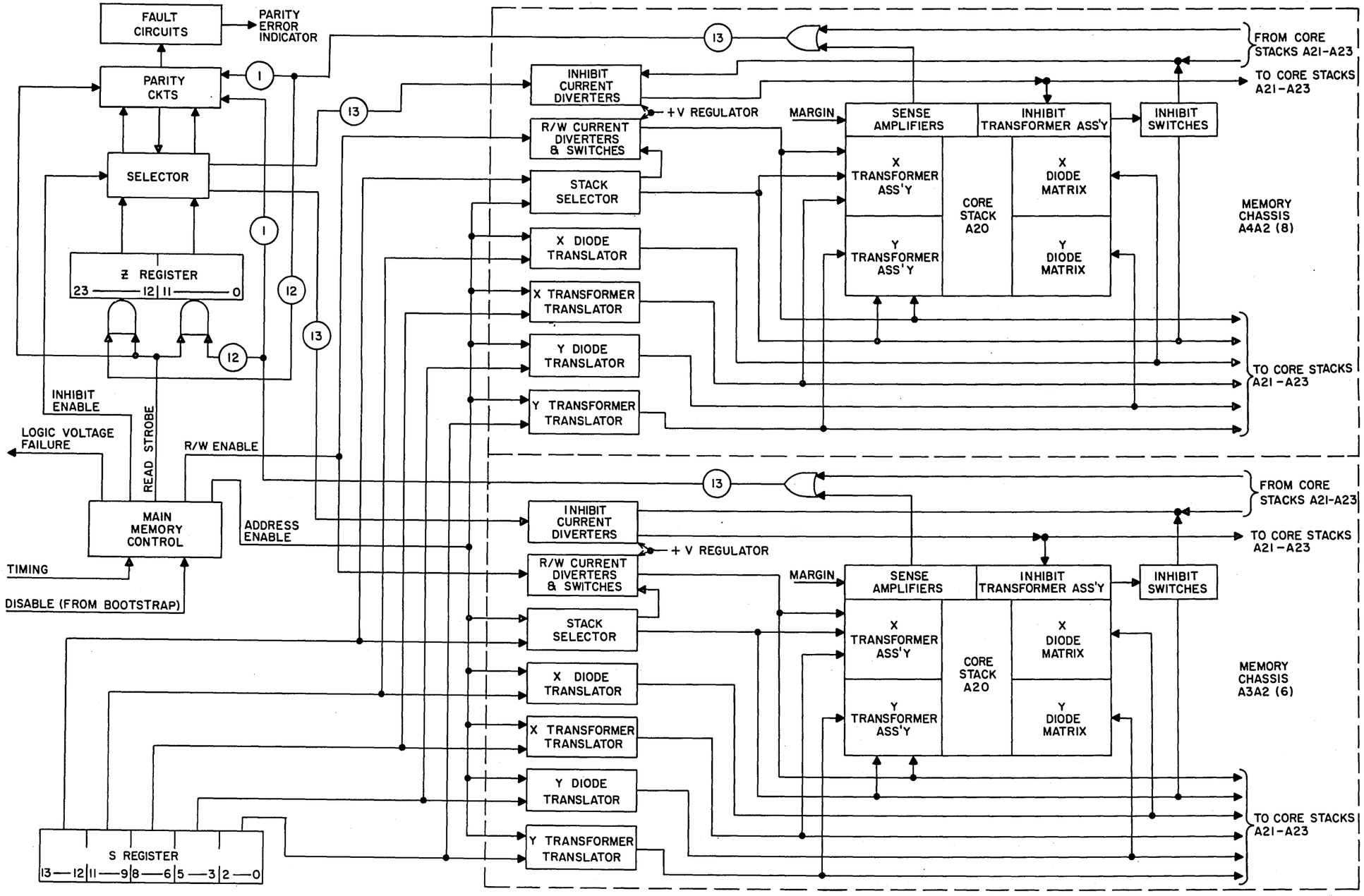


Figure A-7. Memory Block Diagram

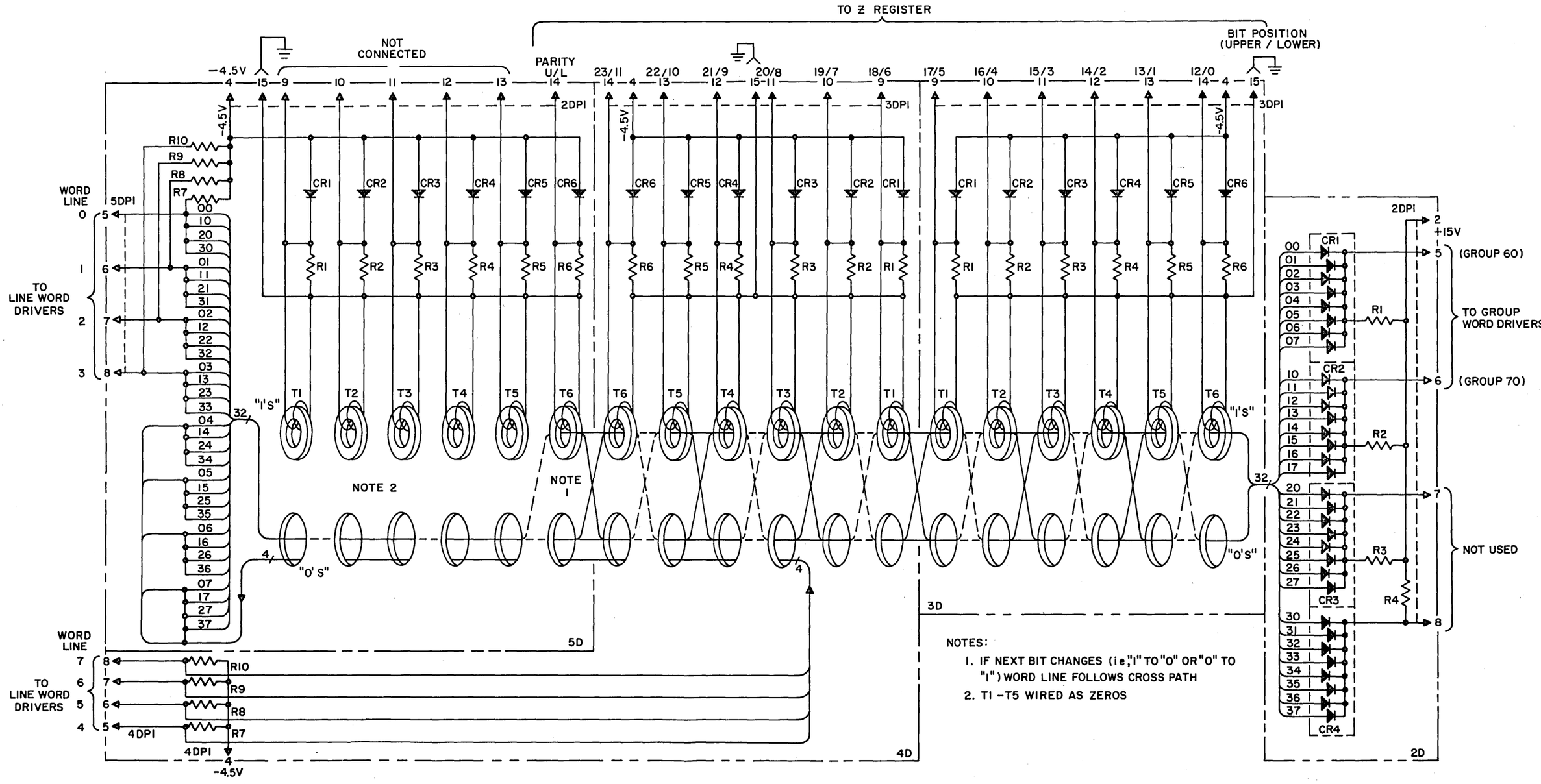


Figure A-8. Bootstrap Prewired Assembly

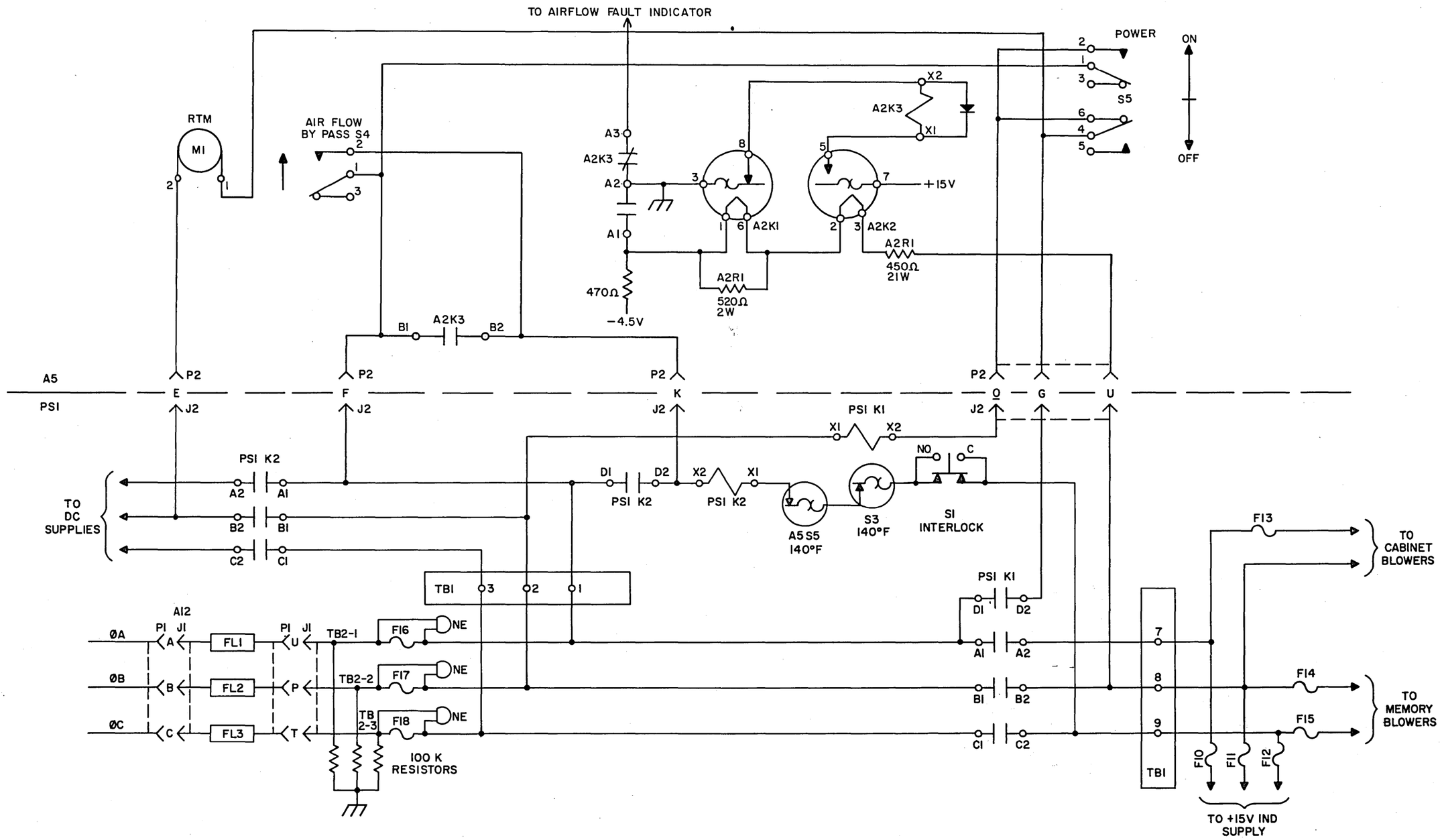


Figure A-9. Simplified AC Distribution, Schematic Diagram